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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc502-i-ss

TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES (CONTINUED)

Device	Page Erase Size (Instructions)	Program Flash Memory (Kbytes)	RAM (Kbytes)	Remappable Peripherals										CRC Generator	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	I/O Pins	Pins	Packages
				16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM ⁽⁴⁾ (Channels)	Quadrature Encoder Interface	UART	SPI ⁽²⁾	ECAN TM Technology	External Interrupts ⁽³⁾	I ² C TM								
dsPIC33EP32MC504	512	32	4	5	4	4	6	1	2	2	1	3	2	1	9	3/4	Yes	Yes	35	44/ 48	VTLA ⁽⁵⁾ , TQFP, QFN, UQFN
dsPIC33EP64MC504	1024	64	8																		
dsPIC33EP128MC504	1024	128	16																		
dsPIC33EP256MC504	1024	256	32																		
dsPIC33EP512MC504	1024	512	48	5	4	4	6	1	2	2	1	3	2	1	16	3/4	Yes	Yes	53	64	TQFP, QFN
dsPIC33EP64MC506	1024	64	8																		
dsPIC33EP128MC506	1024	128	16																		
dsPIC33EP256MC506	1024	256	32																		
dsPIC33EP512MC506	1024	512	48																		

- Note 1:** On 28-pin devices, Comparator 4 does not have external connections. Refer to **Section 25.0 "Op Amp/Comparator Module"** for details.
2: Only SPI2 is remappable.
3: INT0 is not remappable.
4: Only the PWM Faults are remappable.
5: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

FIGURE 4-9: DATA MEMORY MAP FOR dsPIC33EP128MC20X/50X AND dsPIC33EP128GP50X DEVICES

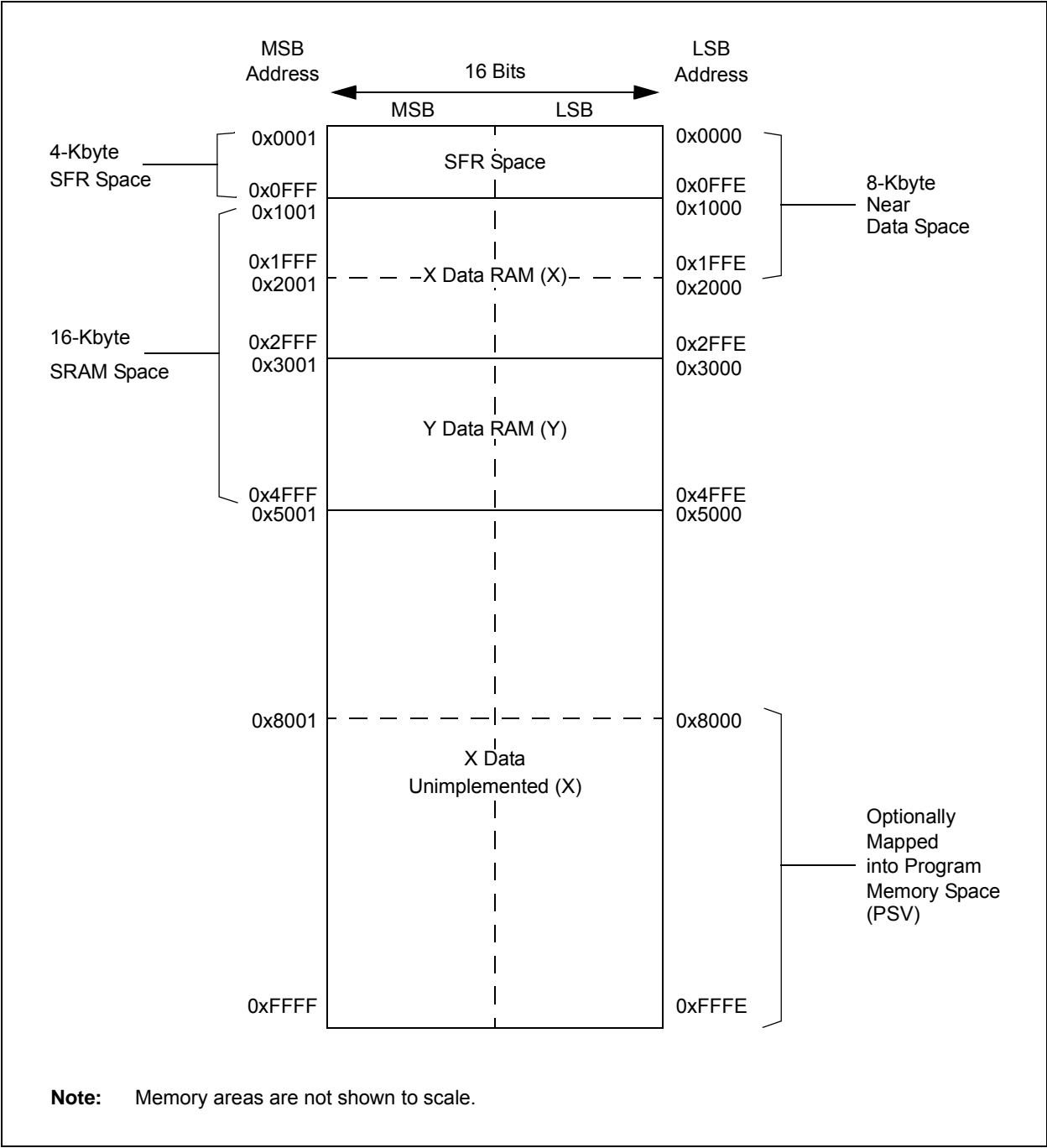


FIGURE 4-15: DATA MEMORY MAP FOR PIC24EP256GP/MC20X/50X DEVICES

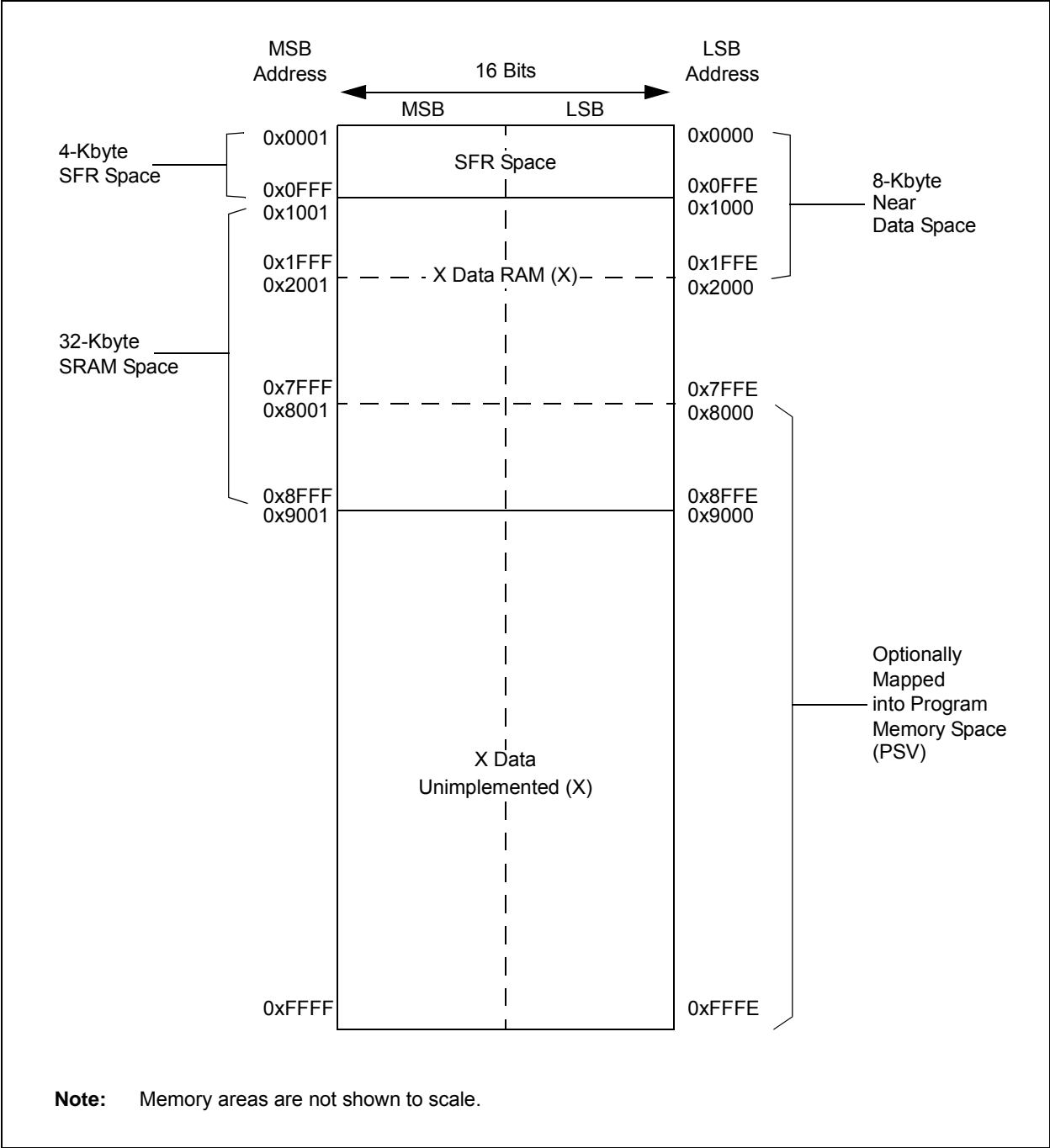


TABLE 4-52: PORTG REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	0E60	—	—	—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	—	—	03C0
PORTG	0E62	—	—	—	—	—	—	RG9	RG8	RG7	RG6	—	—	—	—	—	—	xxxx
LATG	0E64	—	—	—	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	—	—	xxxx
ODCG	0E66	—	—	—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	—	—	0000
CNENG	0E68	—	—	—	—	—	—	CNIEG9	CNIEG8	CNIEG7	CNIEG6	—	—	—	—	—	—	0000
CNPUG	0E6A	—	—	—	—	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	—	—	0000
CNPDG	0E6C	—	—	—	—	—	—	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

9.0 OSCILLATOR CONFIGURATION

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Oscillator**” (DS70580) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

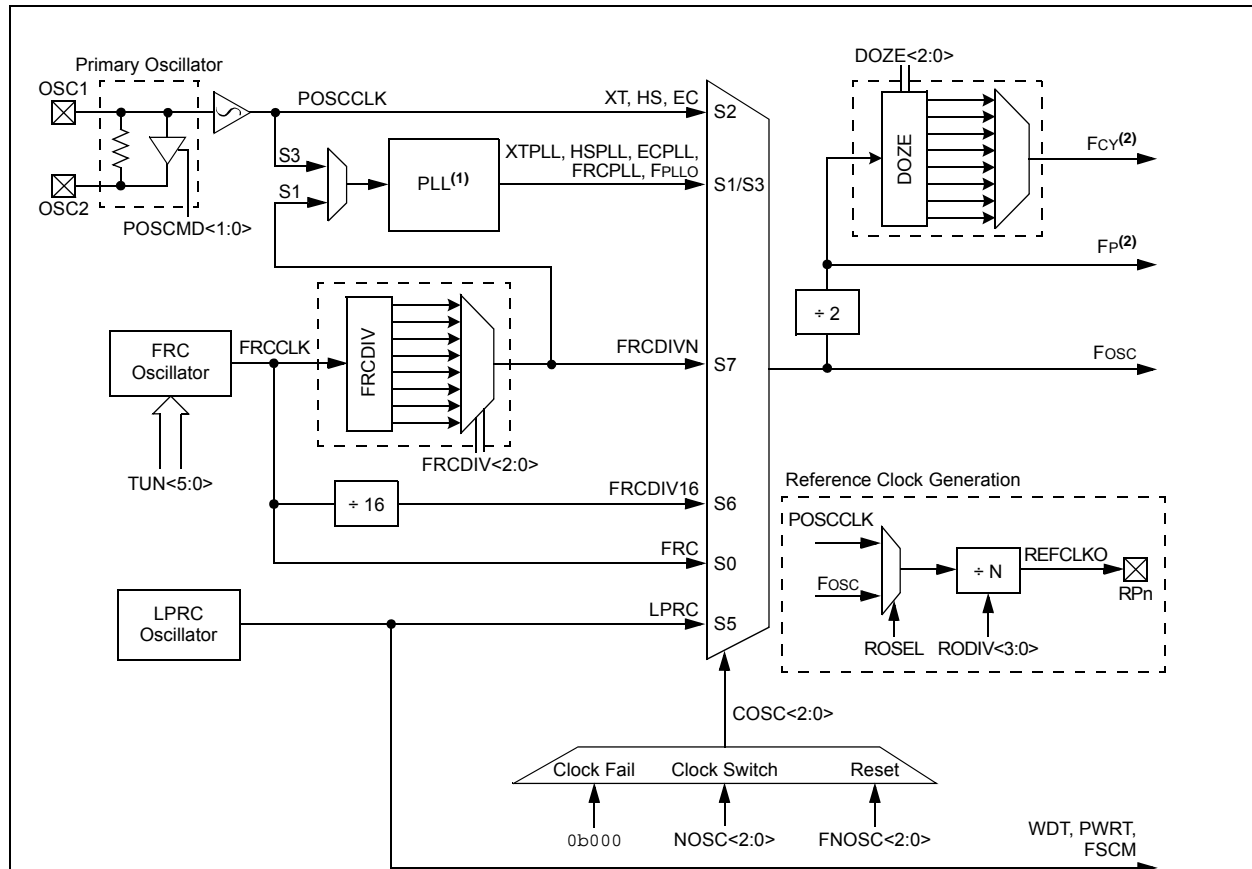
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X oscillator system provides:

- On-chip Phase-Locked Loop (PLL) to boost internal operating frequency on select internal and external oscillator sources
- On-the-fly clock switching between various clock sources
- Doze mode for system power savings
- Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Configuration bits for clock source selection

A simplified diagram of the oscillator system is shown in Figure 9-1.

FIGURE 9-1: OSCILLATOR SYSTEM DIAGRAM



Note 1: See Figure 9-2 for PLL details.

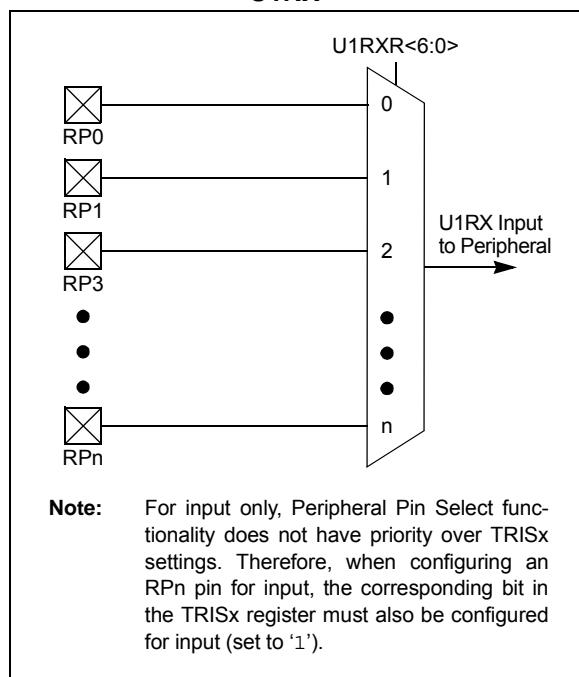
2: The term, Fp, refers to the clock source for all peripherals, while Fcy refers to the clock source for the CPU. Throughout this document, Fcy and Fp are used interchangeably, except in the case of Doze mode. Fp and Fcy will be different when Doze mode is used with a doze ratio of 1:2 or lower.

11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPNR_x registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-17). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPN pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



11.4.4.1 Virtual Connections

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 25-1 in **Section 25.0 “Op Amp/Comparator Module”**), and the PTG module (see **Section 24.0 “Peripheral Trigger Generator (PTG) Module”**).

In addition, dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support virtual connections to the filtered QE1 module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in **Section 17.0 “Quadrature Encoder Interface (QE1) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”**).

Virtual connections provide a simple way of inter-peripheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPNR12 register to the value of 'b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QE1 module allows peripherals to be connected to the QE1 digital filter input. To utilize this filter, the QE1 module must be enabled and its inputs must be connected to a physical RPN pin. Example 11-2 illustrates how the input capture module can be connected to the QE1 digital filter.

EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QE1 DIGITAL FILTER INPUT ON PIN 43 OF THE dsPIC33EPXXXMC206 DEVICE

```

RPNR15 = 0x2500;    /* Connect the QE1 HOME1 input to RP37 (pin 43) */
RPNR7  = 0x009;    /* Connect the IC1 input to the digital filter on the FHOME1 input */

QE1IOC = 0x4000;    /* Enable the QE1 digital filter */
QE1CON = 0x8000;    /* Enable the QE1 module */
    
```

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Peripheral Pin Select Input Register Value	Input/Output	Pin Assignment	Peripheral Pin Select Input Register Value	Input/Output	Pin Assignment
000 0000	I	Vss	010 1101	I	RPI45
000 0001	I	C1OUT ⁽¹⁾	010 1110	I	RPI46
000 0010	I	C2OUT ⁽¹⁾	010 1111	I	RPI47
000 0011	I	C3OUT ⁽¹⁾	011 0000	—	—
000 0100	I	C4OUT ⁽¹⁾	011 0001	—	—
000 0101	—	—	011 0010	—	—
000 0110	I	PTGO30 ⁽¹⁾	011 0011	I	RPI51
000 0111	I	PTGO31 ⁽¹⁾	011 0100	I	RPI52
000 1000	I	FINDX1 ^(1,2)	011 0101	I	RPI53
000 1001	I	FHOME1 ^(1,2)	011 0110	I/O	RP54
000 1010	—	—	011 0111	I/O	RP55
000 1011	—	—	011 1000	I/O	RP56
000 1100	—	—	011 1001	I/O	RP57
000 1101	—	—	011 1010	I	RPI58
000 1110	—	—	011 1011	—	—
000 1111	—	—	011 1100	—	—
001 0000	—	—	011 1101	—	—
001 0001	—	—	011 1110	—	—
001 0010	—	—	011 1111	—	—
001 0011	—	—	100 0000	—	—
001 0100	I/O	RP20	100 0001	—	—
001 0101	—	—	100 0010	—	—
001 0110	—	—	100 0011	—	—
001 0111	—	—	100 0100	—	—
001 1000	I	RPI24	100 0101	—	—
001 1001	I	RPI25	100 0110	—	—
001 1010	—	—	100 0111	—	—
001 1011	I	RPI27	100 1000	—	—
001 1100	I	RPI28	100 1001	—	—
001 1101	—	—	100 1010	—	—
001 1110	—	—	100 1011	—	—
001 1111	—	—	100 1100	—	—
010 0000	I	RPI32	100 1101	—	—
010 0001	I	RPI33	100 1110	—	—
010 0010	I	RPI34	100 1111	—	—
010 0011	I/O	RP35	101 0000	—	—
010 0100	I/O	RP36	101 0001	—	—
010 0101	I/O	RP37	101 0010	—	—
010 0110	I/O	RP38	101 0011	—	—
010 0111	I/O	RP39	101 0100	—	—

Legend: Shaded rows indicate PPS Input register values that are unimplemented.

Note 1: See Section 11.4.4.1 “Virtual Connections” for more information on selecting this pin assignment.

2: These inputs are available on dsPIC33EPXXXGP/MC50X devices only.

11.5 I/O Helpful Tips

1. In some cases, certain pins, as defined in Table 30-11, under “Injection Current”, have internal protection diodes to VDD and VSS. The term, “Injection Current”, is also referred to as “Clamp Current”. On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the VSS and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device, that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.
2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a ‘0’, regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a ‘0’.

Note: Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUs and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to $\sim(VDD - 0.8)$, not VDD. This value is still above the minimum V_{IH} of CMOS and TTL devices.
5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the V_{OH}/I_{OH} and V_{OL}/I_{OL} DC characteristic specification. The respective I_{OH} and I_{OL} current rating only applies to maintaining the corresponding output at or above the V_{OH} , and at or below the V_{OL} levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum V_{IH}/V_{IL} levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of this data sheet. For example:
 $V_{OH} = 2.4V @ I_{OH} = -8\text{ mA}$ and $V_{DD} = 3.3V$
 The maximum output current sourced by any 8 mA I/O pin = 12 mA.
 LED source current < 12 mA is technically permitted. Refer to the V_{OH}/I_{OH} graphs in **Section 30.0 “Electrical Characteristics”** for additional information.
6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:
 - a) Only one “output” function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).
 - b) It is possible to assign a “remappable output” function to multiple pins and externally short or tie them together for increased current drive.
 - c) If any “dedicated output” function is enabled on a pin, it will take precedence over any remappable “output” function.
 - d) If any “dedicated digital” (input or output) function is enabled on a pin, any number of “input” remappable functions can be mapped to the same pin.
 - e) If any “dedicated analog” function(s) are enabled on a given pin, “digital input(s)” of any kind will all be disabled, although a single “digital output”, at the user’s cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input provided there is no external analog input, such as for a built-in self-test.
 - f) Any number of “input” remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable “output”.

REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	IC32
bit 15							bit 8

R/W-0	R/W/HS-0	U-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1
ICTRIG ⁽²⁾	TRIGSTAT ⁽³⁾	—	SYNCSEL4 ⁽⁴⁾	SYNCSEL3 ⁽⁴⁾	SYNCSEL2 ⁽⁴⁾	SYNCSEL1 ⁽⁴⁾	SYNCSEL0 ⁽⁴⁾
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-9 **Unimplemented:** Read as '0'
- bit 8 **IC32:** Input Capture 32-Bit Timer Mode Select bit (Cascade mode)
 1 = Odd IC and Even IC form a single 32-bit input capture module⁽¹⁾
 0 = Cascade module operation is disabled
- bit 7 **ICTRIG:** Input Capture Trigger Operation Select bit⁽²⁾
 1 = Input source used to trigger the input capture timer (Trigger mode)
 0 = Input source used to synchronize the input capture timer to a timer of another module (Synchronization mode)
- bit 6 **TRIGSTAT:** Timer Trigger Status bit⁽³⁾
 1 = ICxTMR has been triggered and is running
 0 = ICxTMR has not been triggered and is being held clear
- bit 5 **Unimplemented:** Read as '0'

- Note 1:** The IC32 bit in both the Odd and Even IC must be set to enable Cascade mode.
- Note 2:** The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
- Note 3:** This bit is set by the selected input source (selected by SYNCSEL<4:0> bits). It can be read, set and cleared in software.
- Note 4:** Do not use the ICx module as its own Sync or Trigger source.
- Note 5:** This option should only be selected as a trigger source and not as a synchronization source.
- Note 6:** Each Input Capture x (ICx) module has one PTG input source. See **Section 24.0 “Peripheral Trigger Generator (PTG) Module”** for more information.
 PTGO8 = IC1
 PTGO9 = IC2
 PTGO10 = IC3
 PTGO11 = IC4

REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)

bit 4-2 **SPRE<2:0>**: Secondary Prescale bits (Master mode)⁽³⁾

111 = Secondary prescale 1:1

110 = Secondary prescale 2:1

•

•

•

000 = Secondary prescale 8:1

bit 1-0 **PPRE<1:0>**: Primary Prescale bits (Master mode)⁽³⁾

11 = Primary prescale 1:1

10 = Primary prescale 4:1

01 = Primary prescale 16:1

00 = Primary prescale 64:1

- Note 1:** The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
- 2:** This bit must be cleared when FRMEN = 1.
- 3:** Do not set both primary and secondary prescalers to the value of 1:1.

REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0
bit 7							bit 0

Legend: C = Writable bit, but only '0' can be written to clear the bit
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **RXOVF<15:0>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16
bit 7							bit 0

Legend: C = Writable bit, but only '0' can be written to clear the bit
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **RXOVF<31:16>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

REGISTER 21-26: CxTRmnCON: ECANx TX/RX BUFFER mn CONTROL REGISTER
(m = 0,2,4,6; n = 1,3,5,7)

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI1	TXnPRI0
bit 15							bit 8

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm ⁽¹⁾	TXLARBm ⁽¹⁾	TXERRm ⁽¹⁾	TXREQm	RTRENm	TXmPRI1	TXmPRI0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 See Definition for bits<7:0>, Controls Buffer n

bit 7 **TXENm:** TX/RX Buffer Selection bit

1 = Buffer TRBn is a transmit buffer

0 = Buffer TRBn is a receive buffer

bit 6 **TXABTm:** Message Aborted bit⁽¹⁾

1 = Message was aborted

0 = Message completed transmission successfully

bit 5 **TXLARBm:** Message Lost Arbitration bit⁽¹⁾

1 = Message lost arbitration while being sent

0 = Message did not lose arbitration while being sent

bit 4 **TXERRm:** Error Detected During Transmission bit⁽¹⁾

1 = A bus error occurred while the message was being sent

0 = A bus error did not occur while the message was being sent

bit 3 **TXREQm:** Message Send Request bit

1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent

0 = Clearing the bit to '0' while set requests a message abort

bit 2 **RTRENm:** Auto-Remote Transmit Enable bit

1 = When a remote transmit is received, TXREQ will be set

0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXmPRI<1:0>:** Message Transmission Priority bits

11 = Highest message priority

10 = High intermediate message priority

01 = Low intermediate message priority

00 = Lowest message priority

Note 1: This bit is cleared when TXREQ is set.

Note: The buffers, SID, EID, DLC, Data Field, and Receive Status registers are located in DMA RAM.

BUFFER 21-3: ECAN™ MESSAGE BUFFER WORD 2

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1
bit 15							bit 8

U-x	U-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	RB0	DLC3	DLC2	DLC1	DLC0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-10 **EID<5:0>**: Extended Identifier bits
- bit 9 **RTR**: Remote Transmission Request bit
When IDE = 1:
1 = Message will request remote transmission
0 = Normal message
When IDE = 0:
The RTR bit is ignored.
- bit 8 **RB1**: Reserved Bit 1
User must set this bit to '0' per CAN protocol.
- bit 7-5 **Unimplemented**: Read as '0'
- bit 4 **RB0**: Reserved Bit 0
User must set this bit to '0' per CAN protocol.
- bit 3-0 **DLC<3:0>**: Data Length Code bits

BUFFER 21-4: ECAN™ MESSAGE BUFFER WORD 3

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 1							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 0							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-8 **Byte 1<15:8>**: ECAN Message Byte 1 bits
- bit 7-0 **Byte 0<7:0>**: ECAN Message Byte 0 bits

**REGISTER 25-4: CMxMSKSRCA: COMPARATOR x MASK SOURCE SELECT
CONTROL REGISTER (CONTINUED)**

bit 3-0 **SELSRCA<3:0>**: Mask A Input Select bits

1111 = FLT4
1110 = FLT2
1101 = PTGO19
1100 = PTGO18
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

TABLE 27-2: CONFIGURATION BITS DESCRIPTION

Bit Field	Description
GCP	General Segment Code-Protect bit 1 = User program memory is not code-protected 0 = Code protection is enabled for the entire program memory space
GWRP	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	Two-Speed Oscillator Start-up Enable bit 1 = Start up device with FRC, then automatically switch to the user-selected oscillator source when ready 0 = Start up device with user-selected oscillator source
PWMLOCK ⁽¹⁾	PWM Lock Enable bit 1 = Certain PWM registers may only be written after a key sequence 0 = PWM registers may be written without a key sequence
FNOSC<2:0>	Oscillator Selection bits 111 = Fast RC Oscillator with Divide-by-N (FRCDIVN) 110 = Fast RC Oscillator with Divide-by-16 (FRCDIV16) 101 = Low-Power RC Oscillator (LPRC) 100 = Reserved; do not use 011 = Primary Oscillator with PLL module (XT + PLL, HS + PLL, EC + PLL) 010 = Primary Oscillator (XT, HS, EC) 001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCPLL) 000 = Fast RC Oscillator (FRC)
FCKSM<1:0>	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	Peripheral Pin Select Configuration bit 1 = Allow only one reconfiguration 0 = Allow multiple reconfigurations
OSCIOFNC	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is a general purpose digital I/O pin
POSCMD<1:0>	Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode
FWDTEN	Watchdog Timer Enable bit 1 = Watchdog Timer is always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.) 0 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)
WINDIS	Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode
PLLKEN	PLL Lock Enable bit 1 = PLL lock is enabled 0 = PLL lock is disabled

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

2: When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

30.1 DC Characteristics

TABLE 30-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temp Range (in °C)	Maximum MIPS
			dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X
—	3.0V to 3.6V ⁽¹⁾	-40°C to +85°C	70
—	3.0V to 3.6V ⁽¹⁾	-40°C to +125°C	60

Note 1: Device is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

TABLE 30-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal chip power dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \sum I_{OH})$ I/O Pin Power Dissipation: $I/O = \sum (\{V_{DD} - V_{OH}\} \times I_{OH}) + \sum (V_{OL} \times I_{OL})$	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	$(T_J - T_A)/\theta_{JA}$			W

TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 64-Pin QFN	θ_{JA}	28.0	—	°C/W	1
Package Thermal Resistance, 64-Pin TQFP 10x10 mm	θ_{JA}	48.3	—	°C/W	1
Package Thermal Resistance, 48-Pin UQFN 6x6 mm	θ_{JA}	41	—	°C/W	1
Package Thermal Resistance, 44-Pin QFN	θ_{JA}	29.0	—	°C/W	1
Package Thermal Resistance, 44-Pin TQFP 10x10 mm	θ_{JA}	49.8	—	°C/W	1
Package Thermal Resistance, 44-Pin VTLA 6x6 mm	θ_{JA}	25.2	—	°C/W	1
Package Thermal Resistance, 36-Pin VTLA 5x5 mm	θ_{JA}	28.5	—	°C/W	1
Package Thermal Resistance, 28-Pin QFN-S	θ_{JA}	30.0	—	°C/W	1
Package Thermal Resistance, 28-Pin SSOP	θ_{JA}	71.0	—	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θ_{JA}	69.7	—	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θ_{JA}	60.0	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

FIGURE 30-7: OUTPUT COMPARE x MODULE (OCx) TIMING CHARACTERISTICS

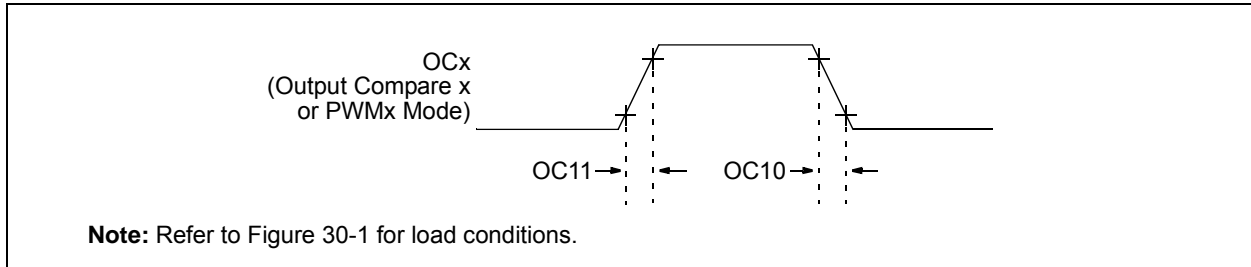


TABLE 30-27: OUTPUT COMPARE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See Parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter DO31

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-8: OCx/PWMx MODULE TIMING CHARACTERISTICS

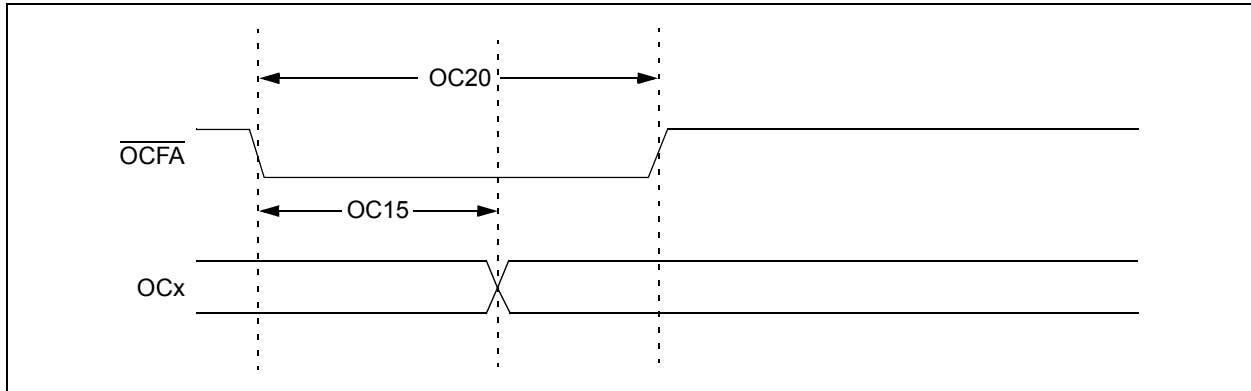
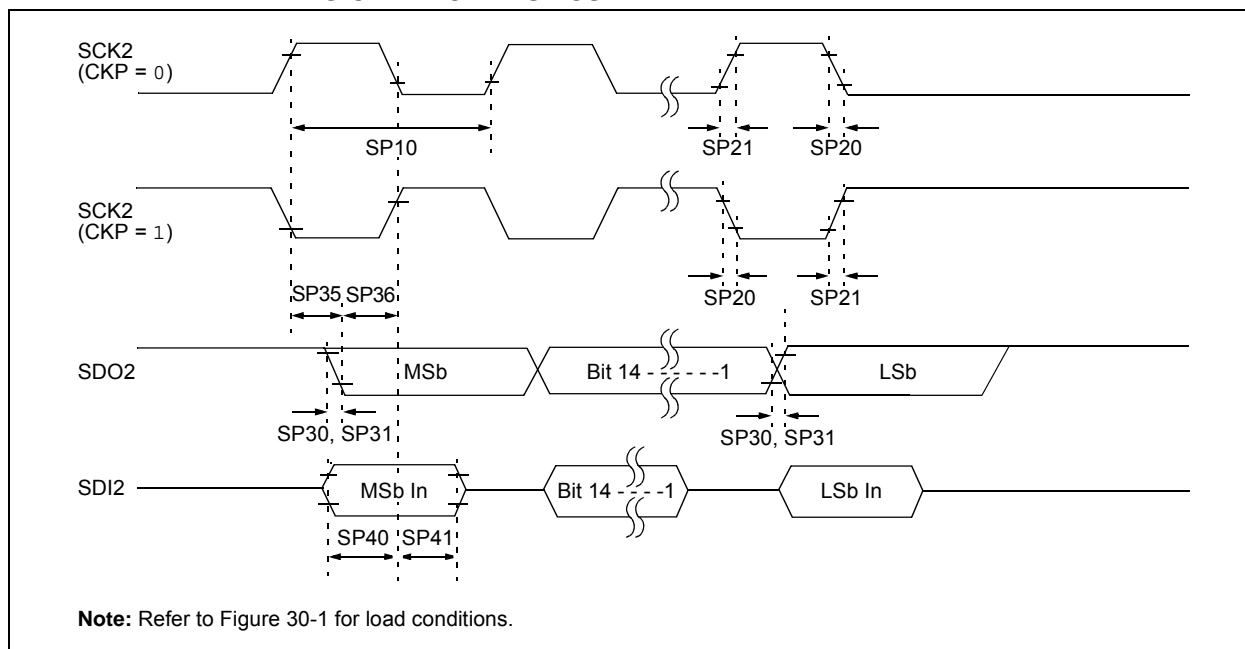


TABLE 30-28: OCx/PWMx MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC15	TFD	Fault Input to PWMx I/O Change	—	—	$T_{CY} + 20$	ns	
OC20	TFLT	Fault Input Pulse Width	$T_{CY} + 20$	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

**FIGURE 30-17: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)
TIMING CHARACTERISTICS**



**TABLE 30-36: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK2 Frequency	—	—	9	MHz	-40°C to +125°C (Note 3)
SP20	TscF	SCK2 Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK2 Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

**TABLE 30-38: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	—	—	Lesser of Fp or 11	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2} \downarrow$ to SCK2 \uparrow or SCK2 \downarrow Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS2} \uparrow$ to SDO2 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	Tsch2ssH TscL2ssH	$\overline{SS2} \uparrow$ after SCK2 Edge	1.5 Tcy + 40	—	—	ns	(Note 4)
SP60	TssL2doV	SDO2 Data Output Valid after $\overline{SS2}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

FIGURE 32-5: TYPICAL I_{PD} CURRENT @ $V_{DD} = 3.3V$

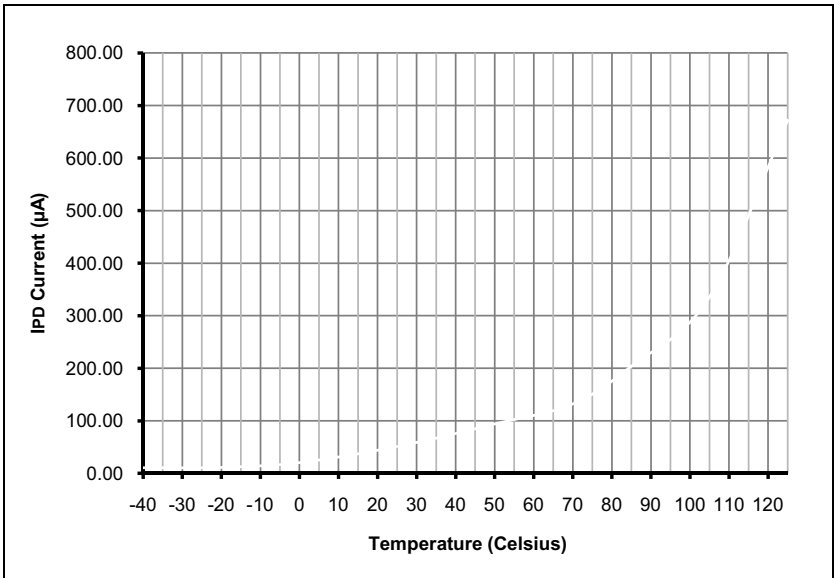


FIGURE 32-6: TYPICAL/MAXIMUM I_{DD} CURRENT @ $V_{DD} = 3.3V$

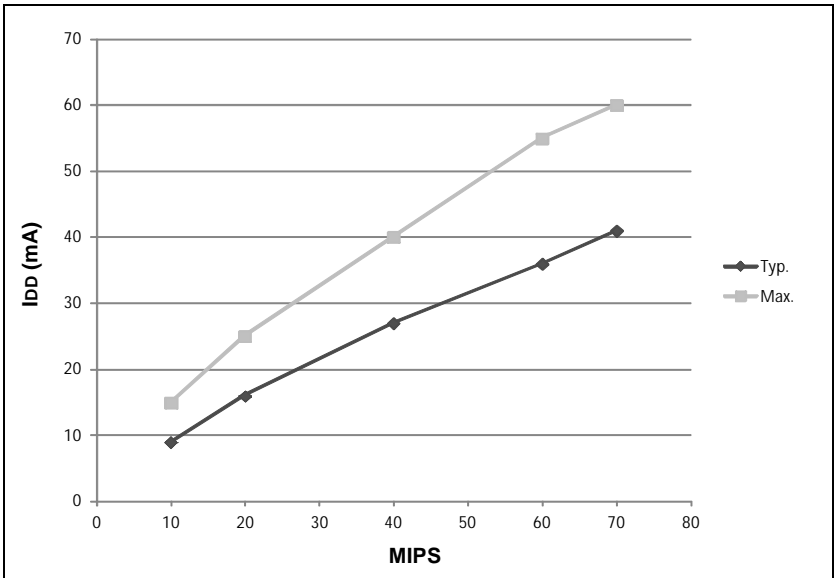


FIGURE 32-7: TYPICAL I_{DOZE} CURRENT @ $V_{DD} = 3.3V$

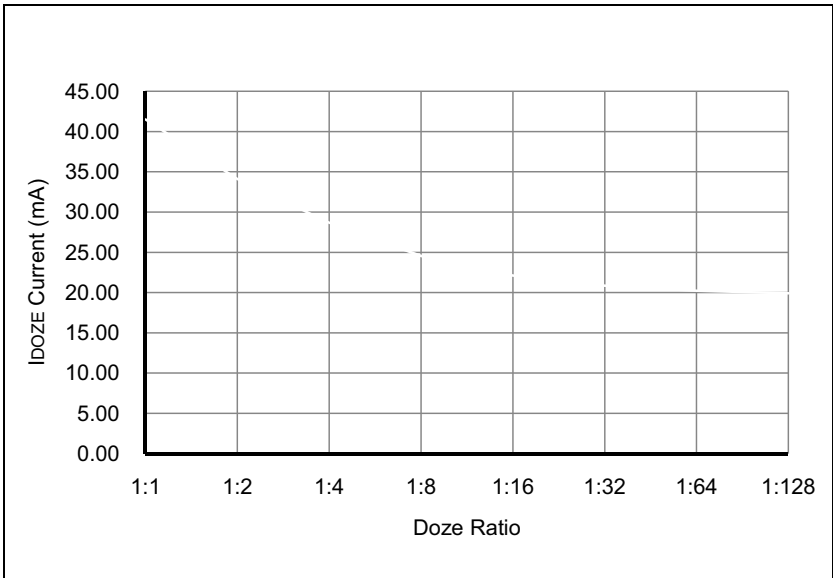


FIGURE 32-8: TYPICAL I_{IDLE} CURRENT @ $V_{DD} = 3.3V$

