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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc503-e-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### 2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 3 MHz <  $F_{IN}$  < 5.5 MHz to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start-up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLFBD, to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

### 2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between Vss and unused pins, and drive the output to logic low.

### 2.9 Application Examples

- · Induction heating
- Uninterruptable Power Supplies (UPS)
- DC/AC inverters
- · Compressor motor control
- · Washing machine 3-phase motor control
- BLDC motor control
- · Automotive HVAC, cooling fans, fuel pumps
- Stepper motor control
- · Audio and fluid sensor monitoring
- · Camera lens focus and stability control
- Speech (playback, hands-free kits, answering machines, VoIP)
- Consumer audio
- Industrial and building control (security systems and access control)
- · Barcode reading
- Networking: LAN switches, gateways
- Data storage device management
- · Smart cards and smart card readers

Examples of typical application connections are shown in Figure 2-4 through Figure 2-8.

#### FIGURE 2-4: BOOST CONVERTER IMPLEMENTATION



#### FIGURE 2-7: INTERLEAVED PFC







#### EXAMPLE 4-3: PAGED DATA MEMORY SPACE

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X



### TABLE 4-64: BIT-REVERSED ADDRESSING SEQUENCE (16-ENTRY)

Normal Address						Bit-Rev	ersed Ac	ldress	
A3	A2	A1	A0	Decimal	A3	A2	A1	A0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

## REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 4	MATHERR: Math Error Status bit
	1 = Math error trap has occurred
	0 = Math error trap has not occurred
bit 3	ADDRERR: Address Error Trap Status bit
	<ul><li>1 = Address error trap has occurred</li><li>0 = Address error trap has not occurred</li></ul>
bit 2	STKERR: Stack Error Trap Status bit
	1 = Stack error trap has occurred
	0 = Stack error trap has not occurred
bit 1	<b>OSCFAIL:</b> Oscillator Failure Trap Status bit
	1 = Oscillator failure trap has occurred
	0 = Oscillator failure trap has not occurred
bit 0	Unimplemented: Read as '0'

Note 1: These bits are available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

NOTES:

### 13.2 Timer Control Registers

R/M/ 0	11.0		11.0	11.0	11.0	11.0	11.0
	0-0		0-0	0-0	0-0	0-0	0-0
bit 15		TOIDE	_				
51115							bit 0
U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
	TGATE	TCKPS1	TCKPS0	T32	_	TCS	_
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	iown
bit 15	When T32 = 1           1 = Starts 32-1           0 = Stops 32-1           When T32 = 0           1 = Starts 16-1           0 = Stops 16-1	On bit L: bit Timerx/y bit Timerx/y <u>):</u> bit Timerx bit Timerx					
bit 14	Unimplement	ted: Read as 'd	)'				
bit 13	TSIDL: Timer	x Stop in Idle M	lode bit				
	1 = Discontinu 0 = Continues	ues module opera	eration when o tion in Idle mo	device enters I ode	dle mode		
bit 12-7	Unimplement	ted: Read as '	י)				
bit 6	<b>TGATE:</b> Timerx Gated Time Accumulation Enable bit         When TCS = 1:         This bit is ignored.         When TCS = 0:         1 = Gated time accumulation is enabled         0 = Gated time accumulation is disabled						
bit 5-4	TCKPS<1:0>	: Timerx Input (	Clock Prescal	e Select bits			
	11 = 1:256 10 = 1:64 01 = 1:8 00 = 1:1						
bit 3	<b>T32:</b> 32-Bit Timer Mode Select bit 1 = Timerx and Timery form a single 32-bit timer 0 = Timerx and Timery act as two 16-bit timers						
bit 2	Unimplement	ted: Read as 'd	י)				
bit 1	<b>TCS:</b> Timerx Clock Source Select bit 1 = External clock is from pin, TxCK (on the rising edge)						
bit 0	Unimplement	ted: Read as '	)'				

## REGISTER 13-1: TxCON: (TIMER2 AND TIMER4) CONTROL REGISTER

## 16.0 HIGH-SPEED PWM MODULE (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "High-Speed PWM" (DS70645) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support a dedicated Pulse-Width Modulation (PWM) module with up to 6 outputs.

The high-speed PWMx module consists of the following major features:

- Three PWM generators
- Two PWM outputs per PWM generator
- Individual period and duty cycle for each PWM pair
- Duty cycle, dead time, phase shift and frequency resolution of Tcy/2 (7.14 ns at Fcy = 70MHz)
- Independent Fault and current-limit inputs for six PWM outputs
- · Redundant output
- Center-Aligned PWM mode
- Output override control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Prescaler for input clock
- PWMxL and PWMxH output pin swapping
- Independent PWM frequency, duty cycle and phase-shift changes for each PWM generator
- Dead-time compensation
- Enhanced Leading-Edge Blanking (LEB) functionality
- Frequency resolution enhancement
- PWM capture functionality

**Note:** In Edge-Aligned PWM mode, the duty cycle, dead time, phase shift and frequency resolution are 8.32 ns.

The high-speed PWMx module contains up to three PWM generators. Each PWM generator provides two PWM outputs: PWMxH and PWMxL. The master time base generator provides a synchronous signal as a common time base to synchronize the various PWM outputs. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limit signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known "safe" state.

Each PWMx can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWMx module also generates a Special Event Trigger to the ADC module based on either of the two master time bases.

The high-speed PWMx module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNCI1 input pin that utilizes PPS, can synchronize the high-speed PWMx module with an external signal. The SYNCO1 pin is an output pin that provides a synchronous signal to an external device.

Figure 16-1 illustrates an architectural overview of the high-speed PWMx module and its interconnection with the CPU and other peripherals.

### 16.1 PWM Faults

The PWMx module incorporates multiple external Fault inputs to include FLT1 and FLT2 which are remappable using the PPS feature, FLT3 and FLT4 which are available only on the larger 44-pin and 64-pin packages, and FLT32 which has been implemented with Class B safety features, and is available on a fixed pin on all dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

These Faults provide a safe and reliable way to safely shut down the PWM outputs when the Fault input is asserted.

### 16.1.1 PWM FAULTS AT RESET

During any Reset event, the PWMx module maintains ownership of the Class B Fault, FLT32. At Reset, this Fault is enabled in Latched mode to ensure the fail-safe power-up of the application. The application software must clear the PWM Fault before enabling the highspeed motor control PWMx module. To clear the Fault condition, the FLT32 pin must first be pulled low externally or the internal pull-down resistor in the CNPDx register can be enabled.

Note: The Fault mode may be changed using the FLTMOD<1:0> bits (FCLCON<1:0>), regardless of the state of FLT32.

#### 16.1.2 WRITE-PROTECTED REGISTERS

On dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices, write protection is implemented for the IOCONx and FCLCONx registers. The write protection feature prevents any inadvertent writes to these registers. This protection feature can be controlled by the PWMLOCK Configuration bit (FOSCSEL<6>). The default state of the write protection feature is enabled (PWMLOCK = 1). The write protection feature can be disabled by configuring, PWMLOCK = 0. To gain write access to these locked registers, the user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation. The write access to the IOCONx or FCLCONx registers must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. To write to both the IOCONx and FCLCONx registers requires two unlock operations.

The correct unlocking sequence is described in Example 16-1.

#### EXAMPLE 16-1: PWMx WRITE-PROTECTED REGISTER UNLOCK SEQUENCE

; FLT32 pin must be p	ulled low externally in order to clear and disable the fault
; Writing to FCLCON1 :	register requires unlock sequence
<pre>mov #0xabcd,w10 mov #0x4321,w11 mov #0x0000,w0 mov w10, PWMKEY mov w11, PWMKEY mov w0,FCLCON1</pre>	<pre>; Load first unlock key to w10 register ; Load second unlock key to w11 register ; Load desired value of FCLCON1 register in w0 ; Write first unlock key to PWMKEY register ; Write second unlock key to PWMKEY register ; Write desired value to FCLCON1 register</pre>
; Set PWM ownership as	nd polarity using the IOCON1 register
; Writing to IOCON1 re	egister requires unlock sequence
<pre>mov #0xabcd,w10 mov #0x4321,w11 mov #0xF000,w0 mov w10, PWMKEY mov w11, PWMKEY mov w0,IOCON1</pre>	<pre>; Load first unlock key to w10 register ; Load second unlock key to w11 register ; Load desired value of IOCON1 register in w0 ; Write first unlock key to PWMKEY register ; Write second unlock key to PWMKEY register ; Write desired value to IOCON1 register</pre>

#### REGISTER 16-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER<sup>(1)</sup>

- bit 7-3 FLTSRC<4:0>: Fault Control Signal Source Select for PWM Generator # bits 11111 = Fault 32 (default) 11110 = Reserved . . 01100 = Reserved 01011 = Comparator 4 01010 = Op Amp/Comparator 3
  - 01001 = Op Amp/Comparator 2
  - 01000 = Op Amp/Comparator 1
  - 00111 = Reserved
  - 00110 = Reserved
  - 00101 = Reserved
  - 00100 = Reserved
  - 00011 = Fault 4
  - 00010 = Fault 3
  - 00001 = Fault 2 00000 = Fault 1
- bit 2 ELTROL Fault Delarity for DWM Concrete

# bit 2 **FLTPOL:** Fault Polarity for PWM Generator # bit<sup>(2)</sup>

- 1 = The selected Fault source is active-low
- 0 = The selected Fault source is active-high
- bit 1-0 FLTMOD<1:0>: Fault Mode for PWM Generator # bits
  - 11 = Fault input is disabled
  - 10 = Reserved
  - 01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (cycle)
  - 00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (latched condition)
- **Note 1:** If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.
  - **2:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

### 23.2 ADC Helpful Tips

- 1. The SMPIx control bits in the AD1CON2 register:
  - a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
  - b) When the CSCNA bit in the AD1CON2 registers is set to '1', this determines when the ADC analog scan channel list, defined in the AD1CSSL/AD1CSSH registers, starts over from the beginning.
  - c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
  - d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA.
- 2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMPIx bits and the condition described in 1c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
- 3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer (i.e., ADC1BUF0) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA Controller, before the next ADC conversion is complete to avoid overwriting the previous value.
- 4. The DONE bit (AD1CON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (AD1CON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.

5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for ANO, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUXA selections use AN0-AN2. Carefully study the ADC block diagram to determine the configuration that will best suit your application. Configuration examples are available in the "Analog-to-Digital Converter (ADC)" (DS70621) section in the "dsPIC33/ PIC24 Family Reference Manual".

### 23.3 ADC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

### 23.3.1 KEY RESOURCES

- "Analog-to-Digital Converter (ADC)" (DS70621) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

#### REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER (CONTINUED)

- bit 3-0 SELSRCA<3:0>: Mask A Input Select bits
  - 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved 0101 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H 0000 = PWM1L

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed, or an SFR register is read. In these cases, the execution takes multiple instruction cycles with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Note: For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157). For more information on instructions that take more than one instruction cycle to execute, refer to **"CPU"** (DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*, particularly the **"Instruction Flow Types"** section.

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{}	Optional field or operation
$a\in\{b,c,d\}$	a is selected from the set of values b, c, d
<n:m></n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator write back destination address register $\in$ {W13, [W13]+ = 2}
bit4	4-bit bit selection field (used in word addressed instructions) $\in \{015\}$
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0x00000x1FFF}
lit1	1-bit unsigned literal $\in \{0,1\}$
lit4	4-bit unsigned literal ∈ {015}
lit5	5-bit unsigned literal $\in \{031\}$
lit8	8-bit unsigned literal $\in$ {0255}
lit10	10-bit unsigned literal $\in$ {0255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal $\in \{016384\}$
lit16	16-bit unsigned literal $\in \{065535\}$
lit23	23-bit unsigned literal $\in$ {08388608}; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal $\in$ {-512511}
Slit16	16-bit signed literal ∈ {-3276832767}
Slit6	6-bit signed literal $\in$ {-1616}
Wb	Base W register ∈ {W0W15}
Wd	Destination W register $\in$ { Wd, [Wd], [Wd++], [Wd], [++Wd], [Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd], [++Wnd], [Wnd], [Wnd+Wb] }

#### TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS



#### FIGURE 30-29: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X



#### FIGURE 30-36: ADC CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)

### 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	MILLIMETERS			
Dimension	l Limits	MIN	NOM	MAX
Number of Pins	Ν		28	
Pitch	е		1.27 BSC	
Overall Height	Α	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	С	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

#### Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2



#### 48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing C04-153A Sheet 1 of 2

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN] With 0.40 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	N	<b>ILLIMETER</b>	S	
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Optional Center Pad Width	W2			4.45
Optional Center Pad Length	T2			4.45
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A

## Revision E (April 2012)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

TABLE A-4:	MAJOR SECTION UPDATES
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Section Name	Update Description					
"16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High- Speed PWM, Op amps, and Advanced Analog"	The following 512-Kbyte devices were added to the General Purpose Families table (see Table 1): PIC24EP512GP202 PIC24EP512GP204 PIC24EP512GP206 dsPIC33EP512GP502 dsPIC33EP512GP506 The following 512-Kbyte devices were added to the Motor Control Families table (see Table 2): PIC24EP512MC202 PIC24EP512MC204 PIC24EP512MC206 dsPIC33EP512MC202 dsPIC33EP512MC202 dsPIC33EP512MC204 dsPIC33EP512MC204 dsPIC33EP512MC206 dsPIC33EP512MC206 dsPIC33EP512MC506					
Section 4.0 "Memory Organization"	Added a Program Memory Map for the new 512-Kbyte devices (see Figure 4-4). Added a Data Memory Map for the new dsPIC 512-Kbyte devices (see Figure 4-11). Added a Data Memory Map for the new PIC24 512-Kbyte devices (see Figure 4-16).					
Section 7.0 "Interrupt Controller"	Updated the VECNUM bits in the INTTREG register (see Register 7-7).					
Section 11.0 "I/O Ports"	Added tip 6 to Section 11.5 "I/O Helpful Tips".					
Section 27.0 "Special Features"	<ul> <li>The following modifications were made to the Configuration Byte Register Map (see Table 27-1):</li> <li>Added the column Device Memory Size (Kbytes)</li> <li>Removed Notes 1 through 4</li> <li>Added addresses for the new 512-Kbyte devices</li> </ul>					
Section 30.0 "Electrical Characteristics"	Updated the Minimum value for Parameter DC10 (see Table 30-4). Added Power-Down Current (Ipd) parameters for the new 512-Kbyte devices (see Table 30-8). Updated the Minimum value for Parameter CM34 (see Table 30-53). Updated the Minimum and Maximum values and the Conditions for parameter SY12 (see Table 30-22).					

## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

ECAN Module	
Control Registers	
Modes of Operation	
Overview	
Resources	
Electrical Characteristics	401
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