What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc503-h-tl

1.0   DEVICE OVERVIEW

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com)
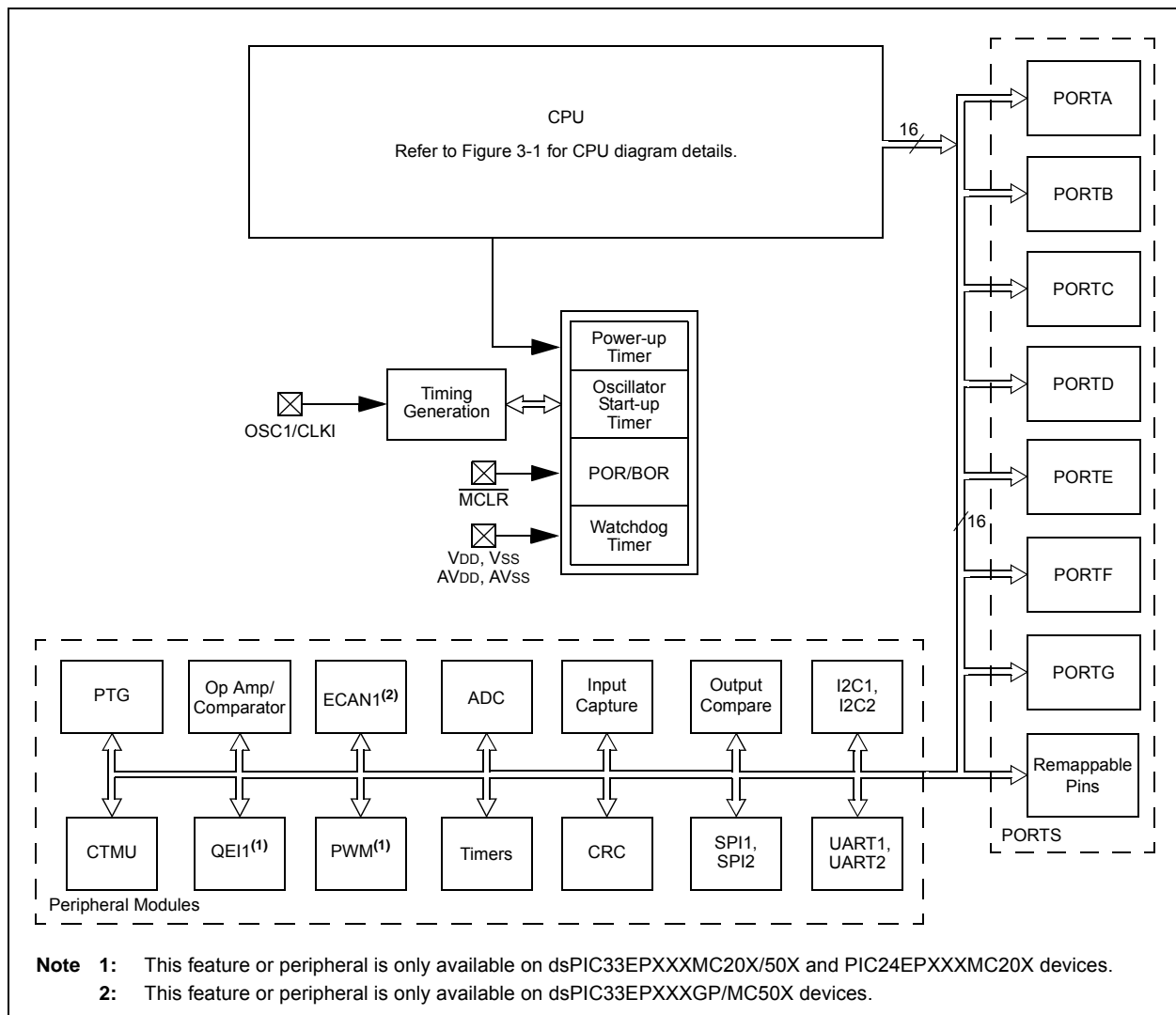>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1:   **dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X BLOCK DIAGRAM**

Note   1:   This feature or peripheral is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.
2:    This feature or peripheral is only available on dsPIC33EPXXXGP/MC50X devices.

REGISTER 3-2: **CORCON: CORE CONTROL REGISTER**

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1[1]	US0[1]	EDT[1,2]	DL2[1]	DL1[1]	DL0[1]
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA[1]	SATB[1]	SATDW[1]	ACCSAT[1]	IPL3[3]	SFA	RND[1]	IF[1]
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing latency is enabled
0 = Fixed exception processing latency is enabled

bit 14 **Unimplemented:** Read as '0'

bit 13-12 **US<1:0>:** DSP Multiply Unsigned/Signed Control bits[1]
11 = Reserved
10 = DSP engine multiplies are mixed-sign
01 = DSP engine multiplies are unsigned
00 = DSP engine multiplies are signed

bit 11 **EDT:** Early DO Loop Termination Control bit[1,2]
1 = Terminates executing DO loop at end of current loop iteration
0 = No effect

bit 10-8 **DL<2:0>:** DO Loop Nesting Level Status bits[1]
111 = 7 DO loops are active
•
•
•
001 = 1 DO loop is active
000 = 0 DO loops are active

bit 7 **SATA:** ACCA Saturation Enable bit[1]
1 = Accumulator A saturation is enabled
0 = Accumulator A saturation is disabled

bit 6 **SATB:** ACCB Saturation Enable bit[1]
1 = Accumulator B saturation is enabled
0 = Accumulator B saturation is disabled

bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit[1]
1 = Data Space write saturation is enabled
0 = Data Space write saturation is disabled

bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit[1]
1 = 9.31 saturation (super saturation)
0 = 1.31 saturation (normal saturation)

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3[3]
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.
2: This bit is always read as '0'.
3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

FIGURE 4-4: **PROGRAM MEMORY MAP FOR dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X AND PIC24EP256GP/MC20X DEVICES**

GOTO Instruction	0x000000
Reset Address	0x000002
Interrupt Vector Table	0x000004
	0x0001FE
	0x000200
User Program Flash Memory (88K instructions)	
	0x02AFEA
Flash Configuration Bytes	0x02AFEC
	0x02AFFE
	0x02B000
Unimplemented (Read '0's)	
	0x7FFFFE
	0x800000
Reserved	
	0x800FF6
	0x800FF8
USERID	
	0x800FFE
	0x801000
Reserved	
	0xF9FFFE
	0xFA0000
Write Latches	0xFA0002
	0xFA0004
Reserved	
	0xFEFFFE
	0xFF0000
DEVID	0xFF0002
	0xFF0004
Reserved	
	0xFFFFFE

User Memory Space

Configuration Memory Space

Note: Memory areas are not shown to scale.

TABLE 4-8: TIMER1 THROUGH TIMER5 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register																xxxx
PR1	0102	Period Register 1																FFFF
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		—	TSYNC	TCS	—	0000
TMR2	0106	Timer2 Register																xxxx
TMR3HLD	0108	Timer3 Holding Register (for 32-bit timer operations only)																xxxx
TMR3	010A	Timer3 Register																xxxx
PR2	010C	Period Register 2																FFFF
PR3	010E	Period Register 3																FFFF
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		T32	—	TCS	—	0000
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		—	—	TCS	—	0000
TMR4	0114	Timer4 Register																xxxx
TMR5HLD	0116	Timer5 Holding Register (for 32-bit operations only)																xxxx
TMR5	0118	Timer5 Register																xxxx
PR4	011A	Period Register 4																FFFF
PR5	011C	Period Register 5																FFFF
T4CON	011E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		T32	—	TCS	—	0000
T5CON	0120	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		—	—	TCS	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-34: NVM REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0728	WR	WREN	WRERR	NVMSIDL	—	—	—	—	—	—	—	—	NVMOP<3:0>				0000
NVMADRL	072A	NVMADR<15:0>																0000
NVMADRH	072C	—	—	—	—	—	—	—	—	NVMADR<23:16>								0000
NVMKEY	072E	—	—	—	—	—	—	—	—	NVMKEY<7:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-35: SYSTEM CONTROL REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	—	—	VREGSF	—	CM	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	Note 1
OSCCON	0742	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	IOLOCK	LOCK	—	CF	—	—	OSWEN	Note 2
CLKDIV	0744	ROI	DOZE<2:0>			DOZEN	FRCDIV<2:0>			PLLPOST<1:0>		—	PLLPRE<4:0>					0030
PLLFBD	0746	—	—	—	—	—	—	—	PLLDIV<8:0>									0030
OSCTUN	0748	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000

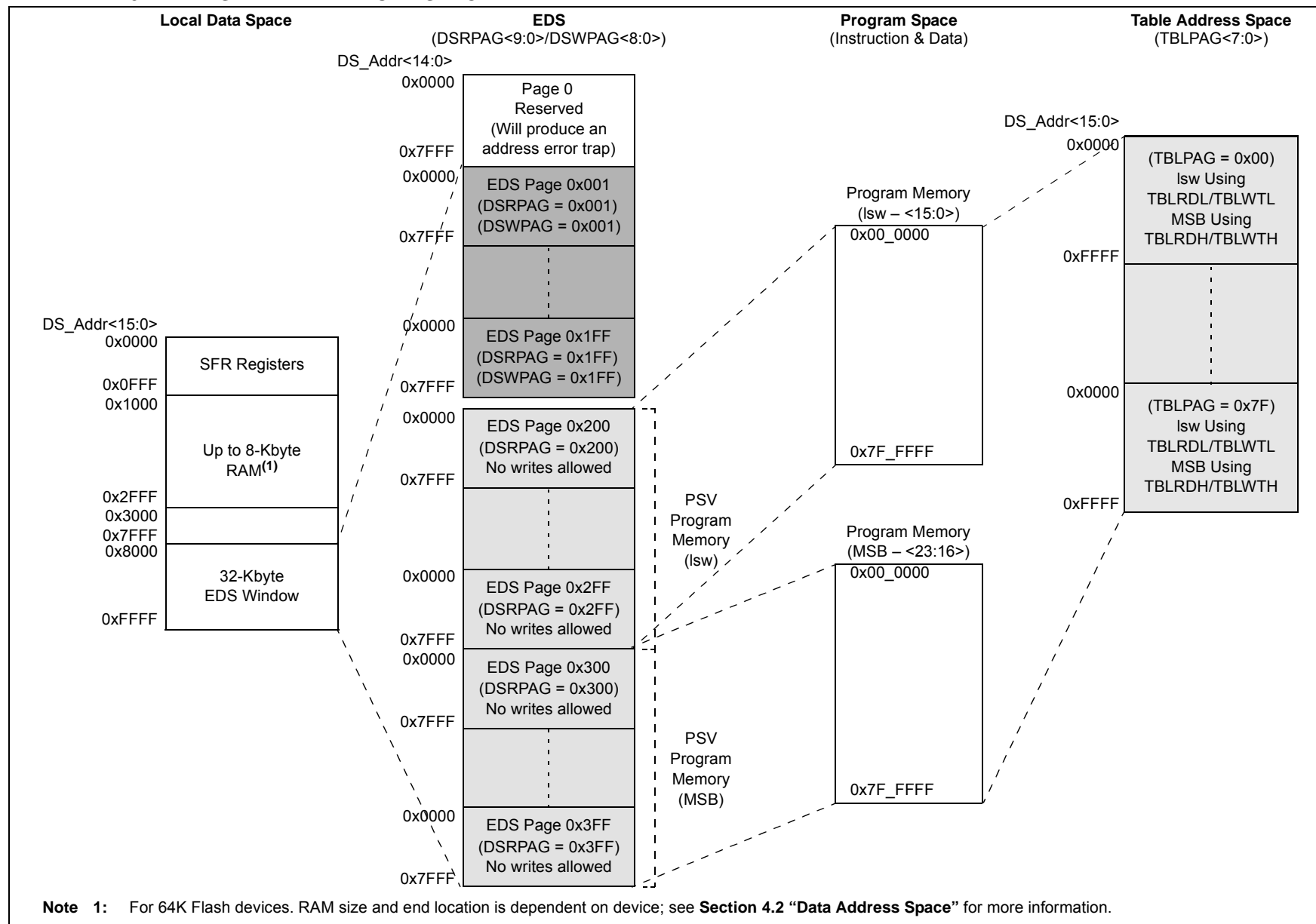**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: RCON register Reset values are dependent on the type of Reset.
2: OSCCON register Reset values are dependent on the Configuration Fuses.

TABLE 4-36: REFERENCE CLOCK REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
REFOCON	074E	ROON	—	ROSSLP	ROSEL	RODIV<3:0>				—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

EXAMPLE 4-3: **PAGED DATA MEMORY SPACE**

Local Data Space	EDS (DSRPAG<9:0>/DSWPAG<8:0>)	Program Space (Instruction & Data)	Table Address Space (TBLPAG<7:0>)

DS_Addr<14:0>

0x0000
Page 0
Reserved
(Will produce an address error trap)
0x7FFF

DS_Addr<15:0>

0x0000
EDS Page 0x001
(DSRPAG = 0x001)
(DSWPAG = 0x001)
0x7FFF

0x0000
EDS Page 0x1FF
(DSRPAG = 0x1FF)
(DSWPAG = 0x1FF)
0x7FFF

DS_Addr<15:0>
0x0000
SFR Registers
0x0FFF
0x1000
Up to 8-Kbyte RAM**(1)**
0x2FFF
0x3000
0x7FFF
0x8000
32-Kbyte EDS Window
0xFFFF

0x0000
EDS Page 0x200
(DSRPAG = 0x200)
No writes allowed
0x7FFF

0x0000
EDS Page 0x2FF
(DSRPAG = 0x2FF)
No writes allowed
0x7FFF

0x0000
EDS Page 0x300
(DSRPAG = 0x300)
No writes allowed
0x7FFF

0x0000
EDS Page 0x3FF
(DSRPAG = 0x3FF)
No writes allowed
0x7FFF

PSV Program Memory (lsw)

PSV Program Memory (MSB)

Program Memory (lsw – <15:0>)
0x00_0000
0x7F_FFFF

Program Memory (MSB – <23:16>)
0x00_0000
0x7F_FFFF

DS_Addr<15:0>
0x0000
(TBLPAG = 0x00)
lsw Using TBLRDL/TBLWTL
MSB Using TBLRDH/TBLWTH
0xFFFF

0x0000
(TBLPAG = 0x7F)
lsw Using TBLRDL/TBLWTL
MSB Using TBLRDH/TBLWTH
0xFFFF

Note 1: For 64K Flash devices. RAM size and end location is dependent on device; see **Section 4.2 "Data Address Space"** for more information.

4.8 Interfacing Program and Data Memory Spaces

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture uses a 24-bit-wide Program Space (PS) and a 16-bit-wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the architecture of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices provides two methods by which Program Space can be accessed during operation:

• Using table instructions to access individual bytes or words anywhere in the Program Space
• Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

TABLE 4-65:   PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		<23>	**<22:16>**	**<15>**	**<14:1>**	**<0>**
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xx xxxx xxxx xxxx xxxx xxx0				
`TBLRD/TBLWT` (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx xxxx xxxx xxxx xxxx xxxx				
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		1xxx xxxx xxxx xxxx xxxx xxxx				

FIGURE 4-22:   DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION

Note 1: The Least Significant bit (LSb) of Program Space addresses is always fixed as '0' to maintain word alignment of data in the Program and Data Spaces.
2: Table operations are not required to be word-aligned. Table Read operations are permitted in the configuration memory space.
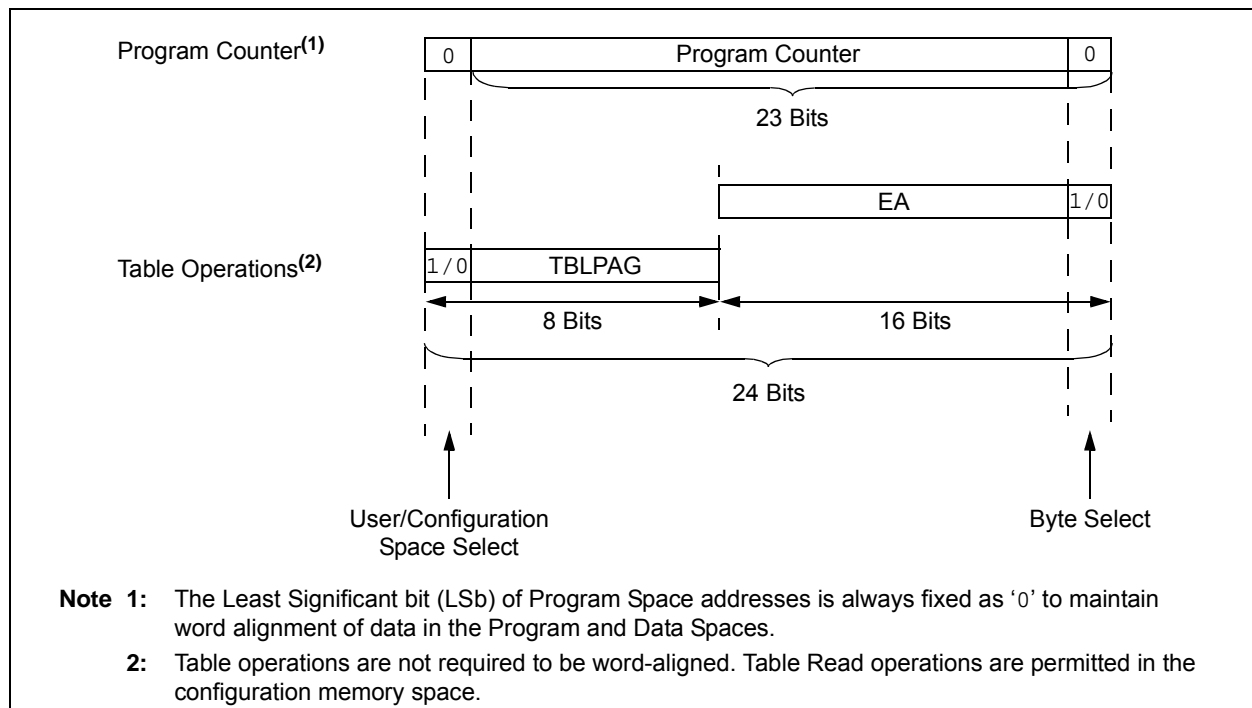
7.0 INTERRUPT CONTROLLER

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Interrupts"** (DS70600) in the "*dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X CPU.

The interrupt controller has the following features:

- Up to eight processor exceptions and software traps
- Eight user-selectable priority levels
- Interrupt Vector Table (IVT) with a unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X Interrupt Vector Table (IVT), shown in Figure 7-1, resides in program memory starting at location, 000004h. The IVT contains seven non-maskable trap vectors and up to 246 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit-wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

> **Note:** Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

REGISTER 9-3: **PLLFBD: PLL FEEDBACK DIVISOR REGISTER**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PLLDIV8
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
PLLDIV7	PLLDIV6	PLLDIV5	PLLDIV4	PLLDIV3	PLLDIV2	PLLDIV1	PLLDIV0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8-0 **PLLDIV<8:0>:** PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)

111111111 = 513

•

•

•

000110000 = 50 (default)

•

•

•

000000010 = 4

000000001 = 3

000000000 = 2

11.5   I/O Helpful Tips

1. In some cases, certain pins, as defined in Table 30-11, under "Injection Current", have internal protection diodes to VDD and VSS. The term, "Injection Current", is also referred to as "Clamp Current". On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the VSS and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device, that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.

2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '0', regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a '0'.

> **Note:** Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.

4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(VDD – 0.8), not VDD. This value is still above the minimum VIH of CMOS and TTL devices.

5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specification. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH, and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of this data sheet. For example:

    VOH = 2.4V @ IOH = -8 mA and VDD = 3.3V

    The maximum output current sourced by any 8 mA I/O pin = 12 mA.

    LED source current < 12 mA is technically permitted. Refer to the VOH/IOH graphs in **Section 30.0 "Electrical Characteristics"** for additional information.

6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:

    a) Only one "output" function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).

    b) It is possible to assign a "remappable output" function to multiple pins and externally short or tie them together for increased current drive.

    c) If any "dedicated output" function is enabled on a pin, it will take precedence over any remappable "output" function.

    d) If any "dedicated digital" (input or output) function is enabled on a pin, any number of "input" remappable functions can be mapped to the same pin.

    e) If any "dedicated analog" function(s) are enabled on a given pin, "digital input(s)" of any kind will all be disabled, although a single "digital output", at the user's cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input provided there is no external analog input, such as for a built-in self-test.

    f) Any number of "input" remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable "output".

REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INT2R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7   **Unimplemented:** Read as '0'

bit 6-0   **INT2R<6:0>:** Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2CKR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7   **Unimplemented:** Read as '0'

bit 6-0   **T2CKR<6:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits
(see Table 11-2 for input pin selection numbers)
1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

13.0   TIMER2/3 AND TIMER4/5

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (DS70362) of the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (32-bit timer pairs, and Timer3 and Timer5 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, and T4CON, T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. T3CON and T5CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw); Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

> **Note:** For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

> **Note:** Only Timer2, 3, 4 and 5 can trigger a DMA data transfer.

REGISTER 16-13: IOCONx: PWMx I/O CONTROL REGISTER[2] (CONTINUED)

bit 1   **SWAP:** SWAP PWMxH and PWMxL Pins bit

1 = PWMxH output signal is connected to PWMxL pins; PWMxL output signal is connected to PWMxH pins
0 = PWMxH and PWMxL pins are mapped to their respective pins

bit 0   **OSYNC:** Output Override Synchronization bit

1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWMx period boundary
0 = Output overrides via the OVDDAT<1:0> bits occur on the next CPU clock boundary

Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).

2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

REGISTER 21-15: CxBUFPNT4: ECANx FILTER 12-15 BUFFER POINTER REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15BP<3:0>				F14BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F13BP<3:0>				F12BP<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12   **F15BP<3:0>:** RX Buffer Mask for Filter 15 bits
     1111 = Filter hits received in RX FIFO buffer
     1110 = Filter hits received in RX Buffer 14
     •
     •
     •
     0001 = Filter hits received in RX Buffer 1
     0000 = Filter hits received in RX Buffer 0

bit 11-8   **F14BP<3:0>:** RX Buffer Mask for Filter 14 bits (same values as bits<15:12>)

bit 7-4   **F13BP<3:0>:** RX Buffer Mask for Filter 13 bits (same values as bits<15:12>)

bit 3-0   **F12BP<3:0>:** RX Buffer Mask for Filter 12 bits (same values as bits<15:12>)

REGISTER 24-12: PTGQPTR: PTG STEP QUEUE POINTER REGISTER[1]

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	PTGQPTR<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **PTGQPTR<4:0>:** PTG Step Queue Pointer Register bits
This register points to the currently active Step command in the Step queue.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-13: PTGQUEx: PTG STEP QUEUE REGISTER x (x = 0-7)[1,3]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP(2x + 1)<7:0>[2]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP(2x)<7:0>[2]							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **STEP(2x + 1)<7:0>:** PTG Step Queue Pointer Register bits[2]
A queue location for storage of the STEP(2x + 1) command byte.

bit 7-0 **STEP(2x)<7:0>:** PTG Step Queue Pointer Register bits[2]
A queue location for storage of the STEP(2x) command byte.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).
2: Refer to Table 24-1 for the Step command encoding.
3: The Step registers maintain their values on any type of Reset.

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed, or an SFR register is read. In these cases, the execution takes multiple instruction cycles with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

> **Note:** For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).
>
> For more information on instructions that take more than one instruction cycle to execute, refer to **"CPU"** (DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*, particularly the **"Instruction Flow Types"** section.

TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
a ∈ {b, c, d}	a is selected from the set of values b, c, d
<n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator write back destination address register ∈ {W13, [W13]+ = 2}
bit4	4-bit bit selection field (used in word addressed instructions) ∈ {0...15}
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0x0000...0x1FFF}
lit1	1-bit unsigned literal ∈ {0,1}
lit4	4-bit unsigned literal ∈ {0...15}
lit5	5-bit unsigned literal ∈ {0...31}
lit8	8-bit unsigned literal ∈ {0...255}
lit10	10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal ∈ {0...16384}
lit16	16-bit unsigned literal ∈ {0...65535}
lit23	23-bit unsigned literal ∈ {0...8388608}; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512...511}
Slit16	16-bit signed literal ∈ {-32768...32767}
Slit6	6-bit signed literal ∈ {-16...16}
Wb	Base W register ∈ {W0...W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] }

30.0   ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings[(1)]

Ambient temperature under bias..-40°C to +125°C
Storage temperature .... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} .... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to V_{SS}[(3)]... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 3.0V$[(3)].................................... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} < 3.0V$[(3)].................................... -0.3V to +3.6V
Maximum current out of V_{SS} pin ....300 mA
Maximum current into V_{DD} pin[(2)]...300 mA
Maximum current sunk/sourced by any 4x I/O pin ....15 mA
Maximum current sunk/sourced by any 8x I/O pin ....25 mA
Maximum current sunk by all ports[(2,4)] ....200 mA

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

   2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

   3: See the **"Pin Diagrams"** section for the 5V tolerant pins.

   4: Exceptions are: dsPIC33EPXXXGP502, dsPIC33EPXXXMC202/502 and PIC24EPXXXGP/MC202 devices, which have a maximum sink/source capability of 130 mA.

FIGURE 30-6:   **INPUT CAPTURE x (ICx) TIMING CHARACTERISTICS**

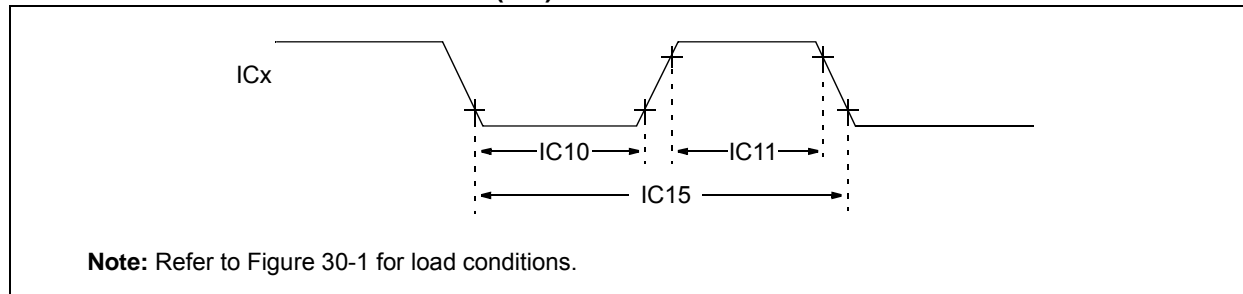**Note:** Refer to Figure 30-1 for load conditions.

TABLE 30-26:   INPUT CAPTURE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics[1]	Min.	Max.	Units	Conditions	
IC10	TccL	ICx Input Low Time	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	—	ns	Must also meet Parameter IC15	N = prescale value (1, 4, 16)
IC11	TccH	ICx Input High Time	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	—	ns	Must also meet Parameter IC15	
IC15	TccP	ICx Input Period	Greater of 25 + 50 or (1 Tcy/N) + 50	—	ns		

Note 1:   These parameters are characterized, but not tested in manufacturing.

NOTES:

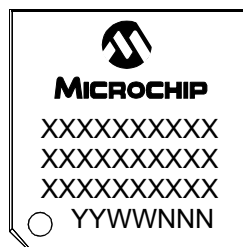## 33.1 Package Marking Information (Continued)

48-Lead UQFN (6x6x0.5 mm)

Example

```
       ☒
XXXXXXXXXX
XXXXXXXXXX
XXXXXXXXXX
    YYWWNNN
```

```
       ☒
33EP64GP
504-I/MV (e3)
1310017
```

64-Lead QFN (9x9x0.9 mm)

Example

```
       ☒
XXXXXXXXXX
XXXXXXXXXX
XXXXXXXXXX
    YYWWNNN
```

```
       ☒
dsPIC33EP
64GP506
-I/MR (e3)
    1310017
```

64-Lead TQFP (10x10x1 mm)

Example

```
       ☒
    MICROCHIP
XXXXXXXXXX
XXXXXXXXXX
XXXXXXXXXX
○  YYWWNNN
```

```
       ☒
    MICROCHIP
dsPIC33EP
64GP506
-I/PT (e3)
○    1310017
```