

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc503t-e-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES

		<u>~</u>				Re	mappa	ble P	eriphe	erals											
Device	Page Erase Size (Instructions)	Program Flash Memory (Kbyte	RAM (Kbytes)	16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM ⁽⁴⁾ (Channels)	Quadrature Encoder Interface	UART	SPI ⁽²⁾	ECAN™ Technology	External Interrupts ⁽³⁾	I²C™	CRC Generator	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	СТМИ	PTG	l/O Pins	Pins	Packages
PIC24EP32MC202	512	32	4																		
PIC24EP64MC202	1024	64	8																		SPDIP,
PIC24EP128MC202	1024	128	16	5	4	4	6	1	2	2	_	3	2	1	6	2/3 ⁽¹⁾	Yes	Yes	21	28	SOIC,
PIC24EP256MC202	1024	256	32																		QFN-S
PIC24EP512MC202	1024	512	48																		
PIC24EP32MC203	512	32	4	-			_	4	0	0		0	0	4	•	2/4	V	Vee	05	20	
PIC24EP64MC203	1024	64	8	5	4	4	ю	1	2	2	_	3	2	1	8	3/4	res	res	25	30	VILA
PIC24EP32MC204	512	32	4																		
PIC24EP64MC204	1024	64	8																		VTLA ⁽⁵⁾ ,
PIC24EP128MC204	1024	128	16	5	4	4	6	1	2	2	_	3	2	1	9	3/4	Yes	Yes	35	44/	TQFP,
PIC24EP256MC204	1024	256	32																	40	UQFN
PIC24EP512MC204	1024	512	48																		
PIC24EP64MC206	1024	64	8																		
PIC24EP128MC206	1024	128	16	_					-			•									TQFP.
PIC24EP256MC206	1024	256	32	5	4	4	6	1	2	2	_	3	2	1	16	3/4	res	res	53	64	QFN
PIC24EP512MC206	1024	512	48																		
dsPIC33EP32MC202	512	32	4																		
dsPIC33EP64MC202	1024	64	8																		SPDIP,
dsPIC33EP128MC202	1024	128	16	5	4	4	6	1	2	2	_	3	2	1	6	2/3(1)	Yes	Yes	21	28	SOIC,
dsPIC33EP256MC202	1024	256	32																		QFN-S
dsPIC33EP512MC202	1024	512	48																		
dsPIC33EP32MC203	512	32	4	_		_			-	_		-	-		-						
dsPIC33EP64MC203	1024	64	8	5	4	4	6	1	2	2	—	3	2	1	8	3/4	Yes	Yes	25	36	VTLA
dsPIC33EP32MC204	512	32	4																		
dsPIC33EP64MC204	1024	64	8																		VTLA ⁽⁵⁾ ,
dsPIC33EP128MC204	1024	128	16	5	4	4	6	1	2	2	_	3	2	1	9	3/4	Yes	Yes	35	44/	TQFP,
dsPIC33EP256MC204	1024	256	32																	40	UQFN,
dsPIC33EP512MC204	1024	512	48																		
dsPIC33EP64MC206	1024	64	8																		
dsPIC33EP128MC206	1024	128	16	_					-			-	-								TOFP
dsPIC33EP256MC206	1024	256	32	5	4	4	6	1	2	2	—	3	2	1	16	3/4	Yes	Yes	53	64	QFN
dsPIC33EP512MC206	1024	512	48																		
dsPIC33EP32MC502	512	32	4																		
dsPIC33EP64MC502	1024	64	8																		SPDIP,
dsPIC33EP128MC502	1024	128	16	5	4	4	6	1	2	2	1	3	2	1	6	2/3(1)	Yes	Yes	21	28	SOIC,
dsPIC33EP256MC502	1024	256	32																		QFN-S
dsPIC33EP512MC502	1024	512	48																		_
dsPIC33EP32MC503	512	32	4	_		l .	6		_	-		-	-		_			~	a-		
dsPIC33EP64MC503	1024	64	8	5	4	4	6	1	2	2	1	3	2	1	8	3/4	res	res	25	36	VILA

Note 1: On 28-pin devices, Comparator 4 does not have external connections. Refer to Section 25.0 "Op Amp/Comparator Module" for details. 2: Only SPI2 is remappable.

3: INTO is not remappable.

4: Only the PWM Faults are remappable.

5: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

FIGURE 2-7: INTERLEAVED PFC





dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER	(10-2: PMD	2: PERIPHER		DISABLE C	UNIKOL RE	GISTER 2	
U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
_	—	—	_	IC4MD	IC3MD	IC2MD	IC1MD
bit 15							bit 8
U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
_			_	OC4MD	OC3MD	OC2MD	OC1MD
bit 7							bit 0
Legend:							
R = Readab	ole bit	W = Writable b	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	iown
hit 15-12	Unimpleme	nted: Read as '(,'				
bit 11		It Capture 4 Mod	, Iula Disabla bi	+			
	1 = Input Ca	nture 4 module i	s disabled	L .			
	0 = Input Ca	pture 4 module i	s enabled				
bit 10	IC3MD: Inpu	It Capture 3 Mod	ule Disable bi	t			
	1 = Input Ca	, pture 3 module i	s disabled				
	0 = Input Ca	pture 3 module i	s enabled				
bit 9	IC2MD: Inpu	it Capture 2 Mod	ule Disable bi	t			
	1 = Input Ca	pture 2 module i	s disabled				
hit 0		plure 2 mouule i					
DILO		nturo 1 modulo i	ule Disable bi	L			
	0 = Input Ca	pture 1 module i pture 1 module i	s enabled				
bit 7-4	Unimpleme	nted: Read as '0)'				
bit 3	OC4MD: Ou	tput Compare 4	Module Disab	le bit			
	1 = Output C	 Compare 4 modu	le is disabled				
	0 = Output C	ompare 4 modu	le is enabled				
bit 2	OC3MD: Ou	tput Compare 3	Module Disab	le bit			
	1 = Output C	ompare 3 modu	le is disabled				
	0 = Output C	compare 3 modu	le is enabled				
bit 1	OC2MD: Ou	tput Compare 2	Module Disab	le bit			
	1 = Output C	Compare 2 modu	le is disabled				
h:+ 0		ompare 2 modu	le is enabled Medule Disch				
		ipui Compare 1					
	$\perp = Output C$ 0 = Output C	Compare 1 modu	le is usabled				

~

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1 (CONTINUED)

- bit 3 TRIGMODE: Trigger Status Mode Select bit
 - 1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software
 - 0 = TRIGSTAT is cleared only by software
- bit 2-0 OCM<2:0>: Output Compare x Mode Select bits
 - 111 = Center-Aligned PWM mode: Output set high when OCxTMR = OCxR and set low when OCxTMR = OCxRS⁽¹⁾
 - 110 = Edge-Aligned PWM mode: Output set high when OCxTMR = 0 and set low when OCxTMR = OCxR⁽¹⁾
 - 101 = Double Compare Continuous Pulse mode: Initializes OCx pin low, toggles OCx state continuously on alternate matches of OCxR and OCxRS
 - 100 = Double Compare Single-Shot mode: Initializes OCx pin low, toggles OCx state on matches of OCxR and OCxRS for one cycle
 - 011 = Single Compare mode: Compare event with OCxR, continuously toggles OCx pin
 - 010 = Single Compare Single-Shot mode: Initializes OCx pin high, compare event with OCxR, forces OCx pin low
 - 001 = Single Compare Single-Shot mode: Initializes OCx pin low, compare event with OCxR, forces OCx pin high
 - 000 = Output compare channel is disabled
- Note 1: OCxR and OCxRS are double-buffered in PWM mode only.
 - 2: Each Output Compare x module (OCx) has one PTG clock source. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.
 - PTGO4 = OC1 PTGO5 = OC2
 - PTGO6 = OC3 PTGO7 = OC4

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 16-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	x<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PDC	x<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	id as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 **PDCx<15:0>:** PWMx Generator # Duty Cycle Value bits

REGISTER 16-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	Ex<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	SEx<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable b	it	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkı	nown

bit 15-0 PHASEx<15:0>: PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

Note 1: If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs

 If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER (CONTINUED)

- PTGITM<1:0>: PTG Input Trigger Command Operating Mode bits⁽¹⁾
 - 11 = Single level detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
 - 10 = Single level detect with Step delay executed on exit of command
 - 01 = Continuous edge detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
 - 00 = Continuous edge detect with Step delay executed on exit of command
- Note 1: These bits apply to the PTGWHI and PTGWLO commands only.

bit 1-0

- **2:** This bit is only used with the PTGCTRL step command software trigger option.
- **3:** Use of the PTG Single-Step mode is reserved for debugging tools only.

REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER (CONTINUED)

- bit 5 Unimplemented: Read as '0'
- bit 4 **CREF:** Comparator Reference Select bit (VIN+ input)⁽¹⁾
 - 1 = VIN+ input connects to internal CVREFIN voltage
 - 0 = VIN+ input connects to C4IN1+ pin
- bit 3-2 Unimplemented: Read as '0'
- bit 1-0 CCH<1:0>: Comparator Channel Select bits⁽¹⁾
 - 11 = VIN- input of comparator connects to OA3/AN6
 - 10 = VIN- input of comparator connects to OA2/AN0
 - 01 = VIN- input of comparator connects to OA1/AN3
 - 00 = VIN- input of comparator connects to C4IN1-
- Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.

DC CHARACTI	ERISTICS		Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended							
Parameter No.	Тур.	Max.	Units	Units Conditions						
Idle Current (III	dle) ⁽¹⁾									
DC40d	3	8	mA	-40°C						
DC40a	3	8	mA	+25°C	2 21/					
DC40b	3	8	mA	+85°C	5.5V	10 1011-5				
DC40c	3	8	mA	+125°C						
DC42d	6	12	mA	-40°C						
DC42a	6	12	mA	+25°C	3 3\/	20 MIPS				
DC42b	6	12	mA	+85°C	5.5 V	20 1011 3				
DC42c	6	12	mA	+125°C						
DC44d	11	18	mA	-40°C						
DC44a	11	18	mA	+25°C	3 3\/	40 MIPS				
DC44b	11	18	mA	+85°C	0.0 V	40 1011 0				
DC44c	11	18	mA	+125°C						
DC45d	17	27	mA	-40°C						
DC45a	17	27	mA	+25°C	3 3\/	60 MIRS				
DC45b	17	27	mA	+85°C	5.5 V	00 1011 3				
DC45c	17	27	mA	+125°C						
DC46d	20	35	mA	-40°C						
DC46a	20	35	mA	+25°C	3.3V	70 MIPS				
DC46b	20	35	mA	+85°C						

TABLE 30-7: DC CHARACTERISTICS: IDLE CURRENT (lidle)

Note 1: Base Idle current (IIDLE) is measured as follows:

• CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- · CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to Vss
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

DC CH	ARACTE	RISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$									
Param No.	Symbol	Characteristic	Min. Typ. Max. Units Conditions									
	VIL	Input Low Voltage										
DI10		Any I/O Pin and MCLR	Vss	—	0.2 VDD	V						
DI18		I/O Pins with SDAx, SCLx	Vss	_	0.3 VDD	V	SMBus disabled					
DI19		I/O Pins with SDAx, SCLx	Vss — 0.8 V SMBus enabled									
	Vih	Input High Voltage										
DI20		I/O Pins Not 5V Tolerant	0.8 VDD	—	Vdd	V	(Note 3)					
		I/O Pins 5V Tolerant and MCLR	0.8 VDD	—	5.5	V	(Note 3)					
		I/O Pins with SDAx, SCLx	0.8 VDD	—	5.5	V	SMBus disabled					
		I/O Pins with SDAx, SCLx	2.1	—	5.5	V	SMBus enabled					
	ICNPU	Change Notification Pull-up Current										
DI30			150	250	550	μA	VDD = 3.3V, VPIN = VSS					
	ICNPD	Change Notification Pull-Down Current ⁽⁴⁾										
DI31			20	50	100	μA	VDD = 3.3V, VPIN = VDD					

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 2: Negative current is defined as current sourced by the pin.
- 3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 4: VIL source < (Vss 0.3). Characterized but not tested.

5: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

- 6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

DC CHA	ARACTER	ISTICS	Standa (unless Operat	rd Oper s otherw ing temp	rating Co vise stat perature	ondition ed) -40°C -40°C	s: 3.0V to 3.6V ≤ TA ≤ +85°C for Industrial ≤ TA ≤ +125°C for Extended
Param.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
DO10	Vol	Output Low Voltage 4x Sink Driver Pins ⁽²⁾	_	—	0.4	V	VDD = 3.3V, $IOL \le 6 \text{ mA}, -40^{\circ}\text{C} \le Ta \le +85^{\circ}\text{C}$ $IOL \le 5 \text{ mA}, +85^{\circ}\text{C} < Ta \le +125^{\circ}\text{C}$
		Output Low Voltage 8x Sink Driver Pins ⁽³⁾		—	0.4	V	
DO20	Vон	Output High Voltage 4x Source Driver Pins ⁽²⁾	2.4	_	_	V	$IOH \ge -10 \text{ mA}, \text{ VDD} = 3.3 \text{ V}$
		Output High Voltage 8x Source Driver Pins ⁽³⁾	2.4	_	—	V	$IOH \ge -15 \text{ mA}, \text{ VDD} = 3.3 \text{ V}$
DO20A	Voн1	Output High Voltage	1.5 ⁽¹⁾	_		V	$IOH \ge -14 \text{ mA}, \text{ VDD} = 3.3 \text{V}$
		4x Source Driver Pins	2.0 ⁽¹⁾	_			$IOH \ge -12 \text{ mA}, \text{ VDD} = 3.3 \text{V}$
			3.0(1)	—	—		$IOH \ge -7 \text{ mA}, \text{ VDD} = 3.3 \text{V}$
		Output High Voltage	1.5 ⁽¹⁾	_		V	$IOH \ge -22 \text{ mA}, \text{ VDD} = 3.3 \text{V}$
		8x Source Driver Pins	2.0 ⁽¹⁾	—	_		$IOH \ge -18 \text{ mA}, \text{ VDD} = 3.3 \text{V}$
			3.0(1)	—	—		$IOH \ge -10 \text{ mA}, \text{ VDD} = 3.3 \text{V}$

TABLE 30-12: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

Note 1: Parameters are characterized but not tested.

2: Includes all I/O pins that are not 8x Sink Driver pins (see below).

Includes the following pins:
 For devices with less than 64 pins: RA3, RA4, RA9, RB<7:15> and RC3
 For 64-pin devices: RA4, RA9, RB<7:15>, RC3 and RC15

TABLE 30-13: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)}^{(1)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$						
Param No.	Symbol	Characteristic	Min. ⁽²⁾	Min. ⁽²⁾ Typ. Max.			Conditions		
BO10	VBOR	BOR Event on VDD Transition High-to-Low	2.65	_	2.95	V	VDD (Notes 2 and 3)		

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance.

2: Parameters are for design guidance only and are not tested in manufacturing.

3: The VBOR specification is relative to VDD.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

FIGURE 30-6: INPUT CAPTURE x (ICx) TIMING CHARACTERISTICS



TABLE 30-26: INPUT CAPTURE x MODULE TIMING REQUIREMENTS

АС СНА	RACTERI	STICS	Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le Ta \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le Ta \le +125^{\circ}C$ for Extended					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	ditions				
IC10	TccL	ICx Input Low Time	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	—	ns	Must also meet Parameter IC15		
IC11	ТссН	ICx Input High Time	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	—	ns	Must also meet Parameter IC15	N = prescale value (1, 4, 16)	
IC15	TccP	ICx Input Period	Greater of 25 + 50 or (1 Tcy/N) + 50	_	ns			

Note 1: These parameters are characterized, but not tested in manufacturing.



FIGURE 30-12: QEA/QEB INPUT CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

TABLE 30-31: QUADRATURE DECODER TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHAR	ACTERIS	TICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industria} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$						
Param No.	Symbol	Characteristic ⁽¹⁾	Тур. ⁽²⁾	Max.	Units	Conditions			
TQ30	TQUL	Quadrature Input Low Time	6 Tcy		ns				
TQ31	ΤουΗ	Quadrature Input High Time	6 Tcy	—	ns				
TQ35	ΤουΙΝ	Quadrature Input Period	12 Tcy	—	ns				
TQ36	TQUP	Quadrature Phase Period	3 TCY	—	ns				
TQ40	TQUFL	Filter Time to Recognize Low, with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)			
TQ41	TQUFH	Filter Time to Recognize High, with Digital Filter	3 * N * Tcy		ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)			

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: N = Index Channel Digital Filter Clock Divide Select bits. Refer to "Quadrature Encoder Interface (QEI)" (DS70601) in the "*dsPIC33/PIC24 Family Reference Manual*". Please see the Microchip web site for the latest family reference manual sections.





TABLE 30-34: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHA	RACTERIST	ICS	Standard (unless of Operating	d Operatin otherwise g tempera	ng Condi stated) ature -4 -4	tions: 3. $0^{\circ}C \le TA$ $0^{\circ}C \le TA$	0V to 3.6V ≤ +85°C for Industrial ≤ +125°C for Extended
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK2 Frequency	—	_	15	MHz	(Note 3)
SP20	TscF	SCK2 Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK2 Output Rise Time	—	—	_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	—	_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdiV2scH, TdiV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	_	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

TABLE 30-38:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param. Symbol Characteristic ⁽¹⁾			Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP70	FscP	Maximum SCK2 Input Frequency	_		Lesser of FP or 11	MHz	(Note 3)	
SP72	TscF	SCK2 Input Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCK2 Input Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO2 Data Output Fall Time	—			ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO2 Data Output Rise Time	—			ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_	_	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30			ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns		
SP50	TssL2scH, TssL2scL	SS2 ↓ to SCK2 ↑ or SCK2 ↓ Input	120	_	-	ns		
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	_	50	ns	(Note 4)	
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 TCY + 40	_	_	ns	(Note 4)	
SP60	TssL2doV	SDO2 Data Output Valid after SS2 Edge	—	_	50	ns		

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.



FIGURE 30-21: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

AC CHARA	CTERISTICS		$\label{eq:standard} \begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$					
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	СКР	SMP		
15 MHz	Table 30-42			0,1	0,1	0,1		
10 MHz	—	Table 30-43	—	1	0,1	1		
10 MHz	—	Table 30-44	—	0	0,1	1		
15 MHz	—	—	Table 30-45	1	0	0		
11 MHz	—	—	Table 30-46	1	1	0		
15 MHz	_	_	Table 30-47	0	1	0		
11 MHz	_	_	Table 30-48	0	0	0		

TABLE 30-41: SPI1 MAXIMUM DATA/CLOCK RATE SUMMARY

FIGURE 30-22: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS



AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated) ⁽¹⁾ Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param No.	Symbol	Characteristic	Min.	Typ. Max. Units Conditions			Conditions	
ADC Accuracy (10-Bit Mode)								
AD20b	Nr	Resolution	10 Data Bits		bits			
AD21b	INL	Integral Nonlinearity	-0.625		0.625	LSb	-40°C ≤ TA ≤ +85°C (Note 2)	
			-1.5	_	1.5	LSb	+85°C < TA ≤ +125°C (Note 2)	
AD22b	DNL	Differential Nonlinearity	-0.25	_	0.25	LSb	-40°C \leq TA \leq +85°C (Note 2)	
			-0.25		0.25	LSb	+85°C < TA \leq +125°C (Note 2)	
AD23b	Gerr	Gain Error	-2.5		2.5	LSb	-40°C \leq TA \leq +85°C (Note 2)	
			-2.5	_	2.5	LSb	+85°C < TA \leq +125°C (Note 2)	
AD24b	EOFF	Offset Error	-1.25		1.25	LSb	$-40^{\circ}C \le TA \le +85^{\circ}C \text{ (Note 2)}$	
			-1.25	_	1.25	LSb	+85°C < TA \leq +125°C (Note 2)	
AD25b	—	Monotonicity	_	_	_		Guaranteed	
Dynamic Performance (10-Bit Mode)								
AD30b	THD	Total Harmonic Distortion ⁽³⁾		64	—	dB		
AD31b	SINAD	Signal to Noise and Distortion ⁽³⁾	-	57	_	dB		
AD32b	SFDR	Spurious Free Dynamic Range ⁽³⁾	—	72	—	dB		
AD33b	Fnyq	Input Signal Bandwidth ⁽³⁾	_	550		kHz		
AD34b	ENOB	Effective Number of Bits ⁽³⁾	—	9.4	—	bits		

TABLE 30-59: ADC MODULE SPECIFICATIONS (10-BIT MODE)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

3: Parameters are characterized but not tested in manufacturing.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X



FIGURE 30-36: ADC CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)

64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS	3	
Dimensio	on Limits	MIN	NOM	MAX	
Number of Leads	Ν	64			
Lead Pitch	е	0.50 BSC			
Overall Height	А	_	-	1.20	
Molded Package Thickness	A2	0.95	1.00	1.05	
Standoff	A1	0.05	-	0.15	
Foot Length	L	0.45	0.60	0.75	
Footprint	L1	1.00 REF			
Foot Angle	φ	0° 3.5° 7°			
Overall Width	Е	12.00 BSC			
Overall Length	D	12.00 BSC			
Molded Package Width	E1	10.00 BSC			
Molded Package Length	D1	10.00 BSC			
Lead Thickness	С	0.09	-	0.20	
Lead Width	b	0.17	0.22	0.27	
Mold Draft Angle Top	α	11°	12°	13°	
Mold Draft Angle Bottom	β	11° 12° 13°			

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B

NOTES: