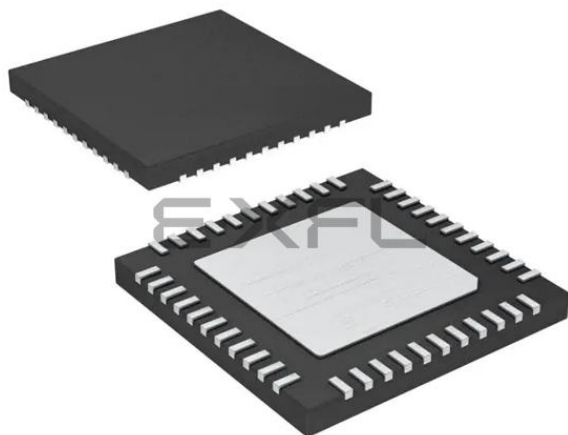




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc504-e-ml

TABLE 4-23: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
	0400-041E	See definition when WIN = x																	
C1BUFPNT1	0420	F3BP<3:0>				F2BP<3:0>				F1BP<3:0>				F0BP<3:0>				0000	
C1BUFPNT2	0422	F7BP<3:0>				F6BP<3:0>				F5BP<3:0>				F4BP<3:0>				0000	
C1BUFPNT3	0424	F11BP<3:0>				F10BP<3:0>				F9BP<3:0>				F8BP<3:0>				0000	
C1BUFPNT4	0426	F15BP<3:0>				F14BP<3:0>				F13BP<3:0>				F12BP<3:0>				0000	
C1RXM0SID	0430	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx	
C1RXM0EID	0432	EID<15:8>								EID<7:0>								xxxx	
C1RXM1SID	0434	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx	
C1RXM1EID	0436	EID<15:8>								EID<7:0>								xxxx	
C1RXM2SID	0438	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx	
C1RXM2EID	043A	EID<15:8>								EID<7:0>								xxxx	
C1RXF0SID	0440	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF0EID	0442	EID<15:8>								EID<7:0>								xxxx	
C1RXF1SID	0444	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF1EID	0446	EID<15:8>								EID<7:0>								xxxx	
C1RXF2SID	0448	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF2EID	044A	EID<15:8>								EID<7:0>								xxxx	
C1RXF3SID	044C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF3EID	044E	EID<15:8>								EID<7:0>								xxxx	
C1RXF4SID	0450	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF4EID	0452	EID<15:8>								EID<7:0>								xxxx	
C1RXF5SID	0454	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF5EID	0456	EID<15:8>								EID<7:0>								xxxx	
C1RXF6SID	0458	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF6EID	045A	EID<15:8>								EID<7:0>								xxxx	
C1RXF7SID	045C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF7EID	045E	EID<15:8>								EID<7:0>								xxxx	
C1RXF8SID	0460	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF8EID	0462	EID<15:8>								EID<7:0>								xxxx	
C1RXF9SID	0464	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF9EID	0466	EID<15:8>								EID<7:0>								xxxx	
C1RXF10SID	0468	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	
C1RXF10EID	046A	EID<15:8>								EID<7:0>								xxxx	
C1RXF11SID	046C	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-42: OP AMP/COMPARATOR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	0A80	PSIDL	—	—	—	C4EVT	C3EVT	C2EVT	C1EVT	—	—	—	—	C4OUT	C3OUT	C2OUT	C1OUT	0000
CVRCON	0A82	—	CVR2OE	—	—	—	VREFSEL	—	—	CVREN	CVR1OE	CVRR	CVRSS	CVR<3:0>				0000
CM1CON	0A84	CON	COE	CPOL	—	—	OPMODE	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM1MSKSRC	0A86	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM1MSKCON	0A88	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM1FLTR	0A8A	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CM2CON	0A8C	CON	COE	CPOL	—	—	OPMODE	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM2MSKSRC	0A8E	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM2MSKCON	0A90	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM2FLTR	0A92	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CM3CON ⁽¹⁾	0A94	CON	COE	CPOL	—	—	OPMODE	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM3MSKSRC ⁽¹⁾	0A96	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM3MSKCON ⁽¹⁾	0A98	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM3FLTR ⁽¹⁾	0A9A	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
CM4CON	0A9C	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
CM4MSKSRC	0A9E	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
CM4MSKCON	0AA0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM4FLTR	0AA2	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are unavailable on dsPIC33EPXXGP502/MC502/MC202 and PIC24EP256GP/MC202 (28-pin) devices.

TABLE 4-43: CTMU REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CTMUCON1	033A	CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	—	—	—	—	—	—	—	—	0000
CTMUCON2	033C	EDG1MOD	EDG1POL	EDG1SEL<3:0>				EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL<3:0>				—	—	0000
CTMUICON	033E	ITRIM<5:0>						IRNG<1:0>		—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-44: JTAG INTERFACE REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
JDATAH	0FF0	—	—	—	—	JDATAH<27:16>												xxxx
JDATAL	0FF2	JDATAL<15:0>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-49: PORTD REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	0E30	—	—	—	—	—	—	—	TRISD8	—	TRISD6	TRISD5	—	—	—	—	—	0160
PORTD	0E32	—	—	—	—	—	—	—	RD8	—	RD6	RD5	—	—	—	—	—	xxxx
LATD	0E34	—	—	—	—	—	—	—	LATD8	—	LATD6	LATD5	—	—	—	—	—	xxxx
ODCD	0E36	—	—	—	—	—	—	—	ODCD8	—	ODCD6	ODCD5	—	—	—	—	—	0000
CNEND	0E38	—	—	—	—	—	—	—	CNIED8	—	CNIED6	CNIED5	—	—	—	—	—	0000
CNPUD	0E3A	—	—	—	—	—	—	—	CNPUD8	—	CNPUD6	CNPUD5	—	—	—	—	—	0000
CNPDD	0E3C	—	—	—	—	—	—	—	CNPDD8	—	CNPDD6	CNPDD5	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-50: PORTE REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISE	0E40	TRISE15	TRISE14	TRISE13	TRISE12	—	—	—	—	—	—	—	—	—	—	—	—	F000
PORTE	0E42	RE15	RE14	RE13	RE12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
LATE	0E44	LATE15	LATE14	LATE13	LATE12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
ODCE	0E46	ODCE15	ODCE14	ODCE13	ODCE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNENE	0E48	CNIEE15	CNIEE14	CNIEE13	CNIEE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPUE	0E4A	CNPUE15	CNPUE14	CNPUE13	CNPUE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPDE	0E4C	CNPDE15	CNPDE14	CNPDE13	CNPDE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
ANSELE	0E4E	ANSE15	ANSE14	ANSE13	ANSE12	—	—	—	—	—	—	—	—	—	—	—	—	F000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-51: PORTF REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRISF1	TRISF0	0003
PORTF	0E52	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RF1	RF0	xxxx
LATF	0E54	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LATF1	LATF0	xxxx
ODCF	0E56	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODCF1	ODCF0	0000
CNENF	0E58	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNIEF1	CNIEF0	0000
CNPUF	0E5A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPUF1	CNPUF0	0000
CNPDF	0E5C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPDF1	CNPDF0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-52: PORTG REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	0E60	—	—	—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	—	—	03C0
PORTG	0E62	—	—	—	—	—	—	RG9	RG8	RG7	RG6	—	—	—	—	—	—	xxxx
LATG	0E64	—	—	—	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	—	—	xxxx
ODCG	0E66	—	—	—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	—	—	0000
CNENG	0E68	—	—	—	—	—	—	CNIEG9	CNIEG8	CNIEG7	CNIEG6	—	—	—	—	—	—	0000
CNPUG	0E6A	—	—	—	—	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	—	—	0000
CNPDG	0E6C	—	—	—	—	—	—	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

11.7 Peripheral Pin Select Registers

REGISTER 11-1: RPIR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INT1R<6:0>						
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **INT1R<6:0>:** Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	INT2R<6:0>							
bit 7								bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **INT2R<6:0>:** Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.
.
.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2CKR<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **T2CKR<6:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.
.
.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 17-13: QE11LECH: QE11 LESS THAN OR EQUAL COMPARE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **QEILEC<31:16>**: High Word Used to Form 32-Bit Less Than or Equal Compare Register (QE11LEC) bits**REGISTER 17-14: QE11LECL: QE11 LESS THAN OR EQUAL COMPARE LOW WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **QEILEC<15:0>**: Low Word Used to Form 32-Bit Less Than or Equal Compare Register (QE11LEC) bits

REGISTER 17-15: QE1GEC: QE1 GREATER THAN OR EQUAL COMPARE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIGEC<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIGEC<23:16>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **QEIGEC<31:16>**: High Word Used to Form 32-Bit Greater Than or Equal Compare Register (QE1GEC) bits

REGISTER 17-16: QE1GECL: QE1 GREATER THAN OR EQUAL COMPARE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIGEC<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIGEC<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **QEIGEC<15:0>**: Low Word Used to Form 32-Bit Greater Than or Equal Compare Register (QE1GEC) bits

REGISTER 21-11: CxFEN1: ECANx ACCEPTANCE FILTER ENABLE REGISTER 1

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **FLTEN<15:0>**: Enable Filter n to Accept Messages bits
1 = Enables Filter n
0 = Disables Filter n

REGISTER 21-12: CxBUFNT1: ECANx FILTER 0-3 BUFFER POINTER REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3BP<3:0>				F2BP<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F1BP<3:0>				F0BP<3:0>			
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **F3BP<3:0>**: RX Buffer Mask for Filter 3 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
.
.
.
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F2BP<3:0>**: RX Buffer Mask for Filter 2 bits (same values as bits<15:12>)

bit 7-4 **F1BP<3:0>**: RX Buffer Mask for Filter 1 bits (same values as bits<15:12>)

bit 3-0 **F0BP<3:0>**: RX Buffer Mask for Filter 0 bits (same values as bits<15:12>)

21.5 ECAN Message Buffers

ECAN Message Buffers are part of RAM memory. They are not ECAN Special Function Registers. The user application must directly write into the RAM area that is configured for ECAN Message Buffers. The location and size of the buffer area is defined by the user application.

BUFFER 21-1: ECAN™ MESSAGE BUFFER WORD 0

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	SID10	SID9	SID8	SID7	SID6
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID5	SID4	SID3	SID2	SID1	SID0	SRR	IDE
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'
 bit 12-2 **SID<10:0>:** Standard Identifier bits
 bit 1 **SRR:** Substitute Remote Request bit
 When IDE = 0:
 1 = Message will request remote transmission
 0 = Normal message
 When IDE = 1:
 The SRR bit must be set to '1'.
 bit 0 **IDE:** Extended Identifier bit
 1 = Message will transmit Extended Identifier
 0 = Message will transmit Standard Identifier

BUFFER 21-2: ECAN™ MESSAGE BUFFER WORD 1

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	—	EID17	EID16	EID15	EID14
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID13	EID12	EID11	EID10	EID9	EID8	EID7	EID6
bit 7							bit 0

Legend:

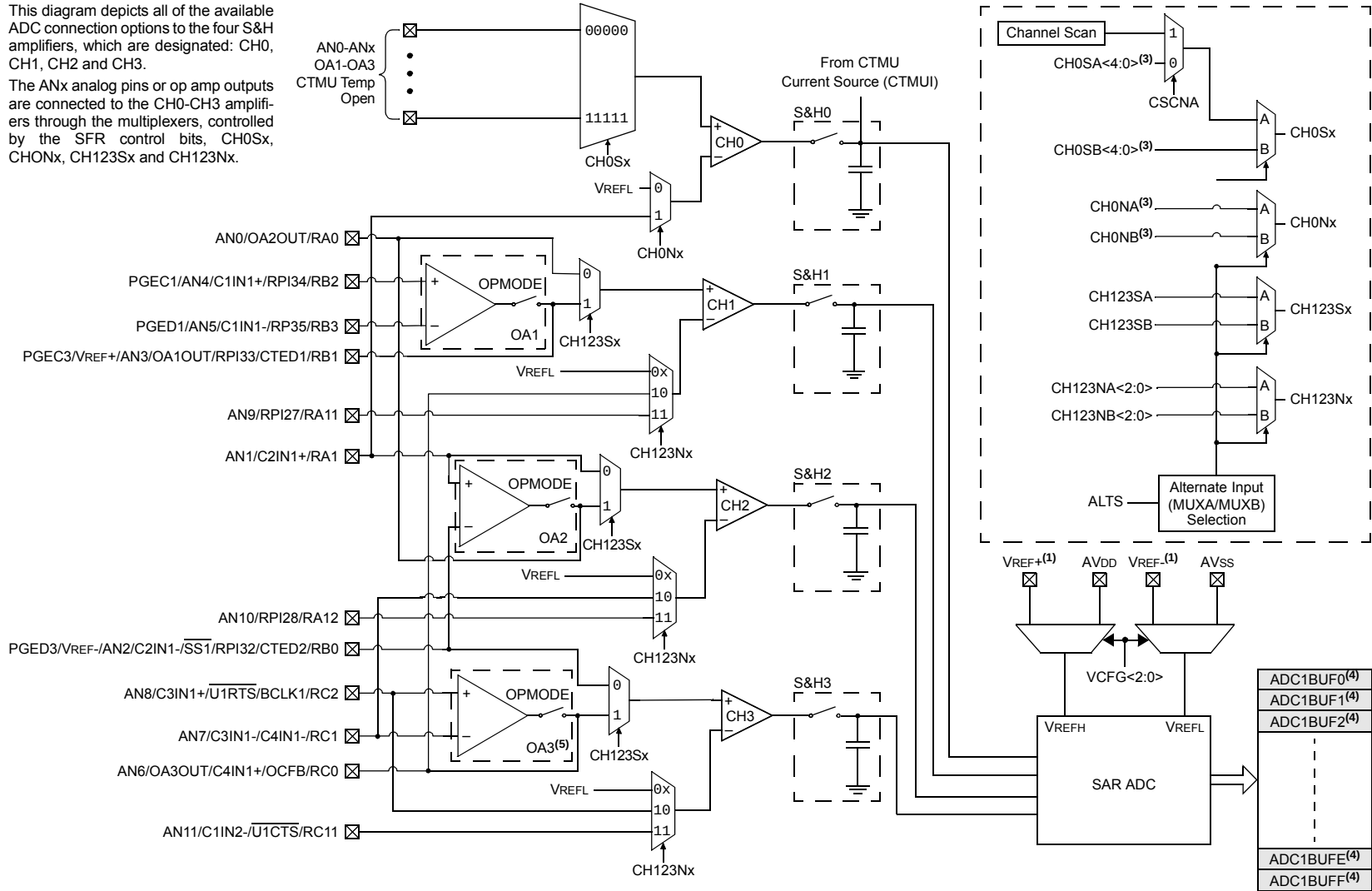
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'
 bit 11-0 **EID<17:6>:** Extended Identifier bits

FIGURE 23-1: ADC MODULE BLOCK DIAGRAM WITH CONNECTION OPTIONS FOR ANx PINS AND OP AMPS

This diagram depicts all of the available ADC connection options to the four S&H amplifiers, which are designated: CH0, CH1, CH2 and CH3.

The ANx analog pins or op amp outputs are connected to the CH0-CH3 amplifiers through the multiplexers, controlled by the SFR control bits, CH0Sx, CHONx, CH123Sx and CH123Nx.



- Note**
- 1: VREF+, VREF- inputs can be multiplexed with other analog inputs.
 - 2: Channels 1, 2 and 3 are not applicable for the 12-bit mode of operation.
 - 3: These bits can be updated with Step commands from the PTG module. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.
 - 4: When ADDMAEN (AD1CON4<8>) = 1, enabling DMA, only ADC1BUF0 is used.
 - 5: OA3 is not available for 28-pin devices.

REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
VCFG2	VCFG1	VCFG0	—	—	CSCNA	CHPS1	CHPS0
bit 15						bit 8	

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **VCFG<2:0>**: Converter Voltage Reference Configuration bits

Value	VREFH	VREFL
000	AVDD	Avss
001	External VREF+	Avss
010	AVDD	External VREF-
011	External VREF+	External VREF-
1xx	AVDD	AVSS

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **CSCNA**: Input Scan Select bit

1 = Scans inputs for CH0+ during Sample MUXA

0 = Does not scan inputs

bit 9-8 **CHPS<1:0>**: Channel Select bits

In 12-bit mode (AD21B = 1), the CHPS<1:0> bits are Unimplemented and are Read as '0':

1x = Converts CH0, CH1, CH2 and CH3

01 = Converts CH0 and CH1

00 = Converts CH0

bit 7 **BUFS**: Buffer Fill Status bit (only valid when BUFM = 1)

1 = ADC is currently filling the second half of the buffer; the user application should access data in the first half of the buffer

0 = ADC is currently filling the first half of the buffer; the user application should access data in the second half of the buffer

bit 6-2 **SMPI<4:0>**: Increment Rate bits

When ADDMAEN = 0:

x1111 = Generates interrupt after completion of every 16th sample/conversion operation

x1110 = Generates interrupt after completion of every 15th sample/conversion operation

.

.

.

x0001 = Generates interrupt after completion of every 2nd sample/conversion operation

x0000 = Generates interrupt after completion of every sample/conversion operation

When ADDMAEN = 1:

11111 = Increments the DMA address after completion of every 32nd sample/conversion operation

11110 = Increments the DMA address after completion of every 31st sample/conversion operation

.

.

.

00001 = Increments the DMA address after completion of every 2nd sample/conversion operation

00000 = Increments the DMA address after completion of every sample/conversion operation

REGISTER 25-6: CMxFLTR: COMPARATOR x FILTER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'bit 6-4 **CFSEL<2:0>:** Comparator Filter Input Clock Select bits111 = T5CLK⁽¹⁾110 = T4CLK⁽²⁾101 = T3CLK⁽¹⁾100 = T2CLK⁽²⁾

011 = Reserved

010 = SYNCO1⁽³⁾001 = FOSC⁽⁴⁾000 = Fp⁽⁴⁾bit 3 **CFLTREN:** Comparator Filter Enable bit

1 = Digital filter is enabled

0 = Digital filter is disabled

bit 2-0 **CFDIV<2:0>:** Comparator Filter Clock Divide Select bits

111 = Clock Divide 1:128

110 = Clock Divide 1:64

101 = Clock Divide 1:32

100 = Clock Divide 1:16

011 = Clock Divide 1:8

010 = Clock Divide 1:4

001 = Clock Divide 1:2

000 = Clock Divide 1:1

Note 1: See the Type C Timer Block Diagram (Figure 13-2).**Note 2:** See the Type B Timer Block Diagram (Figure 13-1).**Note 3:** See the High-Speed PWMx Module Register Interconnection Diagram (Figure 16-2).**Note 4:** See the Oscillator System Diagram (Figure 9-1).

29.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB XC Compiler
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for
Various Device Families
- Simulators
 - MPLAB X SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
 - MPLAB ICD 3
 - PICKit™ 3
- Device Programmers
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards,
Evaluation Kits and Starter Kits
- Third-party development tools

29.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

FIGURE 30-3: I/O TIMING CHARACTERISTICS

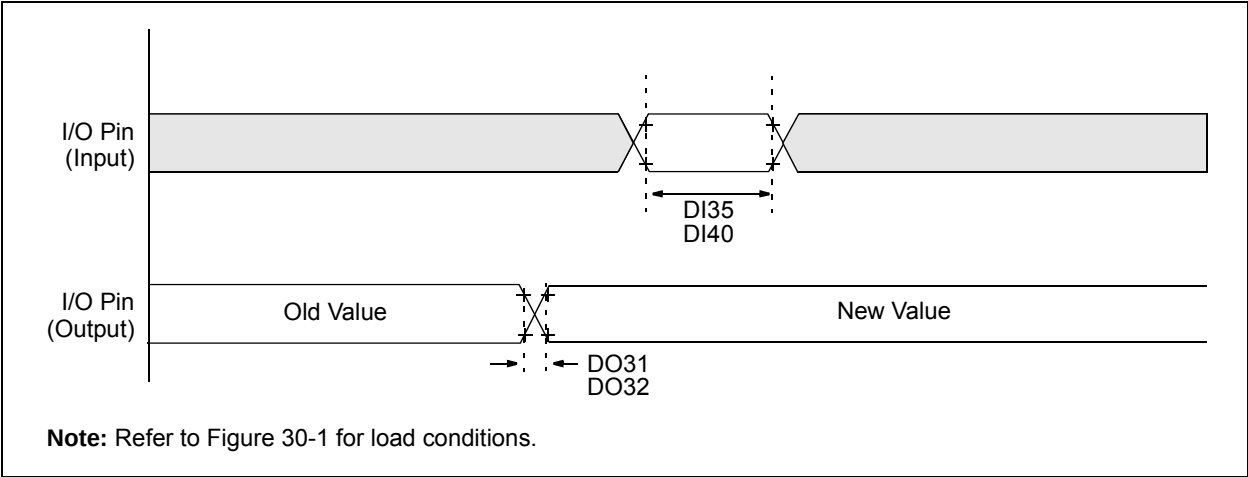


TABLE 30-21: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Param No.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
DO31	TioR	Port Output Rise Time	—	5	10	ns	
DO32	TioF	Port Output Fall Time	—	5	10	ns	
DI35	TINP	INTx Pin High or Low Time (input)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	Tcy	

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

FIGURE 30-4: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS

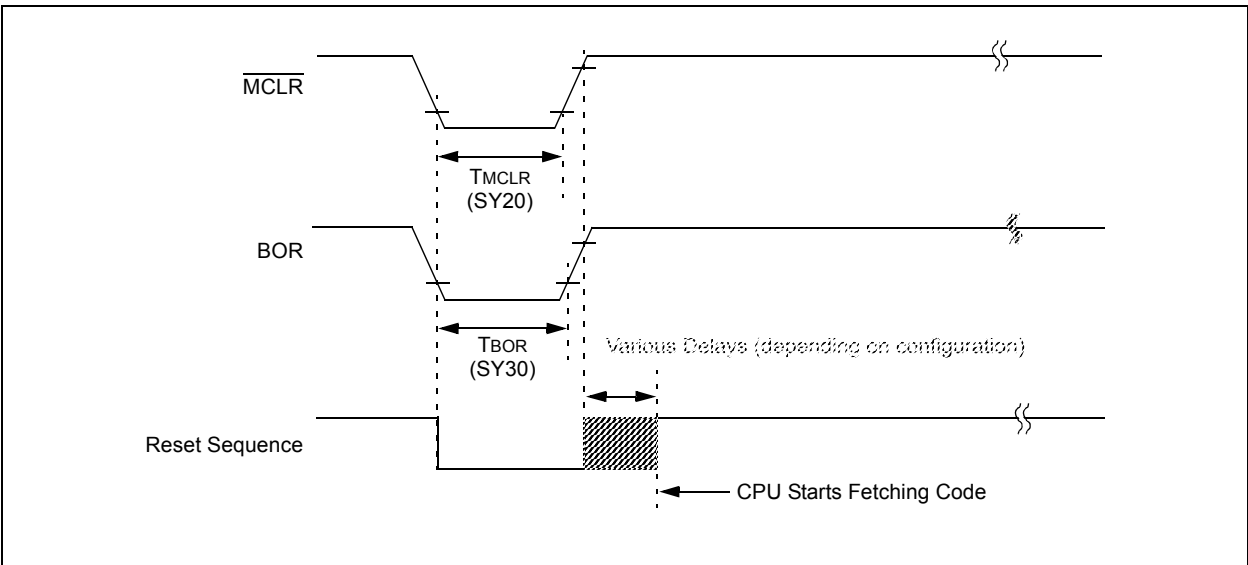


FIGURE 30-7: OUTPUT COMPARE x MODULE (OCx) TIMING CHARACTERISTICS

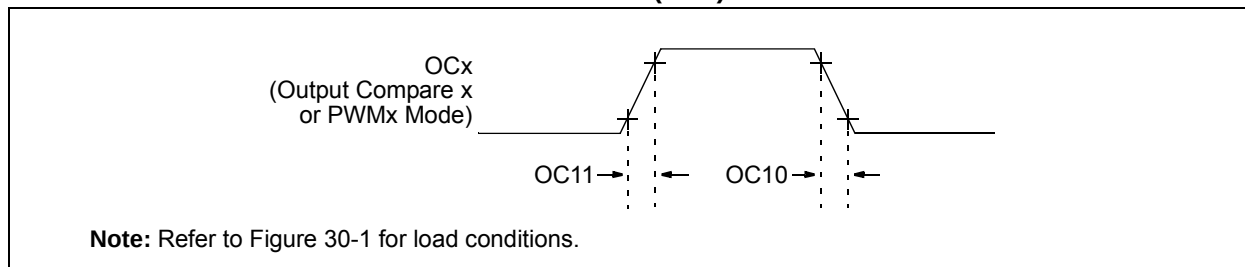


TABLE 30-27: OUTPUT COMPARE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See Parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter DO31

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-8: OCx/PWMx MODULE TIMING CHARACTERISTICS

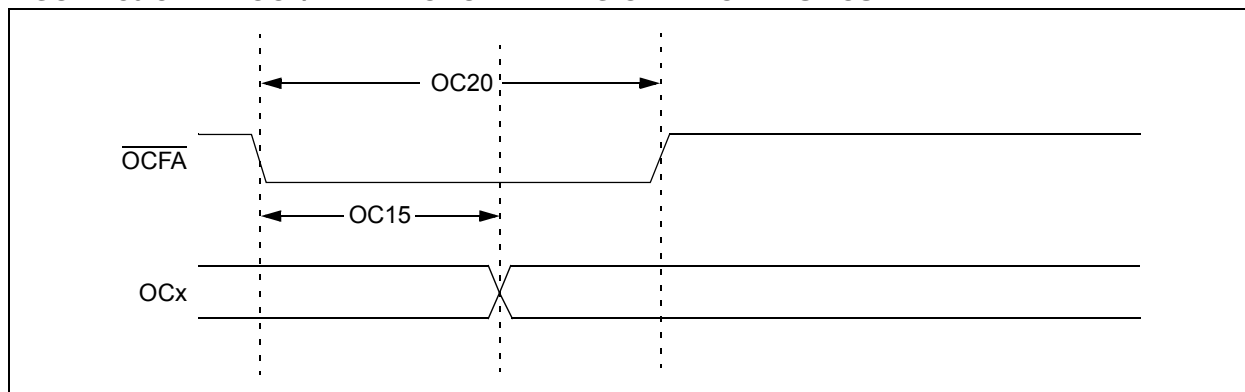


TABLE 30-28: OCx/PWMx MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC15	TFD	Fault Input to PWMx I/O Change	—	—	$T_{CY} + 20$	ns	
OC20	TFLT	Fault Input Pulse Width	$T_{CY} + 20$	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 30-41: SPI1 MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	CKP	SMP
15 MHz	Table 30-42	—	—	0,1	0,1	0,1
10 MHz	—	Table 30-43	—	1	0,1	1
10 MHz	—	Table 30-44	—	0	0,1	1
15 MHz	—	—	Table 30-45	1	0	0
11 MHz	—	—	Table 30-46	1	1	0
15 MHz	—	—	Table 30-47	0	1	0
11 MHz	—	—	Table 30-48	0	0	0

FIGURE 30-22: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0)
TIMING CHARACTERISTICS

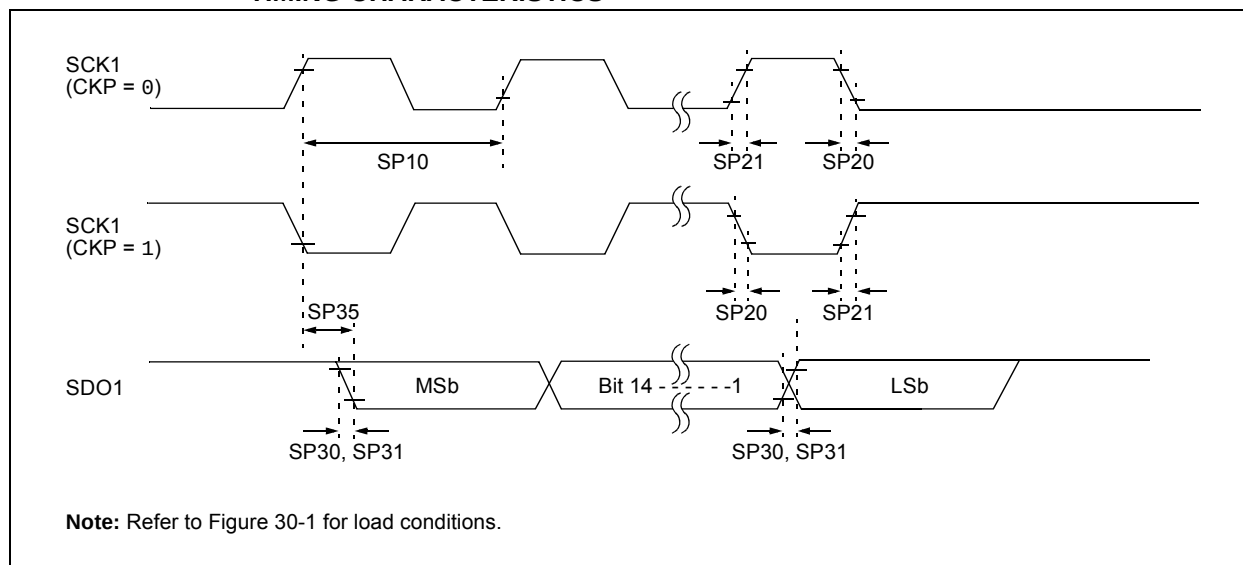


TABLE 30-49: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Param No.	Symbol	Characteristic ⁽⁴⁾		Min. ⁽¹⁾	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM11	THI:SCL	Clock High Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_b$	300	ns	
			1 MHz mode ⁽²⁾	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_b$	300	ns	
			1 MHz mode ⁽²⁾	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode ⁽²⁾	40	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	
			400 kHz mode	0	0.9	μs	
			1 MHz mode ⁽²⁾	0.2	—	μs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			400 kHz mode	$T_{CY}/2$ (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	$T_{CY}/2$ (BRG + 2)	—	μs	
IM40	TAA:SCL	Output Valid From Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode ⁽²⁾	—	400	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽²⁾	0.5	—	μs	
IM50	CB	Bus Capacitive Loading		—	400	pF	
IM51	TPGD	Pulse Gobbler Delay		65	390	ns	(Note 3)

Note 1: BRG is the value of the I²C™ Baud Rate Generator. Refer to “Inter-Integrated Circuit (I²C™)” (DS70330) in the “dsPIC33/PIC24 Family Reference Manual”. Please see the Microchip web site for the latest family reference manual sections.

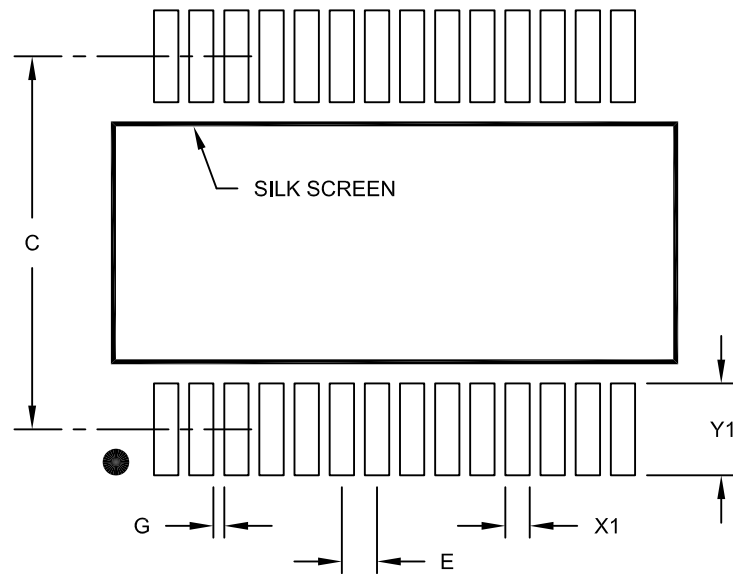
2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: Typical value for this parameter is 130 ns.

4: These parameters are characterized, but not tested in manufacturing.

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C	7.20		
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

PMD (PIC24EPXXXMC20X Devices).....	94	CMxMSKCON (Comparator x Mask Gating Control).....	368
PORTA (PIC24EPXXXGP/MC202, dsPIC33EPXXXGP/MC202/502 Devices)	104	CMxMSKSR (Comparator x Mask Source Select Control).....	366
PORTA (PIC24EPXXXGP/MC203, dsPIC33EPXXXGP/MC203/503 Devices)	103	CORCON (Core Control).....	42, 133
PORTA (PIC24EPXXXGP/MC204, dsPIC33EPXXXGP/MC204/504 Devices)	102	CRCCON1 (CRC Control 1).....	375
PORTA (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	99	CRCCON2 (CRC Control 2).....	376
PORTB (PIC24EPXXXGP/MC202, dsPIC33EPXXXGP/MC202/502 Devices)	104	CRCXORH (CRC XOR Polynomial High)	377
PORTB (PIC24EPXXXGP/MC203, dsPIC33EPXXXGP/MC203/503 Devices)	103	CRCXORL (CRC XOR Polynomial Low).....	377
PORTB (PIC24EPXXXGP/MC204, dsPIC33EPXXXGP/MC204/504 Devices)	102	CTMUCON1 (CTMU Control 1).....	317
PORTB (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	99	CTMUCON2 (CTMU Control 2).....	318
PORTC (PIC23EPXXXGP/MC203, dsPIC33EPXXXGP/MC203/503 Devices)	103	CTMUICON (CTMU Current Control).....	319
PORTC (PIC24EPXXXGP/MC204, dsPIC33EPXXXGP/MC204/504 Devices)	102	CVRCON (Comparator Voltage Reference Control).....	371
PORTC (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	99	CxBUFPNT1 (ECANx Filter 0-3 Buffer Pointer 1).....	300
PORTD (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	100	CxBUFPNT2 (ECANx Filter 4-7 Buffer Pointer 2).....	301
PORTE (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	100	CxBUFPNT3 (ECANx Filter 8-11 Buffer Pointer 3).....	301
PORTF (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	100	CxBUFPNT4 (ECANx Filter 12-15 Buffer Pointer 4).....	302
PORTG (PIC24EPXXXGP/MC206 and dsPIC33EPXXXGP/MC206/506 Devices)	101	CxCFG1 (ECANx Baud Rate Configuration 1).....	298
PTG.....	78	CxCFG2 (ECANx Baud Rate Configuration 2).....	299
PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices).....	79	CxCTRL1 (ECANx Control 1).....	290
PWM Generator 1 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices).....	79	CxCTRL2 (ECANx Control 2).....	291
PWM Generator 2 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices).....	80	CxEC (ECANx Transmit/Receive Error Count)	298
PWM Generator 3 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices).....	80	CxFCTRL (ECANx FIFO Control).....	293
QE11 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices).....	81	CxFEN1 (ECANx Acceptance Filter Enable 1).....	300
Reference Clock	93	CxFIFO (ECANx FIFO Status)	294
SPI1 and SPI2	83	CxFMSKSEL1 (ECANx Filter 7-0 Mask Selection 1).....	304
System Control	93	CxFMSKSEL2 (ECANx Filter 15-8 Mask Selection 2).....	305
Time1 through Time5.....	75	CxINTE (ECANx Interrupt Enable)	297
UART1 and UART2	82	CxINTF (ECANx Interrupt Flag).....	295
Registers		CxRXFnEID (ECANx Acceptance Filter n Extended Identifier)	304
AD1CHS0 (ADC1 Input Channel 0 Select)	333	CxRXFnSID (ECANx Acceptance Filter n Standard Identifier)	303
AD1CHS123 (ADC1 Input Channel 1, 2, 3 Select)	331	CxRXFUL1 (ECANx Receive Buffer Full 1).....	307
AD1CON1 (ADC1 Control 1)	325	CxRXFUL2 (ECANx Receive Buffer Full 2).....	307
AD1CON2 (ADC1 Control 2)	327	CxRXMnEID (ECANx Acceptance Filter Mask n Extended Identifier)	306
AD1CON3 (ADC1 Control 3)	329	CxRXMnSID (ECANx Acceptance Filter Mask n Standard Identifier)	306
AD1CON4 (ADC1 Control 4)	330	CxRXOVF1 (ECANx Receive Buffer Overflow 1).....	308
AD1CSSH (ADC1 Input Scan Select High)	335	CxRXOVF2 (ECANx Receive Buffer Overflow 2).....	308
AD1CSSL (ADC1 Input Scan Select Low).....	336	CxTRMnCON (ECANx TX/RX Buffer mn Control)	309
ALTDTRx (PWMx Alternate Dead-Time)	238	CxVEC (ECANx Interrupt Code).....	292
AUXCONx (PWMx Auxiliary Control).....	247	DEVID (Device ID).....	383
CHOP (PWMx Chop Clock Generator).....	234	DEVREV (Device Revision).....	383
CLKDIV (Clock Divisor).....	158	DMALCA (DMA Last Channel Active Status)	150
CM4CON (Comparator 4 Control)	364	DMAPPS (DMA Ping-Pong Status)	151
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CMxCON (Comparator x Control, x = 1,2,3).....	362	DMARQC (DMA Request Collision Status).....	149
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