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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc504-e-tl

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Pin Diagrams (Continued)



FIGURE 3-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X CPU BLOCK DIAGRAM





FIGURE 4-8: DATA MEMORY MAP FOR dsPIC33EP64MC20X/50X AND dsPIC33EP64GP50X DEVICES





R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0	
OA	OB	SA	SB	OAB	SAB	DA	DC	
bit 15							bit 8	
R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R-0	R/W-0	R/W-0	R/W-0	R/W-0	
	IPL<2:0> ⁽²⁾		RA	Ν	OV	Z	С	
bit 7						-	bit 0	
								1

REGISTER 7-1: SR: CPU STATUS REGISTER⁽¹⁾

Legend:	C = Clearable bit		-
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5	IPL<2:0>: CPU Interrupt Priority Level Status bits ^(2,3)
	111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
	110 = CPU Interrupt Priority Level is 6 (14)
	101 = CPU Interrupt Priority Level is 5 (13)
	100 = CPU Interrupt Priority Level is 4 (12)
	011 = CPU Interrupt Priority Level is 3 (11)
	010 = CPU Interrupt Priority Level is 2 (10)
	001 = CPU Interrupt Priority Level is 1 (9)
	000 = CPU Interrupt Priority Level is 0 (8)

- **Note 1:** For complete register details, see Register 3-1.
 - 2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
 - **3:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

HS/HC-	0 HS/HC-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
FLTSTAT	-(1) CLSTAT ⁽¹⁾	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB ⁽²⁾	MDCS ⁽²⁾	
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	
DTC1	DTC0	DTCP ⁽³⁾	<u> </u>	MTBS	CAM ^(2,4)	XPRES ⁽⁵⁾	IUE ⁽²⁾	
bit 7							bit 0	
Legend:		HC = Hardware	Clearable bit	HS = Hardwa	are Settable bit			
R = Reada	able bit	W = Writable bi	t	U = Unimplei	mented bit, rea	d as '0'		
-n = Value	at POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unk	nown	
bit 15	FLTSTAT: Fai 1 = Fault inter 0 = No Fault i This bit is clea	ult Interrupt Statu rrupt is pending interrupt is pendi	us bit ⁽¹⁾ ng LTIEN = 0					
hit 14	CI STAT. Cur	rent-l imit Interru	nt Status hit(1)					
	1 = Current-lin 0 = No curren This bit is clea	mit interrupt is pentitienter interrupt is pentitienter interrupt is ared by setting C	ending s pending CLIEN = 0.					
bit 13	TRGSTAT: Tr	igger Interrupt S	tatus bit					
	1 = Trigger in 0 = No trigger This bit is clea	terrupt is pending r interrupt is pend ared by setting T	g ding RGIEN = 0.					
bit 12	FLTIEN: Faul	t Interrupt Enabl	e bit					
	1 = Fault inter 0 = Fault inter	rrupt is enabled rrupt is disabled	and the FLTST	AT bit is cleare	ed			
bit 11	CLIEN: Curre	ent-Limit Interrup	t Enable bit					
	1 = Current-lii 0 = Current-lii	mit interrupt is er mit interrupt is di	nabled sabled and the	CLSTAT bit is	cleared			
bit 10	TRGIEN: Trig	ger Interrupt Ena	able bit					
	1 = A trigger e 0 = Trigger ev	event generates /ent interrupts ar	an interrupt rec	quest the TRGSTAT	bit is cleared			
bit 9	ITB: Independ	dent Time Base	Mode bit ⁽²⁾					
	 1 = PHASEx register provides time base period for this PWM generator 0 = PTPER register provides timing for this PWM generator 							
bit 8	MDCS: Maste	er Duty Cycle Re	gister Select bi	it(2)				
	1 = MDC regi 0 = PDCx reg	ster provides du ister provides du	ty cycle informa ity cycle inform	ation for this P ation for this F	WM generator WM generator			
Note 1:	Software must clea	ar the interrupt st	atus here and	in the correspo	onding IFSx bit	in the interrup	ot controller.	
2:	These bits should	not be changed	after the PWM	, is enabled (P	PTEN = 1).			
3:	DTC<1:0> = 11 for	r DTCP to be effe	ective; otherwis	se, DTCP is ig	nored.			
4:	The Independent T CAM bit is ignored	Time Base (ITB =	1) mode must	be enabled to	use Center-Ali	igned mode. If	TTB = 0, the	
-	T		· · · · · · · · · · · · · · · · · · ·					

REGISTER 16-7: PWMCONx: PWMx CONTROL REGISTER

5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

REGISTER 17-17: INT1TMRH: INTERVAL 1 TIMER HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTTM	R<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTTM	R<23:16>			
bit 7							bit 0
Legend:							
R = Readable b	bit	W = Writable bi	it	U = Unimplem	nented bit, read	d as '0'	
-n = Value at P	-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown						

bit 15-0 INTTMR<31:16>: High Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

REGISTER 17-18: INT1TMRL: INTERVAL 1 TIMER LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTTM	1R<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTT	/IR<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable b	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value at P	-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown						

bit 15-0 INTTMR<15:0>: Low Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

19.0 INTER-INTEGRATED CIRCUIT[™] (I²C[™])

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Inter-Integrated Circuit™ (I²C™)" (DS70330) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.
 - 3: There are minimum bit rates of approximately FCY/512. As a result, high processor speeds may not support 100 Kbit/second operation. See timing specifications, IM10 and IM11, and the "Baud Rate Generator" in the "dsPIC33/PIC24 Family Reference Manual".

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X family of devices contains two Inter-Integrated Circuit (I²C) modules: I2C1 and I2C2.

The l^2C module provides complete hardware support for both Slave and Multi-Master modes of the l^2C serial communication standard, with a 16-bit interface.

The I^2C module has a 2-pin interface:

- · The SCLx pin is clock
- The SDAx pin is data

The I²C module offers the following key features:

- I²C interface supporting both Master and Slave modes of operation
- I²C Slave mode supports 7 and 10-bit addressing
- I²C Master mode supports 7 and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation, detects bus collision and arbitrates accordingly
- Intelligent Platform Management Interface (IPMI)
 support
- System Management Bus (SMBus) support

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8
R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0

REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0
bit 7							bit 0
Legend:		C = Writable b	oit, but only '0'	can be writter	ו to clear the bit		

Legend:	C = Writable bit, but only '0' can be written to clear the bit				
R = Readable bit	W = Writable bit	V = Writable bit U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 RXOVF<15:0>: Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 RXOVF<31:16>: Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

21.5 ECAN Message Buffers

ECAN Message Buffers are part of RAM memory. They are not ECAN Special Function Registers. The user application must directly write into the RAM area that is configured for ECAN Message Buffers. The location and size of the buffer area is defined by the user application.

BUFFER 21-1: ECAN™ MESSAGE BUFFER WORD 0

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
		_	SID10	SID9	SID8	SID7	SID6
bit 15							bit 8
r							
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID5	SID4	SID3	SID2	SID1	SID0	SRR	IDE
bit 7							bit 0
Legend:							
R = Readable b	bit	W = Writable	bit	U = Unimplei	mented bit, read	l as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unki	nown
bit 15-13	Unimplemen	ted: Read as '	0'				
bit 12-2	SID<10:0>: S	Standard Identif	ier bits				
bit 1	SRR: Substitu	ute Remote Re	quest bit				
	When IDE = 0	<u>):</u>					
	1 = Message	will request rer	mote transmis	ssion			
	0 = Normal m	lessage					
When IDE = 1:							
	The SRR bit r	must be set to '	1'.				
bit 0	IDE: Extended Identifier bit						
	1 = Message	will transmit Ex	ktended Ident	ifier			
	0 = Message	will transmit St	andard Identi	fier			

BUFFER 21-2: ECAN™ MESSAGE BUFFER WORD 1

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—		EID17	EID16	EID15	EID14
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID13	EID12	EID11	EID10	EID9	EID8	EID7	EID6
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	bit	U = Unimplemented bit, read as '0'			
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown		iown	

bit 15-12 Unimplemented: Read as '0'

bit 11-0 EID<17:6>: Extended Identifier bits

REGISTER 2	5-3: CM4C	ON: COMPAI	RATOR 4 CO	ONTROL RE	GISTER		
R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
CON	COE	CPOL				CEVT	COUT
bit 15							bit 8
R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1	EVPOL0		CREF ⁽¹⁾		_	CCH1 ⁽¹⁾	CCH0 ⁽¹⁾
bit 7	•				•		bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	l as '0'	
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkn	iown
bit 15	CON: Compa	rator Enable bi	t				
	1 = Comparat	tor is enabled					
	0 = Comparat	tor is disabled					
bit 14	COE: Compa	rator Output Er	hable bit				
	1 = Comparat	tor output is pre	esent on the C	xout pin			
hit 13		arator Output IS III	Polarity Salact	bit			
bit 15	1 = Comparat	tor output is inv	erted				
	0 = Comparat	tor output is not	t inverted				
bit 12-10	Unimplemen	ted: Read as ')'				
bit 9	CEVT: Compa	arator Event bit					
	1 = Compara	itor event acco	ording to EVF	POL<1:0> sett	tings occurred;	disables future	triggers and
		s until the bit is	cleared				
hit 0		areter Output h					
DILO	When CPOL :	= 0 (non-invert	ad polarity):				
	1 = VIN + > VIN	N-	ou polanty).				
	0 = VIN + < VIN	N-					
	When CPOL	= 1 (inverted po	plarity):				
	1 = VIN + < VIN $0 = VIN + > VIN$	N-					
bit 7-6		• Trigger/Event	Interrunt Pol	arity Select hits	e		
bit 7-0	11 = Trigger/e	event/interrupt	nenerated on	any change of	s f the comparato	r output (while (CEVT = 0
	10 = Trigger/e output (v	event/interrupt g while CEVT = 0	jenerated only	on high-to-lov	v transition of the	e polarity selecte	ed comparator
	<u>If CPOL</u> Low-to-h	= 1 (inverted p high transition of	olarity): of the compara	ator output.			
	If CPOL	= 0 (non-inver	ted polarity):				
	Hign-to-	low transition o	t the compara	ator output.	a transition of the		ad comparator
	output (v	while CEVT = 0)	on iow-to-nigr	n transition of the	e polarity selecte	ed comparator
	<u>If CPOL</u> High-to-	<u>= 1 (inverted p</u> low transition o	olarity): f the compara	ator output.			
	<u>If CPOL</u> Low-to-h	<u>= 0 (non-inver</u> nigh transition o	ted polarity): of the compara	ator output.			
	00 = Trigger/e	event/interrupt	generation is	disabled			
							<i>.</i>

Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.

REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	RW-0
—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0
bit 15							bit 8

| R/W-0 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SELSRCB3 | SELSRCB2 | SELSRCB1 | SELSRCB0 | SELSRCA3 | SELSRCA2 | SELSRCA1 | SELSRCA0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 Unimplemented: Read as '0'

bit 11-8	SELSRCC<3:0>: Mask C Input Select bits
	1111 = FLT4
	1110 = FLT2
	1101 = PTGO19
	1100 = PTGO18
	1011 = Reserved
	1010 = Reserved
	1001 = Reserved
	1000 = Reserved
	0111 = Reserved
	0110 = Reserved
	0101 = PWM3H
	0100 = PWM3L
	0011 = PWM2H
	0010 = PWM2L
	0001 = PWM1H
	0000 = PWM1L
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1001 = Reserved 1000 = Reserved 0011 = Reserved 0111 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved 0110 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1000 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3I
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1000 = Reserved 0111 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0111 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2I
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0101 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0101 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H 0000 = PWM1I





26.1 Overview

The CRC module can be programmed for CRC polynomials of up to the 32nd order, using up to 32 bits. Polynomial length, which reflects the highest exponent in the equation, is selected by the PLEN<4:0> bits (CRCCON2<4:0>).

The CRCXORL and CRCXORH registers control which exponent terms are included in the equation. Setting a particular bit includes that exponent term in the equation; functionally, this includes an XOR operation on the corresponding bit in the CRC engine. Clearing the bit disables the XOR.

For example, consider two CRC polynomials, one a 16-bit equation and the other a 32-bit equation:

$$\begin{array}{c} x16+x12+x5+1\\ \text{and}\\ x32+x26+x23+x22+x16+x12+x11+x10+x8+x7\\ +x5+x4+x2+x+1 \end{array}$$

To program these polynomials into the CRC generator, set the register bits as shown in Table 26-1.

Note that the appropriate positions are set to '1' to indicate that they are used in the equation (for example, X26 and X23). The 0 bit required by the equation is always XORed; thus, X0 is a don't care. For a polynomial of length N, it is assumed that the *N*th bit will always be used, regardless of the bit setting. Therefore, for a polynomial length of 32, there is no 32nd bit in the CRCxOR register.

TABLE 26-1:CRC SETUP EXAMPLES FOR16 AND 32-BIT POLYNOMIAL

CBC Control	Bit Values				
Bits	16-bit Polynomial	32-bit Polynomial			
PLEN<4:0>	01111	11111			
X<31:16>	0000 0000 0000 000x	0000 0100 1100 0001			
X<15:0>	0001 0000 0010 000x	0001 1101 1011 011x			

26.2 Programmable CRC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

26.2.1 KEY RESOURCES

- "Programmable Cyclic Redundancy Check (CRC)" (DS70346) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

Field	Description
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 working registers ∈ {W0W15}
Wnd	One of 16 destination working registers ∈ {W0W15}
Wns	One of 16 source working registers ∈ {W0W15}
WREG	W0 (working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb] }
Wx	X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}
Wxd	X Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}
Wy	Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}
Wyd	Y Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}

TABLE 28-1:	SYMBOLS USED IN OPCODE DESCRIPTIONS ((CONTINUED)



AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param No.	Symb	Characteristic	Min.	Тур. ⁽¹⁾	Max.	Units	Conditions
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	_	60	MHz	EC
		Oscillator Crystal Frequency	3.5 10	—	10 25	MHz MHz	XT HS
OS20	Tosc	Tosc = 1/Fosc	8.33	—	DC	ns	+125°C
		Tosc = 1/Fosc	7.14	—	DC	ns	+85°C
OS25	TCY	Instruction Cycle Time ⁽²⁾	16.67	—	DC	ns	+125°C
		Instruction Cycle Time ⁽²⁾	14.28	—	DC	ns	+85°C
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.45 x Tosc	—	0.55 x Tosc	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time ^(3,4)	—	5.2	—	ns	
OS41	TckF	CLKO Fall Time ^(3,4)	—	5.2	—	ns	
OS42	Gм	External Oscillator Transconductance ⁽⁴⁾	—	12	—	mA/V	HS, VDD = 3.3V, TA = +25°C
			—	6	—	mA/V	XT, VDD = 3.3V, TA = +25°C

TABLE 30-17: EXTERNAL CLOCK TIMING REQUIREMENTS

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- 2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Minimum" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Maximum" cycle time limit is "DC" (no clock) for all devices.
- 3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.
- 4: This parameter is characterized, but not tested in manufacturing.

31.2 **AC Characteristics and Timing Parameters**

The information contained in this section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X AC characteristics and timing parameters for high-temperature devices. However, all AC timing specifications in this section are the same as those in Section 30.2 "AC Characteristics and Timing Parameters", with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter OS53 in Section 30.2 "AC Characteristics and Timing Parameters" is the Industrial and Extended temperature equivalent of HOS53.

TABLE 31-9: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

	Standard Operating Conditions: 3.0V to 3.6V
	(unless otherwise stated)
AC CHARACTERISTICS	Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$
	Operating voltage VDD range as described in Table 31-1.

FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



TABLE 31-10: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				
Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions
HOS53	DCLK	CLKO Stability (Jitter) ⁽¹⁾	-5	0.5	5	%	Measured over 100 ms period

These parameters are characterized by similarity, but are not tested in manufacturing. This specification is Note 1: based on clock cycle by clock cycle measurements. To calculate the effective jitter for individual time bases or communication clocks use this formula:

$$Peripheral Clock Jitter = \frac{DCLK}{\sqrt{\frac{FOSC}{Peripheral Bit Rate Clock}}}$$

For example: FOSC = 32 MHz, DCLK = 5%, SPIx bit rate clock (i.e., SCKx) is 2 MHz. Г

$$SPI SCK Jitter = \left\lfloor \frac{D_{CLK}}{\sqrt{\left(\frac{32 MHz}{2 MHz}\right)}} \right\rfloor = \left\lfloor \frac{5\%}{\sqrt{16}} \right\rfloor = \left\lfloor \frac{5\%}{4} \right\rfloor = 1.25\%$$

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AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				
Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions
		ADC A	Accuracy	(12-Bit	Mode) ⁽¹⁾		
HAD20a	Nr	Resolution ⁽³⁾	1:	2 Data B	its	bits	
HAD21a	INL	Integral Nonlinearity	-5.5	_	5.5	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V
HAD22a	DNL	Differential Nonlinearity	-1	—	1	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V
HAD23a	Gerr	Gain Error	-10	—	10	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V
HAD24a	EOFF	Offset Error	-5	—	5	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V
		Dynamic	Performa	nce (12·	Bit Mode	e) ⁽²⁾	
HAD33a	FNYQ	Input Signal Bandwidth	_	_	200	kHz	

TABLE 31-12: ADC MODULE SPECIFICATIONS (12-BIT MODE)

Note 1: These parameters are characterized, but are tested at 20 ksps only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

TABLE 31-13: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHAF	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$							
Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions	
	ADC Accuracy (10-Bit Mode) ⁽¹⁾							
HAD20b	Nr	Resolution ⁽³⁾	1() Data B	its	bits		
HAD21b	INL	Integral Nonlinearity	-1.5	_	1.5	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V	
HAD22b	DNL	Differential Nonlinearity	-0.25	_	0.25	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V	
HAD23b	Gerr	Gain Error	-2.5	_	2.5	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V	
HAD24b	EOFF	Offset Error	-1.25	_	1.25	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V	
	Dynamic Performance (10-Bit Mode) ⁽²⁾							
HAD33b	Fnyq	Input Signal Bandwidth		_	400	kHz		

Note 1: These parameters are characterized, but are tested at 20 ksps only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 30.0 "Electrical Characteristics"	Removed Voltage on VCAP with respect to Vss and added Note 5 in Absolute Maximum Ratings ⁽¹⁾ .
	Removed Parameter DC18 (VCORE) and Note 3 from the DC Temperature and Voltage Specifications (see Table 30-4).
	Updated Note 1 in the DC Characteristics: Operating Current (IDD) (see Table 30-6).
	Updated Note 1 in the DC Characteristics: Idle Current (IIDLE) (see Table 30-7).
	Changed the Typical values for Parameters DC60a-DC60d and updated Note 1 in the DC Characteristics: Power-down Current (IPD) (see Table 30-8).
	Updated Note 1 in the DC Characteristics: Doze Current (IDOZE) (see Table 30-9).
	Updated Note 2 in the Electrical Characteristics: BOR (see Table 30-12).
	Updated Parameters CM20 and CM31, and added Parameters CM44 and CM45 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14).
	Added the Op amp/Comparator Reference Voltage Settling Time Specifications (see Table 30-15).
	Added Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16).
	Updated Internal FRC Accuracy Parameter F20a (see Table 30-21).
	Updated the Typical value and Units for Parameter CTMUI1, and added Parameters CTMUI4, CTMUFV1, and CTMUFV2 to the CTMU Current Source Specifications (see Table 30-55).
Section 31.0 "Packaging Information"	Updated packages by replacing references of VLAP with TLA.
"Product Identification System"	Changed VLAP to TLA.

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