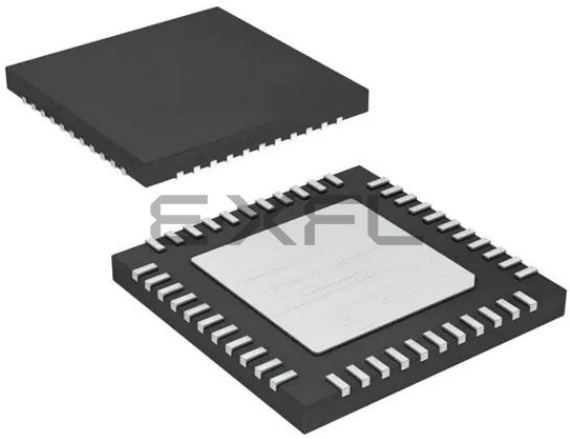
Microchip Technology - DSPIC33EP32MC504-H/ML Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

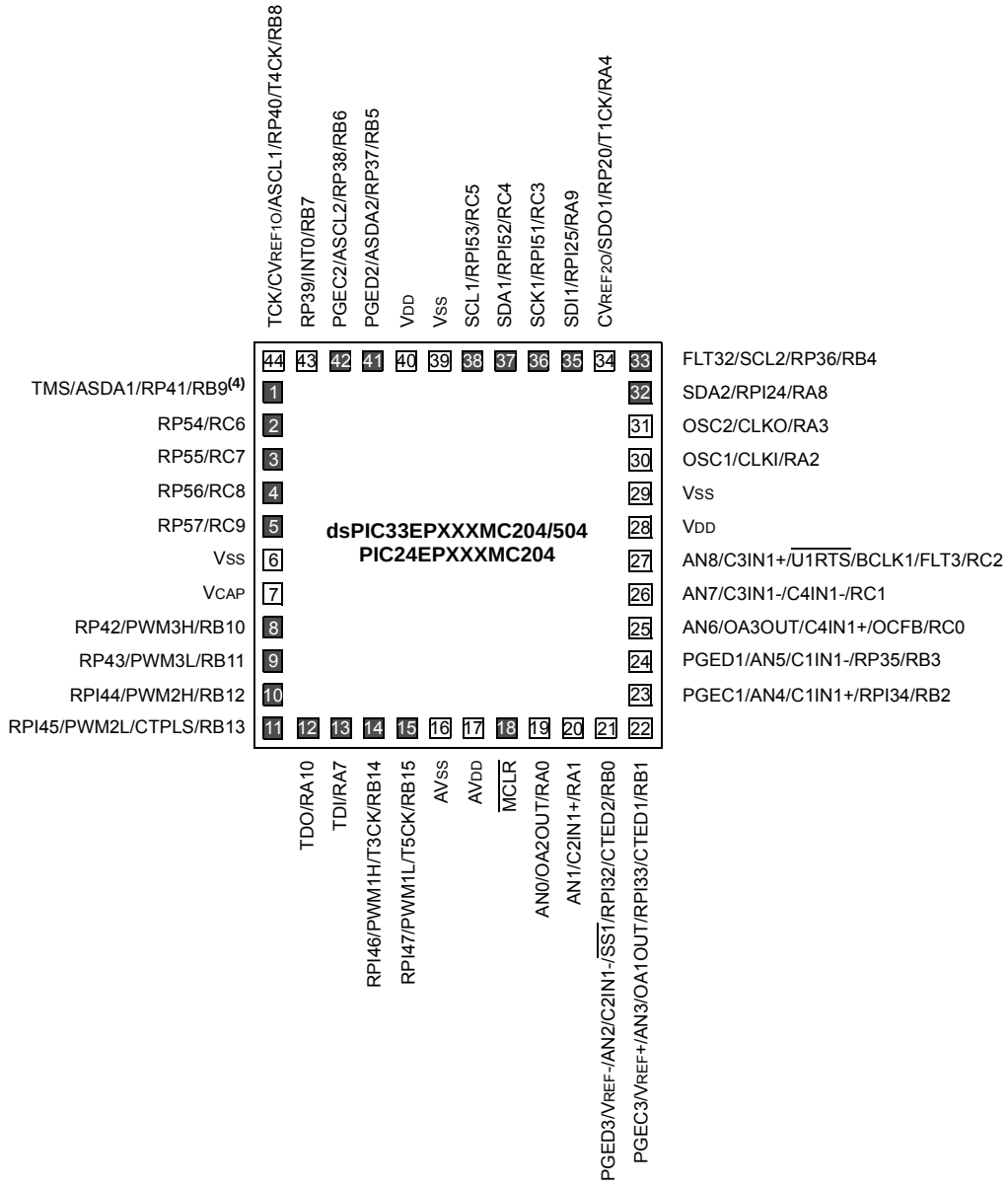
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc504-h-ml

Pin Diagrams (Continued)

44-Pin VTLA(1,2,3)

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

3.6 CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

3.6.1 KEY RESOURCES

- **"CPU"** (DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-6).

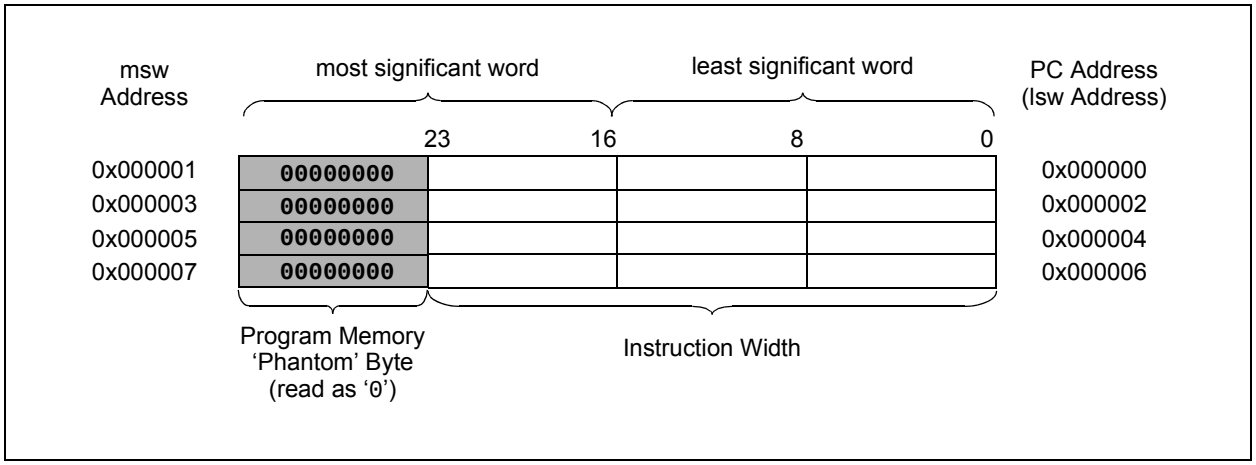
Program memory addresses are always word-aligned on the lower word and addresses are incremented, or decremented by two, during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices reserve the addresses between 0x000000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address, 0x000000, of Flash memory, with the actual address for the start of code at address, 0x000002, of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in **Section 7.1 "Interrupt Vector Table"**.

FIGURE 4-6: PROGRAM MEMORY ORGANIZATION



REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PLLDIV8
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
PLLDIV7	PLLDIV6	PLLDIV5	PLLDIV4	PLLDIV3	PLLDIV2	PLLDIV1	PLLDIV0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as ‘0’

bit 8-0 **PLLDIV<8:0>:** PLL Feedback Divisor bits (also denoted as ‘M’, PLL multiplier)

111111111 = 513
•
•
•
000110000 = 50 (default)
•
•
•
000000010 = 4
000000001 = 3
000000000 = 2

REGISTER 11-12: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SCK2INR<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SDI2R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **SCK2INR<6:0>:** Assign SPI2 Clock Input (SCK2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **SDI2R<6:0>:** Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

NOTES:

REGISTER 17-13: QEI1LECH: QEI1 LESS THAN OR EQUAL COMPARE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **QEILEC<31:16>:** High Word Used to Form 32-Bit Less Than or Equal Compare Register (QEI1LEC) bits

REGISTER 17-14: QEI1LECL: QEI1 LESS THAN OR EQUAL COMPARE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **QEILEC<15:0>:** Low Word Used to Form 32-Bit Less Than or Equal Compare Register (QEI1LEC) bits

REGISTER 21-10: CxCFG2: ECANx BAUD RATE CONFIGURATION REGISTER 2

U-0	R/W-x	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	WAKFIL	—	—	—	SEG2PH2	SEG2PH1	SEG2PH0
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SEG2PHTS	SAM	SEG1PH2	SEG1PH1	SEG1PH0	PRSEG2	PRSEG1	PRSEG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **WAKFIL:** Select CAN Bus Line Filter for Wake-up bit
1 = Uses CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 13-11 **Unimplemented:** Read as '0'

bit 10-8 **SEG2PH<2:0>:** Phase Segment 2 bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 7 **SEG2PHTS:** Phase Segment 2 Time Select bit
1 = Freely programmable
0 = Maximum of SEG1PHx bits or Information Processing Time (IPT), whichever is greater

bit 6 **SAM:** Sample of the CAN Bus Line bit
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 5-3 **SEG1PH<2:0>:** Phase Segment 1 bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 2-0 **PRSEG<2:0>:** Propagation Time Segment bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

REGISTER 21-19: CxFMSKSEL2: ECANx FILTER 15-8 MASK SELECTION REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15MSK<1:0>		F14MSK<1:0>		F13MSK<1:0>		F12MSK<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11MSK<1:0>		F10MSK<1:0>		F9MSK<1:0>		F8MSK<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **F15MSK<1:0>:** Mask Source for Filter 15 bits
11 = Reserved
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F14MSK<1:0>:** Mask Source for Filter 14 bits (same values as bits<15:14>)

bit 11-10 **F13MSK<1:0>:** Mask Source for Filter 13 bits (same values as bits<15:14>)

bit 9-8 **F12MSK<1:0>:** Mask Source for Filter 12 bits (same values as bits<15:14>)

bit 7-6 **F11MSK<1:0>:** Mask Source for Filter 11 bits (same values as bits<15:14>)

bit 5-4 **F10MSK<1:0>:** Mask Source for Filter 10 bits (same values as bits<15:14>)

bit 3-2 **F9MSK<1:0>:** Mask Source for Filter 9 bits (same values as bits<15:14>)

bit 1-0 **F8MSK<1:0>:** Mask Source for Filter 8 bits (same values as bits<15:14>)

23.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Analog-to-Digital Converter (ADC)"** (DS70621) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices have one ADC module. The ADC module supports up to 16 analog input channels.

On ADC1, the AD12B bit (AD1CON1<10>) allows the ADC module to be configured by the user as either a 10-bit, 4 Sample-and-Hold (S&H) ADC (default configuration) or a 12-bit, 1 S&H ADC.

Note: The ADC module needs to be disabled before modifying the AD12B bit.

23.1 Key Features

23.1.1 10-BIT ADC CONFIGURATION

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) conversion
- Conversion speeds of up to 1.1 Msps
- Up to 16 analog input pins
- Connections to three internal op amps
- Connections to the Charge Time Measurement Unit (CTMU) and temperature measurement diode
- Channel selection and triggering can be controlled by the Peripheral Trigger Generator (PTG)
- External voltage reference input pins
- Simultaneous sampling of:
  - Up to four analog input pins
  - Three op amp outputs
  - Combinations of analog inputs and op amp outputs
- Automatic Channel Scan mode
- Selectable conversion Trigger source
- Selectable Buffer Fill modes
- Four result alignment options (signed/unsigned, fractional/integer)
- Operation during CPU Sleep and Idle modes

23.1.2 12-BIT ADC CONFIGURATION

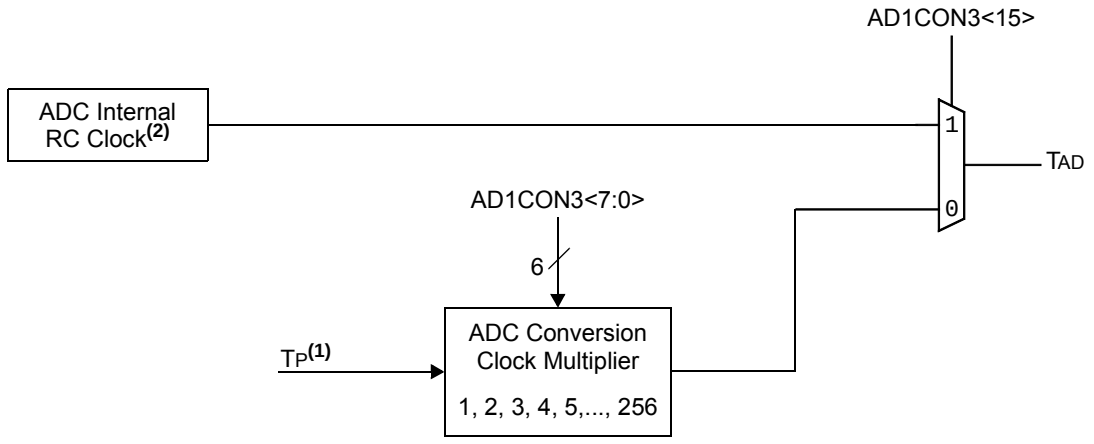
The 12-bit ADC configuration supports all the features listed above, with the exception of the following:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only one S&H amplifier in the 12-bit configuration; therefore, simultaneous sampling of multiple channels is not supported.

Depending on the particular device pinout, the ADC can have up to 16 analog input pins, designated AN0 through AN15. These analog inputs are shared with op amp inputs and outputs, comparator inputs, and external voltage references. When op amp/comparator functionality is enabled, or an external voltage reference is used, the analog input that shares that pin is no longer available. The actual number of analog input pins, op amps and external voltage reference input configuration depends on the specific device.

A block diagram of the ADC module is shown in Figure 23-1. Figure 23-2 provides a diagram of the ADC conversion clock period.

FIGURE 23-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM



Note 1: TP = 1/FP.

2: See the ADC electrical specifications in **Section 30.0 "Electrical Characteristics"** for the exact RC clock value.

REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB	—	—	CH0SB4(1)	CH0SB3(1)	CH0SB2(1)	CH0SB1(1)	CH0SB0(1)
bit 15							bit 8

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA	—	—	CH0SA4(1)	CH0SA3(1)	CH0SA2(1)	CH0SA1(1)	CH0SA0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CH0NB:** Channel 0 Negative Input Select for Sample MUXB bit
1 = Channel 0 negative input is AN1(1)
0 = Channel 0 negative input is VREFL

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **CH0SB<4:0>:** Channel 0 Positive Input Select for Sample MUXB bits(1)
11111 = Open; use this selection with CTMU capacitive and time measurement
11110 = Channel 0 positive input is connected to the CTMU temperature measurement diode (CTMU TEMP)
11101 = Reserved
11100 = Reserved
11011 = Reserved
11010 = Channel 0 positive input is the output of OA3/AN6(2,3)
11001 = Channel 0 positive input is the output of OA2/AN0(2)
11000 = Channel 0 positive input is the output of OA1/AN3(2)
10111 = Reserved
•
•
•
10000 = Reserved
01111 = Channel 0 positive input is AN15(3)
01110 = Channel 0 positive input is AN14(3)
01101 = Channel 0 positive input is AN13(3)
•
•
•
00010 = Channel 0 positive input is AN2(3)
00001 = Channel 0 positive input is AN1(3)
00000 = Channel 0 positive input is AN0(3)

bit 7 **CH0NA:** Channel 0 Negative Input Select for Sample MUXA bit
1 = Channel 0 negative input is AN1(1)
0 = Channel 0 negative input is VREFL

bit 6-5 **Unimplemented:** Read as '0'

Note 1: AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

3: See the **"Pin Diagrams"** section for the available analog channels for each device.

24.2 PTG Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

24.2.1 KEY RESOURCES

- **"Peripheral Trigger Generator"** (DS70669) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER (CONTINUED)

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Reference Select bit (VIN+ input)(1)
1 = VIN+ input connects to internal CVREFIN voltage
0 = VIN+ input connects to C4IN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Channel Select bits(1)
11 = VIN- input of comparator connects to OA3/AN6
10 = VIN- input of comparator connects to OA2/AN0
01 = VIN- input of comparator connects to OA1/AN3
00 = VIN- input of comparator connects to C4IN1-

Note 1: Inputs that are selected and not available will be tied to VSS. See the **"Pin Diagrams"** section for available inputs for each package.

TABLE 27-1: CONFIGURATION BYTE REGISTER MAP

File Name	Address	Device Memory Size (Kbytes)	Bits 23-8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0057EC	32	—	—	—	—	—	—	—	—	—
	00AFEC	64									
	0157EC	128									
	02AFEC	256									
	0557EC	512									
Reserved	0057EE	32	—	—	—	—	—	—	—	—	—
	00AFEE	64									
	0157EE	128									
	02AFEE	256									
	0557EE	512									
FICD	0057F0	32	—	Reserved(3)	—	JTAGEN	Reserved(2)	Reserved(3)	—	ICS<1:0>	
	00AFF0	64									
	0157F0	128									
	02AFF0	256									
	0557F0	512									
FPOR	0057F2	32	—	WDTWIN<1:0>		ALTI2C2	ALTI2C1	Reserved(3)	—	—	—
	00AFF2	64									
	0157F2	128									
	02AFF2	256									
	0557F2	512									
FWDT	0057F4	32	—	FWDTEN	WINDIS	PLLKEN	WDTPRE	WDTPOST<3:0>			
	00AFF4	64									
	0157F4	128									
	02AFF4	256									
	0557F4	512									
FOSC	0057F6	32	—	FCKSM<1:0>		IOL1WAY	—	—	OSCIOFNC	POSCMD<1:0>	
	00AFF6	64									
	0157F6	128									
	02AFF6	256									
	0557F6	512									
FOSCSEL	0057F8	32	—	IESO	PWMLOCK(1)	—	—	—	FNOSC<2:0>		
	00AFF8	64									
	0157F8	128									
	02AFF8	256									
	0557F8	512									
FGS	0057FA	32	—	—	—	—	—	—	—	GCP	GWRP
	00AFFA	64									
	0157FA	128									
	02AFFA	256									
	0557FA	512									
Reserved	0057FC	32	—	—	—	—	—	—	—	—	—
	00AFFC	64									
	0157FC	128									
	02AFFC	256									
	0557FC	512									
Reserved	057FFE	32	—	—	—	—	—	—	—	—	—
	00AFFE	64									
	0157FE	128									
	02AFFE	256									
	0557FE	512									

Legend: — = unimplemented, read as '1'.

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

2: This bit is reserved and must be programmed as '0'.

3: These bits are reserved and must be programmed as '1'.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles(2)	Status Flags Affected
53	NEG	NEG	Acc(1)	Negate Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		NEG	f	f = $\bar{f}$ + 1	1	1	C,DC,N,OV,Z
		NEG	f,WREG	WREG = $\bar{f}$ + 1	1	1	C,DC,N,OV,Z
		NEG	Ws,Wd	Wd = $\overline{Ws}$ + 1	1	1	C,DC,N,OV,Z
54	NOP	NOP		No Operation	1	1	None
		NOPR		No Operation	1	1	None
55	POP	POP	f	Pop f from Top-of-Stack (TOS)	1	1	None
		POP	Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
		POP.D	Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)	1	2	None
		POP.S		Pop Shadow Registers	1	1	All
56	PUSH	PUSH	f	Push f to Top-of-Stack (TOS)	1	1	None
		PUSH	Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
		PUSH.D	Wns	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None
		PUSH.S		Push Shadow Registers	1	1	None
57	PWRSAV	PWRSAV	#lit1	Go into Sleep or Idle mode	1	1	WDTO,Sleep
58	RCALL	RCALL	Expr	Relative Call	1	4	SFA
		RCALL	Wn	Computed Call	1	4	SFA
59	REPEAT	REPEAT	#lit15	Repeat Next Instruction lit15 + 1 times	1	1	None
		REPEAT	Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
60	RESET	RESET		Software device Reset	1	1	None
61	RETFIE	RETFIE		Return from interrupt	1	6 (5)	SFA
62	RETLW	RETLW	#lit10,Wn	Return with literal in Wn	1	6 (5)	SFA
63	RETURN	RETURN		Return from Subroutine	1	6 (5)	SFA
64	RLC	RLC	f	f = Rotate Left through Carry f	1	1	C,N,Z
		RLC	f,WREG	WREG = Rotate Left through Carry f	1	1	C,N,Z
		RLC	Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C,N,Z
65	RLNC	RLNC	f	f = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	f,WREG	WREG = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N,Z
66	RRC	RRC	f	f = Rotate Right through Carry f	1	1	C,N,Z
		RRC	f,WREG	WREG = Rotate Right through Carry f	1	1	C,N,Z
		RRC	Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C,N,Z
67	RRNC	RRNC	f	f = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	f,WREG	WREG = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	Ws,Wd	Wd = Rotate Right (No Carry) Ws	1	1	N,Z
68	SAC	SAC	Acc,#Slit4,Wdo(1)	Store Accumulator	1	1	None
		SAC.R	Acc,#Slit4,Wdo(1)	Store Rounded Accumulator	1	1	None
69	SE	SE	Ws,Wnd	Wnd = sign-extended Ws	1	1	C,N,Z
70	SETM	SETM	f	f = 0xFFFF	1	1	None
		SETM	WREG	WREG = 0xFFFF	1	1	None
		SETM	Ws	Ws = 0xFFFF	1	1	None
71	SFTAC	SFTAC	Acc,Wn(1)	Arithmetic Shift Accumulator by (Wn)	1	1	OA,OB,OAB, SA,SB,SAB
		SFTAC	Acc,#Slit6(1)	Arithmetic Shift Accumulator by Slit6	1	1	OA,OB,OAB, SA,SB,SAB

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 30-7: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions**		
Idle Current (IIDLE)(1)						
DC40d	3	8	mA	-40°C	3.3V	10 MIPS
DC40a	3	8	mA	+25°C		
DC40b	3	8	mA	+85°C		
DC40c	3	8	mA	+125°C		
DC42d	6	12	mA	-40°C	3.3V	20 MIPS
DC42a	6	12	mA	+25°C		
DC42b	6	12	mA	+85°C		
DC42c	6	12	mA	+125°C		
DC44d	11	18	mA	-40°C	3.3V	40 MIPS
DC44a	11	18	mA	+25°C		
DC44b	11	18	mA	+85°C		
DC44c	11	18	mA	+125°C		
DC45d	17	27	mA	-40°C	3.3V	60 MIPS
DC45a	17	27	mA	+25°C		
DC45b	17	27	mA	+85°C		
DC45c	17	27	mA	+125°C		
DC46d	20	35	mA	-40°C	3.3V	70 MIPS
DC46a	20	35	mA	+25°C		
DC46b	20	35	mA	+85°C		

Note 1: Base Idle current (IIDLE) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

FIGURE 30-12: QEA/QEB INPUT CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

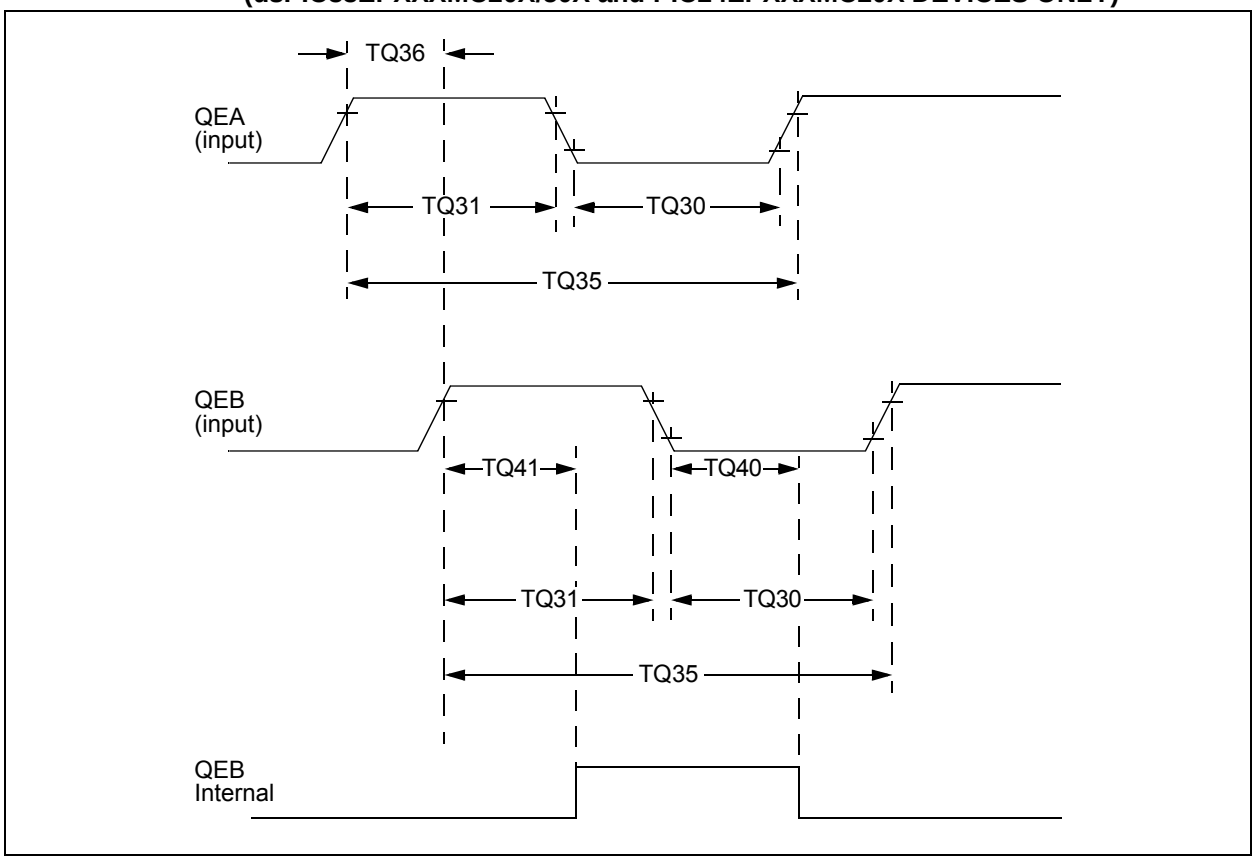


TABLE 30-31: QUADRATURE DECODER TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

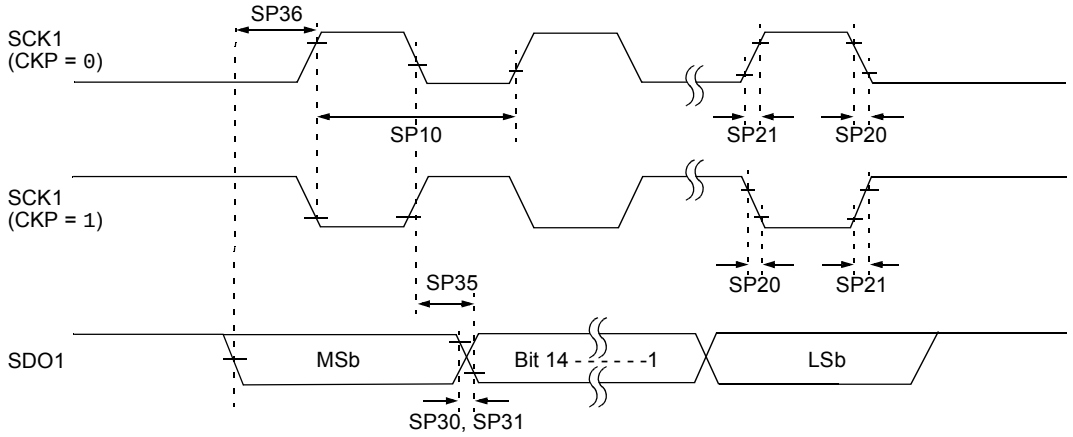
AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Symbol**	**Characteristic(1)**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
TQ30	TQUL	Quadrature Input Low Time	6 TCY	—	ns	
TQ31	TQUH	Quadrature Input High Time	6 TCY	—	ns	
TQ35	TQUIN	Quadrature Input Period	12 TCY	—	ns	
TQ36	TQUP	Quadrature Phase Period	3 TCY	—	ns	
TQ40	TQUFL	Filter Time to Recognize Low, with Digital Filter	3 * N * TCY	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 3)**
TQ41	TQUFH	Filter Time to Recognize High, with Digital Filter	3 * N * TCY	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 3)**

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: N = Index Channel Digital Filter Clock Divide Select bits. Refer to **"Quadrature Encoder Interface (QEI)"** (DS70601) in the "*dsPIC33/PIC24 Family Reference Manual*". Please see the Microchip web site for the latest family reference manual sections.

FIGURE 30-23: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-42: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCK1 Frequency	—	—	15	MHz	**(Note 3)**
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdiV2scH, TdiV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

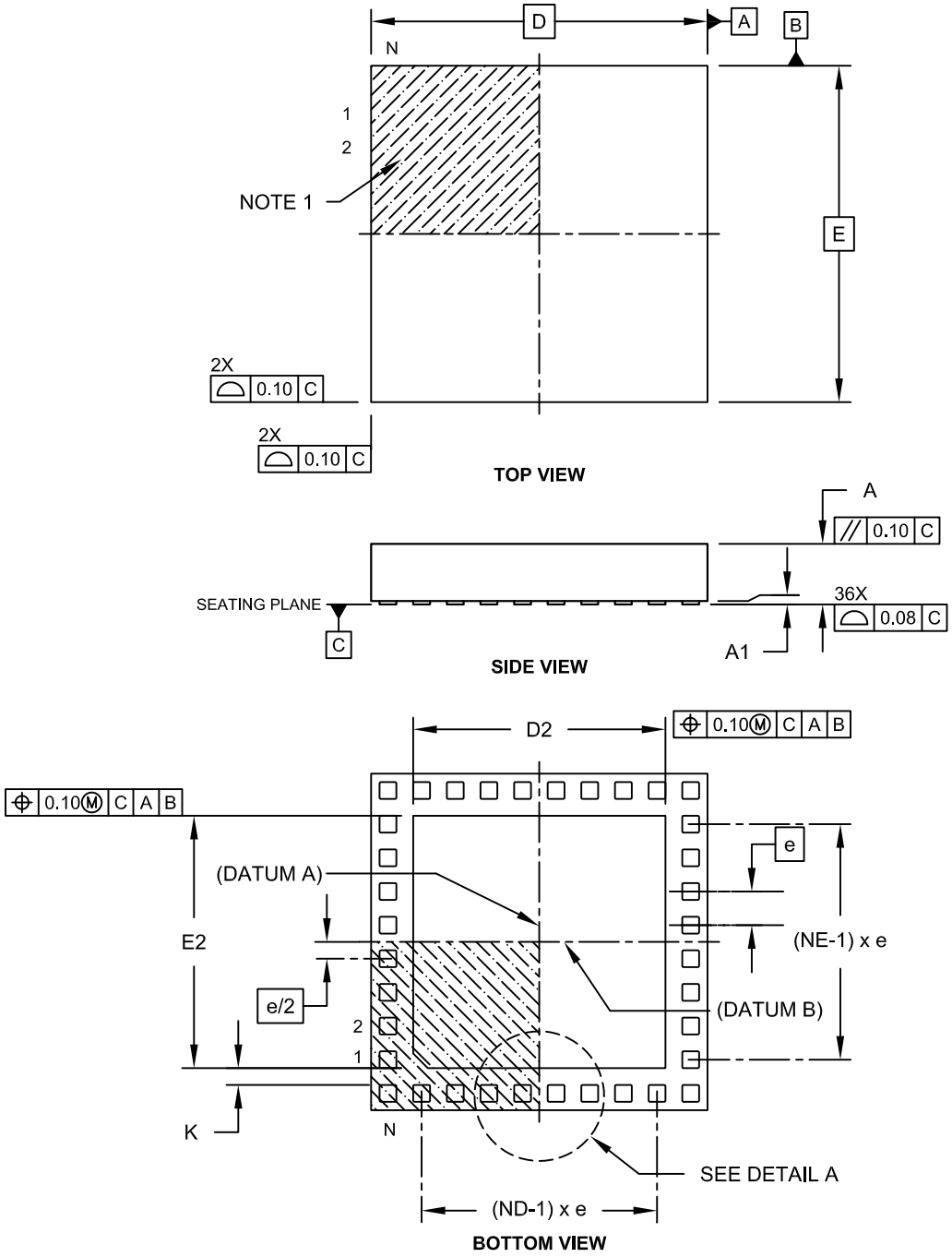
2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-187C Sheet 1 of 2