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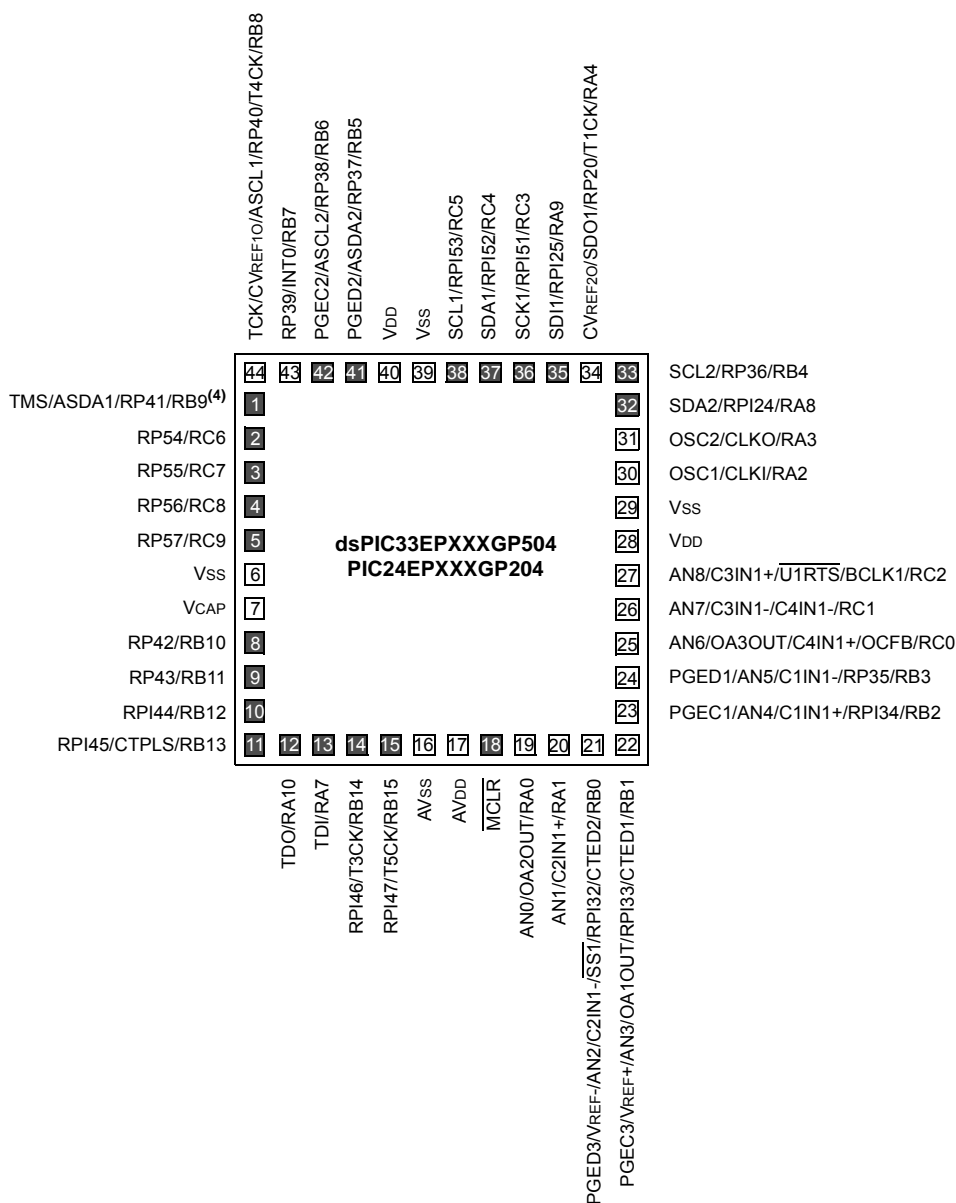
#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (10.7K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc504-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc504-i-pt</a>

## Pin Diagrams (Continued)

44-Pin VTLA<sup>(1,2,3)</sup>

■ = Pins are up to 5V tolerant



- Note 1:** The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
- Note 4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS**

Pin Name <sup>(4)</sup>	Pin Type	Buffer Type	PPS	Description
AN0-AN15	I	Analog	No	Analog input channels.
CLKI	I	ST/ CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/ CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
REFCLKO	O	—	Yes	Reference clock output.
IC1-IC4	I	ST	Yes	Capture Inputs 1 through 4.
OCFA	I	ST	Yes	Compare Fault A input (for Compare channels).
OCFB	I	ST	No	Compare Fault B input (for Compare channels).
OC1-OC4	O	—	Yes	Compare Outputs 1 through 4.
INT0	I	ST	No	External Interrupt 0.
INT1	I	ST	Yes	External Interrupt 1.
INT2	I	ST	Yes	External Interrupt 2.
RA0-RA4, RA7-RA12	I/O	ST	No	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port.
RC0-RC13, RC15	I/O	ST	No	PORTC is a bidirectional I/O port.
RD5, RD6, RD8	I/O	ST	No	PORTD is a bidirectional I/O port.
RE12-RE15	I/O	ST	No	PORTE is a bidirectional I/O port.
RF0, RF1	I/O	ST	No	PORTF is a bidirectional I/O port.
RG6-RG9	I/O	ST	No	PORTG is a bidirectional I/O port.
T1CK	I	ST	No	Timer1 external clock input.
T2CK	I	ST	Yes	Timer2 external clock input.
T3CK	I	ST	No	Timer3 external clock input.
T4CK	I	ST	No	Timer4 external clock input.
T5CK	I	ST	No	Timer5 external clock input.
CTPLS	O	ST	No	CTMU pulse output.
CTED1	I	ST	No	CTMU External Edge Input 1.
CTED2	I	ST	No	CTMU External Edge Input 2.
U1CTS	I	ST	No	UART1 Clear-To-Send.
U1RTS	O	—	No	UART1 Ready-To-Send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
BCLK1	O	ST	No	UART1 IrDA <sup>®</sup> baud clock output.

**Legend:** CMOS = CMOS compatible input or output      Analog = Analog input      P = Power  
ST = Schmitt Trigger input with CMOS levels      O = Output      I = Input  
PPS = Peripheral Pin Select      TTL = TTL input buffer

- Note 1:** This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- 2:** This pin is available on dsPIC33EPXXXGP/MC50X devices only.
- 3:** This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 “High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”** for more information.
- 4:** Not all pins are available in all packages variants. See the **“Pin Diagrams”** section for pin availability.
- 5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

**TABLE 4-17: I2C1 AND I2C2 REGISTER MAP**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
I2C1RCV	0200	—	—	—	—	—	—	—	—	I2C1 Receive Register									0000
I2C1TRN	0202	—	—	—	—	—	—	—	—	I2C1 Transmit Register									00FF
I2C1BRG	0204	—	—	—	—	—	—	—	Baud Rate Generator										0000
I2C1CON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000	
I2C1STAT	0208	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000	
I2C1ADD	020A	—	—	—	—	—	—	I2C1 Address Register											0000
I2C1MSK	020C	—	—	—	—	—	—	I2C1 Address Mask											0000
I2C2RCV	0210	—	—	—	—	—	—	—	—	I2C2 Receive Register									0000
I2C2TRN	0212	—	—	—	—	—	—	—	—	I2C2 Transmit Register									00FF
I2C2BRG	0214	—	—	—	—	—	—	—	Baud Rate Generator										0000
I2C2CON	0216	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000	
I2C2STAT	0218	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000	
I2C2ADD	021A	—	—	—	—	—	—	I2C2 Address Register											0000
I2C2MSK	021C	—	—	—	—	—	—	I2C2 Address Mask											0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-18: UART1 AND UART2 REGISTER MAP**

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMO	—	UEN<1:0>		WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL<1:0>		STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	0228	Baud Rate Generator Prescaler																0000
U2MODE	0230	UARTEN	—	USIDL	IREN	RTSMO	—	UEN<1:0>		WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL<1:0>		STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	—	—	—	—	—	—	—	UART2 Transmit Register									xxxx
U2RXREG	0236	—	—	—	—	—	—	—	UART2 Receive Register									0000
U2BRG	0238	Baud Rate Generator Prescaler																0000

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Allocating different Page registers for read and write access allows the architecture to support data movement between different pages in data memory. This is accomplished by setting the DSRPAG register value to the page from which you want to read, and configuring the DSWPAG register to the page to which it needs to be written. Data can also be moved from different PSV to EDS pages, by configuring the DSRPAG and DSWPAG registers to address PSV and EDS space, respectively. The data can be moved between pages by a single instruction.

When an EDS or PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the EDS or PSV pages can occur at the page boundaries when:

- The initial address prior to modification addresses an EDS or PSV page
- The EA calculation uses Pre-Modified or Post-Modified Register Indirect Addressing; however, this does not include Register Offset Addressing

In general, when an overflow is detected, the DSxPAG register is incremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. When an underflow is detected, the DSxPAG register is decremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. This creates a linear EDS and PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0, EDS and PSV spaces. Table 4-61 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA<15> bit is set and the DSxPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- Register Indirect with Register Offset Addressing
- Modulo Addressing
- Bit-Reversed Addressing

**TABLE 4-61: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0, EDS and PSV SPACE BOUNDARIES<sup>(2,3,4)</sup>**

O/U, R/W	Operation	Before			After		
		DSxPAG	DS EA<15>	Page Description	DSxPAG	DS EA<15>	Page Description
O, Read	[ ++Wn ] or [ Wn++ ]	DSRPAG = 0x1FF	1	EDS: Last page	DSRPAG = 0x1FF	0	See <b>Note 1</b>
O, Read		DSRPAG = 0x2FF	1	PSV: Last lsw page	DSRPAG = 0x300	1	PSV: First MSB page
O, Read		DSRPAG = 0x3FF	1	PSV: Last MSB page	DSRPAG = 0x3FF	0	See <b>Note 1</b>
O, Write		DSWPAG = 0x1FF	1	EDS: Last page	DSWPAG = 0x1FF	0	See <b>Note 1</b>
U, Read	[ --Wn ] or [ Wn-- ]	DSRPAG = 0x001	1	PSV page	DSRPAG = 0x001	0	See <b>Note 1</b>
U, Read		DSRPAG = 0x200	1	PSV: First lsw page	DSRPAG = 0x200	0	See <b>Note 1</b>
U, Read		DSRPAG = 0x300	1	PSV: First MSB page	DSRPAG = 0x2FF	1	PSV: Last lsw page

**Legend:** O = Overflow, U = Underflow, R = Read, W = Write

**Note 1:** The Register Indirect Addressing now addresses a location in the base Data Space (0x0000-0x8000).

**2:** An EDS access with DSxPAG = 0x000 will generate an address error trap.

**3:** Only reads from PS are supported using DSRPAG. An attempt to write to PS using DSWPAG will generate an address error trap.

**4:** Pseudo-Linear Addressing is not supported for large offsets.

## 6.0 RESETS

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “Reset” (DS70602) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal,  $\overline{\text{SYSRST}}$ . The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- $\overline{\text{MCLR}}$ : Master Clear Pin Reset
- SWR: RESET Instruction
- WDTO: Watchdog Timer Time-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
  - Illegal Opcode Reset
  - Uninitialized W Register Reset
  - Security Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the  $\overline{\text{SYSRST}}$  signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state and some are unaffected.

**Note:** Refer to the specific peripheral section or **Section 4.0 “Memory Organization”** of this manual for register Reset states.

All types of device Reset set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

A POR clears all the bits, except for the POR and BOR bits (RCON<1:0>), that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

**Note:** The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.

For all Resets, the default clock source is determined by the FNOSC<2:0> bits in the FOSCSEL Configuration register. The value of the FNOSC<2:0> bits is loaded into NOSC<2:0> (OSCCON<10:8>) on Reset, which in turn, initializes the system clock.

**FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM**

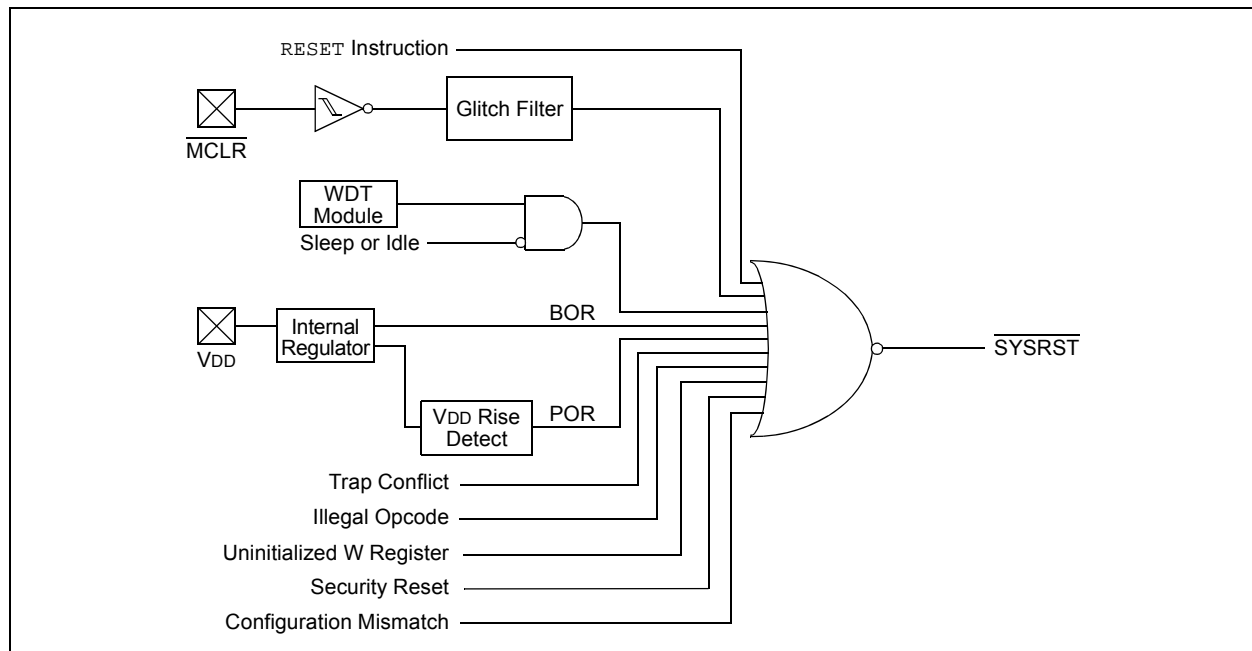


TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	1, 2
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	1
Low-Power RC Oscillator (LPRC)	Internal	xx	101	1
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	1
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	1
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)	Internal	xx	001	1
Fast RC Oscillator (FRC)	Internal	xx	000	1

**Note 1:** OSC2 pin function is determined by the OSCIOFNC Configuration bit.

**2:** This is the default oscillator mode for an unprogrammed (erased) device.

## 9.2 Oscillator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

### 9.2.1 KEY RESOURCES

- “**Oscillator**” (DS70580) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

### 16.3 PWMx Control Registers

**REGISTER 16-1: PTCN: PWMx TIME BASE CONTROL REGISTER**

R/W-0	U-0	R/W-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU <sup>(1)</sup>	SYNCPOL <sup>(1)</sup>	SYNCOEN <sup>(1)</sup>
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN <sup>(1)</sup>	SYNCSRC2 <sup>(1)</sup>	SYNCSRC1 <sup>(1)</sup>	SYNCSRC0 <sup>(1)</sup>	SEVTPS3 <sup>(1)</sup>	SEVTPS2 <sup>(1)</sup>	SEVTPS1 <sup>(1)</sup>	SEVTPS0 <sup>(1)</sup>
bit 7				bit 0			

<b>Legend:</b>	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

- bit 15      **PTEN:** PWMx Module Enable bit  
1 = PWMx module is enabled  
0 = PWMx module is disabled
- bit 14      **Unimplemented:** Read as '0'
- bit 13      **PTSIDL:** PWMx Time Base Stop in Idle Mode bit  
1 = PWMx time base halts in CPU Idle mode  
0 = PWMx time base runs in CPU Idle mode
- bit 12      **SESTAT:** Special Event Interrupt Status bit  
1 = Special event interrupt is pending  
0 = Special event interrupt is not pending
- bit 11      **SEIEN:** Special Event Interrupt Enable bit  
1 = Special event interrupt is enabled  
0 = Special event interrupt is disabled
- bit 10      **EIPU:** Enable Immediate Period Updates bit<sup>(1)</sup>  
1 = Active Period register is updated immediately  
0 = Active Period register updates occur on PWMx cycle boundaries
- bit 9      **SYNCPOL:** Synchronize Input and Output Polarity bit<sup>(1)</sup>  
1 = SYNCI1/SYNCO1 polarity is inverted (active-low)  
0 = SYNCI1/SYNCO1 is active-high
- bit 8      **SYNCOEN:** Primary Time Base Sync Enable bit<sup>(1)</sup>  
1 = SYNCO1 output is enabled  
0 = SYNCO1 output is disabled
- bit 7      **SYNCEN:** External Time Base Synchronization Enable bit<sup>(1)</sup>  
1 = External synchronization of primary time base is enabled  
0 = External synchronization of primary time base is disabled

**Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.

**2:** See **Section 24.0 “Peripheral Trigger Generator (PTG) Module”** for information on this selection.

## 17.1 QEI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

<p><b>Note:</b> In the event you are not able to access the product page using the link above, enter this URL in your browser: <a href="http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464">http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464</a></p>
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### 17.1.1 KEY RESOURCES

- **“Quadrature Encoder Interface”** (DS70601) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

**REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1**

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE <sup>(1)</sup>
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN <sup>(2)</sup>	CKP	MSTEN	SPRE2 <sup>(3)</sup>	SPRE1 <sup>(3)</sup>	SPRE0 <sup>(3)</sup>	PPRE1 <sup>(3)</sup>	PPRE0 <sup>(3)</sup>
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-13      **Unimplemented:** Read as '0'
- bit 12      **DISSCK:** Disable SCKx Pin bit (SPIx Master modes only)  
             1 = Internal SPIx clock is disabled, pin functions as I/O  
             0 = Internal SPIx clock is enabled
- bit 11      **DISSDO:** Disable SDOx Pin bit  
             1 = SDOx pin is not used by the module; pin functions as I/O  
             0 = SDOx pin is controlled by the module
- bit 10      **MODE16:** Word/Byte Communication Select bit  
             1 = Communication is word-wide (16 bits)  
             0 = Communication is byte-wide (8 bits)
- bit 9      **SMP:** SPIx Data Input Sample Phase bit  
             Master mode:  
             1 = Input data is sampled at end of data output time  
             0 = Input data is sampled at middle of data output time  
             Slave mode:  
             SMP must be cleared when SPIx is used in Slave mode.
- bit 8      **CKE:** SPIx Clock Edge Select bit<sup>(1)</sup>  
             1 = Serial output data changes on transition from active clock state to Idle clock state (refer to bit 6)  
             0 = Serial output data changes on transition from Idle clock state to active clock state (refer to bit 6)
- bit 7      **SSEN:** Slave Select Enable bit (Slave mode)<sup>(2)</sup>  
             1 =  $\overline{SSx}$  pin is used for Slave mode  
             0 =  $\overline{SSx}$  pin is not used by the module; pin is controlled by port function
- bit 6      **CKP:** Clock Polarity Select bit  
             1 = Idle state for clock is a high level; active state is a low level  
             0 = Idle state for clock is a low level; active state is a high level
- bit 5      **MSTEN:** Master Mode Enable bit  
             1 = Master mode  
             0 = Slave mode

- Note 1:** The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).  
**Note 2:** This bit must be cleared when FRMEN = 1.  
**Note 3:** Do not set both primary and secondary prescalers to the value of 1:1.

## 21.4 ECAN Control Registers

REGISTER 21-1: CxCTRL1: ECANx CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
—	—	CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0
bit 15						bit 8	

R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE2	OPMODE1	OPMODE0	—	CANCAP	—	—	WIN
bit 7						bit 0	

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

- bit 15-14      **Unimplemented:** Read as '0'
- bit 13      **CSIDL:** ECANx Stop in Idle Mode bit  
1 = Discontinues module operation when device enters Idle mode  
0 = Continues module operation in Idle mode
- bit 12      **ABAT:** Abort All Pending Transmissions bit  
1 = Signals all transmit buffers to abort transmission  
0 = Module will clear this bit when all transmissions are aborted
- bit 11      **CANCKS:** ECANx Module Clock (FCAN) Source Select bit  
1 = FCAN is equal to 2 \* FP  
0 = FCAN is equal to FP
- bit 10-8      **REQOP<2:0>:** Request Operation Mode bits  
111 = Set Listen All Messages mode  
110 = Reserved  
101 = Reserved  
100 = Set Configuration mode  
011 = Set Listen Only mode  
010 = Set Loopback mode  
001 = Set Disable mode  
000 = Set Normal Operation mode
- bit 7-5      **OPMODE<2:0>:** Operation Mode bits  
111 = Module is in Listen All Messages mode  
110 = Reserved  
101 = Reserved  
100 = Module is in Configuration mode  
011 = Module is in Listen Only mode  
010 = Module is in Loopback mode  
001 = Module is in Disable mode  
000 = Module is in Normal Operation mode
- bit 4      **Unimplemented:** Read as '0'
- bit 3      **CANCAP:** CAN Message Receive Timer Capture Event Enable bit  
1 = Enables input capture based on CAN message receive  
0 = Disables CAN capture
- bit 2-1      **Unimplemented:** Read as '0'
- bit 0      **WIN:** SFR Map Window Select bit  
1 = Uses filter window  
0 = Uses buffer window

**REGISTER 21-5: CxFIFO: ECANx FIFO STATUS REGISTER**

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FBP5	FBP4	FBP3	FBP2	FBP1	FBP0
bit 15							bit 8

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FNRB5	FNRB4	FNRB3	FNRB2	FNRB1	FNRB0
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **FBP<5:0>:** FIFO Buffer Pointer bits

011111 = RB31 buffer

011110 = RB30 buffer

•

•

•

000001 = TRB1 buffer

000000 = TRB0 buffer

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **FNRB<5:0>:** FIFO Next Read Buffer Pointer bits

011111 = RB31 buffer

011110 = RB30 buffer

•

•

•

000001 = TRB1 buffer

000000 = TRB0 buffer

**REGISTER 21-20: CxRXMnSID: ECANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER REGISTER (n = 0-2)**

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15						bit 8	

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	MIDE	—	EID17	EID16
bit 7						bit 0	

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-5      **SID<10:0>:** Standard Identifier bits  
1 = Includes bit, SIDx, in filter comparison  
0 = SIDx bit is a don't care in filter comparison
- bit 4      **Unimplemented:** Read as '0'
- bit 3      **MIDE:** Identifier Receive Mode bit  
1 = Matches only message types (standard or extended address) that correspond to EXIDE bit in the filter  
0 = Matches either standard or extended address message if filters match (i.e., if (Filter SID) = (Message SID) or if (Filter SID/EID) = (Message SID/EID))
- bit 2      **Unimplemented:** Read as '0'
- bit 1-0      **EID<17:16>:** Extended Identifier bits  
1 = Includes bit, EIDx, in filter comparison  
0 = EIDx bit is a don't care in filter comparison

**REGISTER 21-21: CxRXMnEID: ECANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER (n = 0-2)**

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 15						bit 8	

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
bit 7						bit 0	

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-0      **EID<15:0>:** Extended Identifier bits  
1 = Includes bit, EIDx, in filter comparison  
0 = EIDx bit is a don't care in filter comparison

## 23.4 ADC Control Registers

REGISTER 23-1: AD1CON1: ADC1 CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	ADDMA BM	—	AD12B	FORM1	FORM0
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC, HS	R/C-0, HC, HS
SSRC2	SSRC1	SSRC0	SSRCG	SIMS AM	ASAM	SAMP	DONE <sup>(3)</sup>
bit 7							bit 0

<b>Legend:</b>	HC = Hardware Clearable bit	HS = Hardware Settable bit	C = Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADON:** ADC1 Operating Mode bit

1 = ADC module is operating  
0 = ADC is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **ADSIDL:** ADC1 Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode  
0 = Continues module operation in Idle mode

bit 12 **ADDMA BM:** DMA Buffer Build Mode bit

1 = DMA buffers are written in the order of conversion; the module provides an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer  
0 = DMA buffers are written in Scatter/Gather mode; the module provides a Scatter/Gather address to the DMA channel, based on the index of the analog input and the size of the DMA buffer.

bit 11 **Unimplemented:** Read as '0'

bit 10 **AD12B:** ADC1 10-Bit or 12-Bit Operation Mode bit

1 = 12-bit, 1-channel ADC operation  
0 = 10-bit, 4-channel ADC operation

bit 9-8 **FORM<1:0>:** Data Output Format bits

For 10-Bit Operation:

11 = Signed fractional (DOUT = sddd dddd dd00 0000, where s = .NOT.d<9>)  
10 = Fractional (DOUT = dddd dddd dd00 0000)  
01 = Signed integer (DOUT = ssss sssd dddd dddd, where s = .NOT.d<9>)  
00 = Integer (DOUT = 0000 00dd dddd dddd)

For 12-Bit Operation:

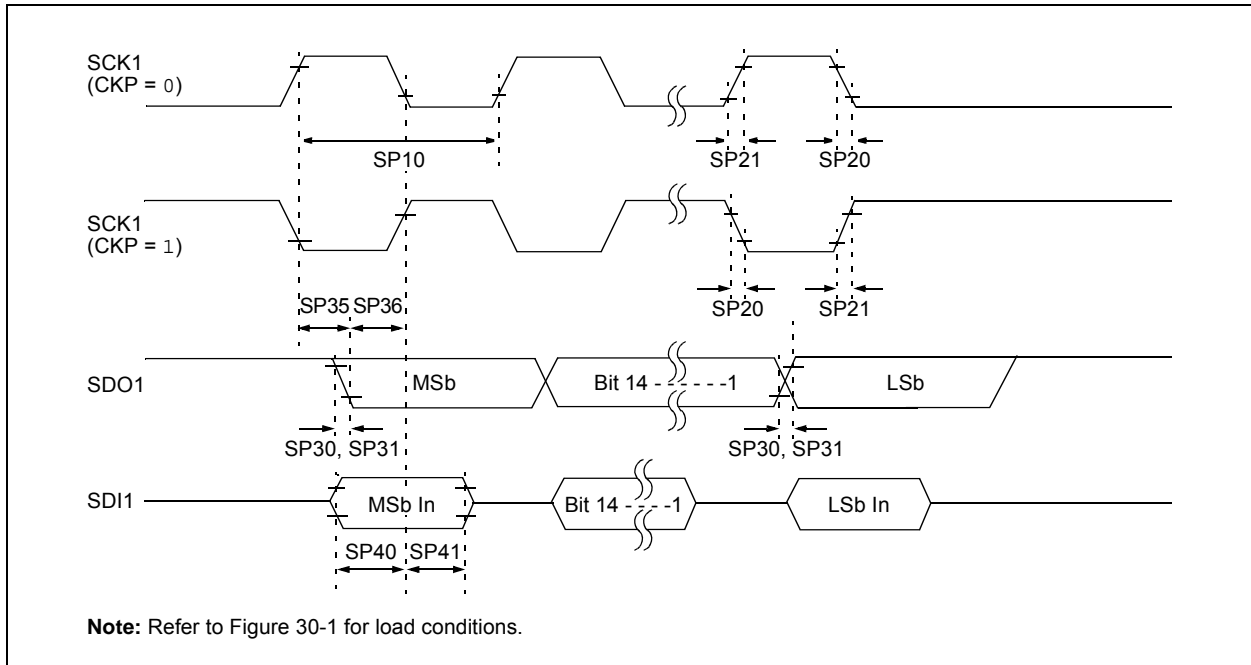
11 = Signed fractional (DOUT = sddd dddd dddd 0000, where s = .NOT.d<11>)  
10 = Fractional (DOUT = dddd dddd dddd 0000)  
01 = Signed integer (DOUT = ssss sddd dddd dddd, where s = .NOT.d<11>)  
00 = Integer (DOUT = 0000 dddd dddd dddd)

**Note 1:** See Section 24.0 “Peripheral Trigger Generator (PTG) Module” for information on this selection.

**2:** This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**3:** Do not clear the DONE bit in software if Auto-Sample is enabled (ASAM = 1).

**FIGURE 30-25: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)  
TIMING CHARACTERISTICS**



**TABLE 30-44: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)  
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	—	—	10	MHz	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (Note 3)
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V,  $+25^{\circ}\text{C}$  unless otherwise stated.

**3:** The minimum clock period for SCK1 is 100 ns. The clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.

TABLE 30-54: OP AMP/COMPARATOR VOLTAGE REFERENCE SETTling TIME SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 2): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
VR310	TSET	Settling Time	—	1	10	μs	(Note 1)

**Note 1:** Settling time is measured while CVRR = 1 and CVR<3:0> bits transition from '0000' to '1111'.

**2:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

TABLE 30-55: OP AMP/COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
VRD310	CVRES	Resolution	CVRSRC/24	—	CVRSRC/32	LSb	
VRD311	CVRAA	Absolute Accuracy <sup>(2)</sup>	—	±25	—	mV	CVRSRC = 3.3V
VRD313	CVRSRC	Input Reference Voltage	0	—	AVDD + 0.3	V	
VRD314	CVRROUT	Buffer Output Resistance <sup>(2)</sup>	—	1.5k	—	Ω	

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** Parameter is characterized but not tested in manufacturing.

TABLE 31-11: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature    -40°C ≤ TA ≤ +150°C					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
HF21	LPRC @ 32.768 kHz <sup>(1,2)</sup>						
	LPRC	-30	—	+30	%	-40°C ≤ TA ≤ +150°C	VDD = 3.0-3.6V

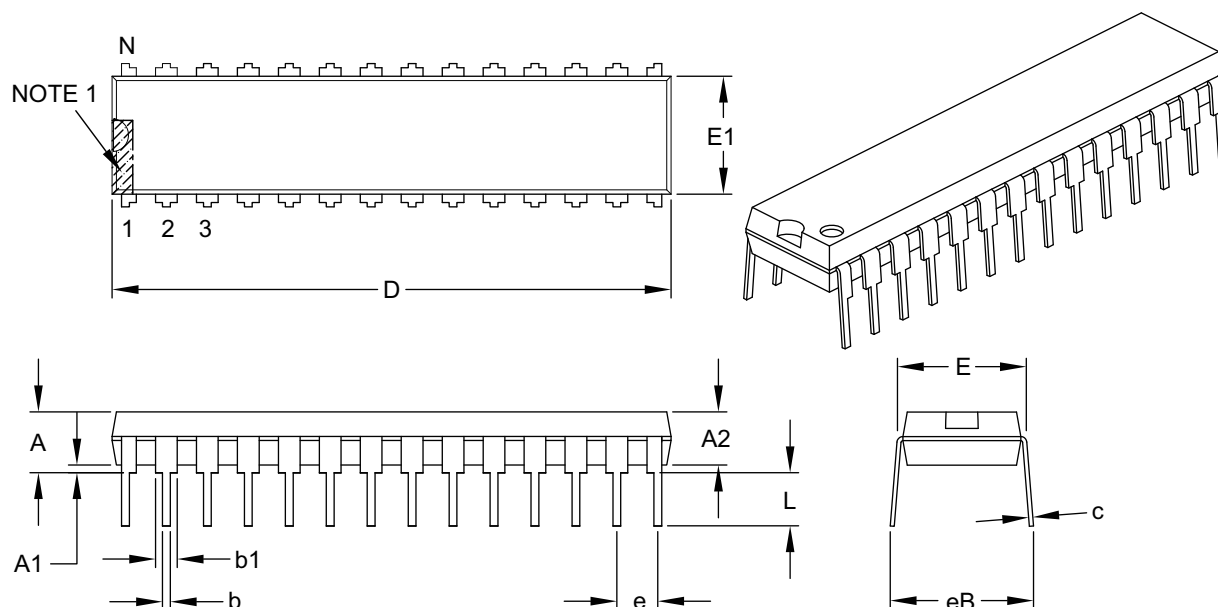
**Note 1:** Change of LPRC frequency as VDD changes.

**Note 2:** LPRC accuracy impacts the Watchdog Timer Time-out Period (TWDT). See **Section 27.5 “Watchdog Timer (WDT)”** for more information.

## 33.2 Package Details

### 28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

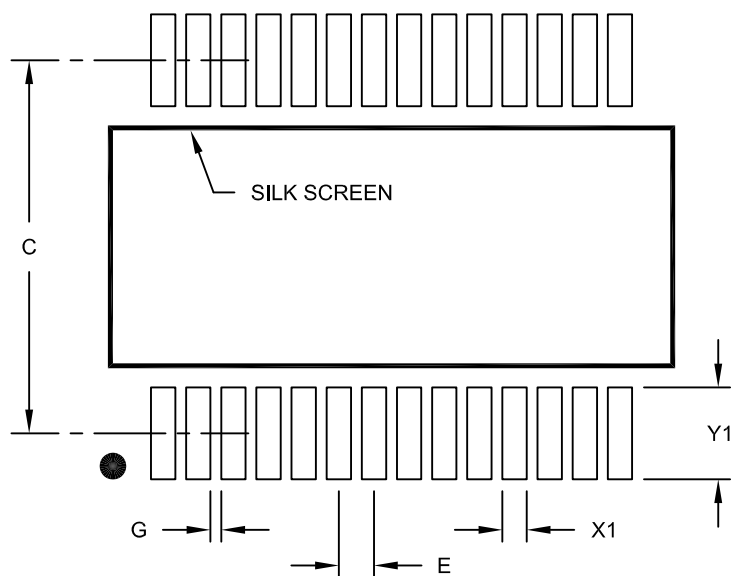
**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C	7.20		
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

**Revision D (December 2011)**

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

**TABLE A-3: MAJOR SECTION UPDATES**

Section Name	Update Description
<b>“16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High-Speed PWM, Op amps, and Advanced Analog”</b>	Removed the Analog Comparators column and updated the Op amps/Comparators column in Table 1 and Table 2.
<b>Section 21.0 “Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)”</b>	Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1).
<b>Section 30.0 “Electrical Characteristics”</b>	Updated the VBOR specifications and/or its related note in the following electrical characteristics tables: <ul style="list-style-type: none"><li>• Table 30-1</li><li>• Table 30-4</li><li>• Table 30-12</li><li>• Table 30-14</li><li>• Table 30-15</li><li>• Table 30-16</li><li>• Table 30-56</li><li>• Table 30-57</li><li>• Table 30-58</li><li>• Table 30-59</li><li>• Table 30-60</li></ul>

**Revision H (August 2013)**

This revision includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-6.

**TABLE A-6: MAJOR SECTION UPDATES**

Section Name	Update Description
<b>Cover Section</b>	<ul style="list-style-type: none"> <li>• Adds Peripheral Pin Select (PPS) to allow Digital Function Remapping and Change Notification Interrupts to Input/Output section</li> <li>• Adds heading information to 64-Pin TQFP</li> </ul>
<b>Section 4.0 “Memory Organization”</b>	<ul style="list-style-type: none"> <li>• Corrects Reset values for ANSELE, TRISF, TRISC, ANSELC and TRISA</li> <li>• Corrects address range from 0x2FFF to 0x7FFF</li> <li>• Corrects DSRPAG and DSWPAG (now 3 hex digits)</li> <li>• Changes Call Stack Frame from &lt;15:1&gt; to PC&lt;15:0&gt;</li> <li>• Word length in Figure 4-20 is changed to 50 words for clarity</li> </ul>
<b>Section 5.0 “Flash Program Memory”</b>	<ul style="list-style-type: none"> <li>• Corrects descriptions of NVM registers</li> </ul>
<b>Section 9.0 “Oscillator Configuration”</b>	<ul style="list-style-type: none"> <li>• Removes resistor from Figure 9-1</li> <li>• Adds Fast RC Oscillator with Divide-by-16 (FRCDIV16) row to Table 9-1</li> <li>• Removes incorrect information from ROI bit in Register 9-2</li> </ul>
<b>Section 14.0 “Input Capture”</b>	<ul style="list-style-type: none"> <li>• Changes 31 user-selectable Trigger/Sync interrupts to 19 user-selectable Trigger/Sync interrupts</li> <li>• Corrects ICTSEL&lt;12:10&gt; bits (now ICTSEL&lt;2:0&gt;)</li> </ul>
<b>Section 17.0 “Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”</b>	<ul style="list-style-type: none"> <li>• Corrects QCAPEN bit description</li> </ul>
<b>Section 19.0 “Inter-Integrated Circuit™ (I<sup>2</sup>C™)”</b>	<ul style="list-style-type: none"> <li>• Adds note to clarify that 100kbit/sec operation of I<sup>2</sup>C is not possible at high processor speeds</li> </ul>
<b>Section 22.0 “Charge Time Measurement Unit (CTMU)”</b>	<ul style="list-style-type: none"> <li>• Clarifies Figure 22-1 to accurately reflect peripheral behavior</li> </ul>
<b>Section 23.0 “10-Bit/12-Bit Analog-to-Digital Converter (ADC)”</b>	<ul style="list-style-type: none"> <li>• Correct Figure 23-1 (changes CH123x to CH123Sx)</li> </ul>
<b>Section 24.0 “Peripheral Trigger Generator (PTG) Module”</b>	<ul style="list-style-type: none"> <li>• Adds footnote to Register 24-1 (In order to operate with CVRSS=1, at least one of the comparator modules must be enabled).</li> </ul>
<b>Section 25.0 “Op Amp/Comparator Module”</b>	<ul style="list-style-type: none"> <li>• Adds note to Figure 25-3 (In order to operate with CVRSS=1, at least one of the comparator modules must be enabled)</li> <li>• Adds footnote to Register 25-2 (COE is not available when OPMODE (CMxCON&lt;10&gt;) = 1)</li> </ul>
<b>Section 27.0 “Special Features”</b>	<ul style="list-style-type: none"> <li>• Corrects the bit description for FNOSC&lt;2:0&gt;</li> </ul>
<b>Section 30.0 “Electrical Characteristics”</b>	<ul style="list-style-type: none"> <li>• Corrects 512K part power-down currents based on test data</li> <li>• Corrects WDT timing limits based on LPRC oscillator tolerance</li> </ul>
<b>Section 31.0 “High-Temperature Electrical Characteristics”</b>	<ul style="list-style-type: none"> <li>• Adds Table 31-5 (DC Characteristics: Idle Current (I<sub>IDLE</sub>))</li> </ul>