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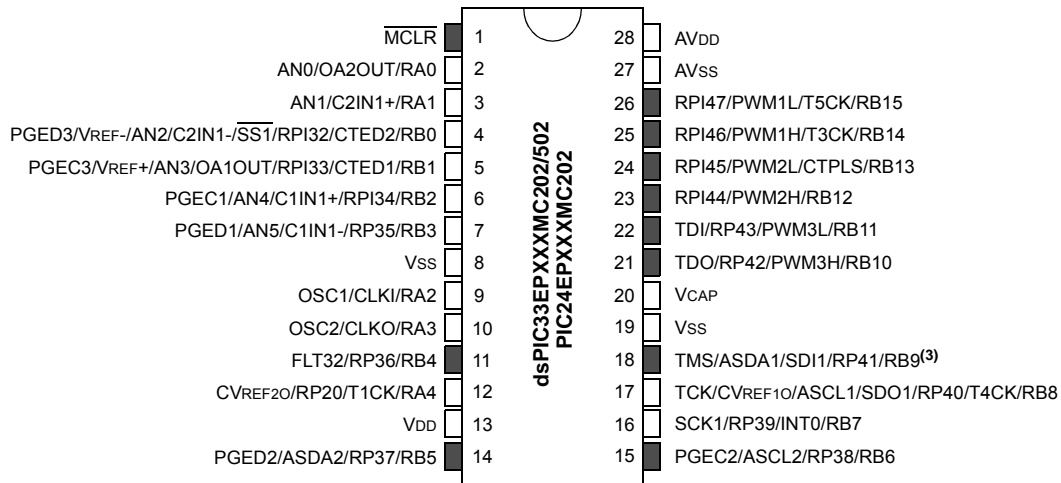
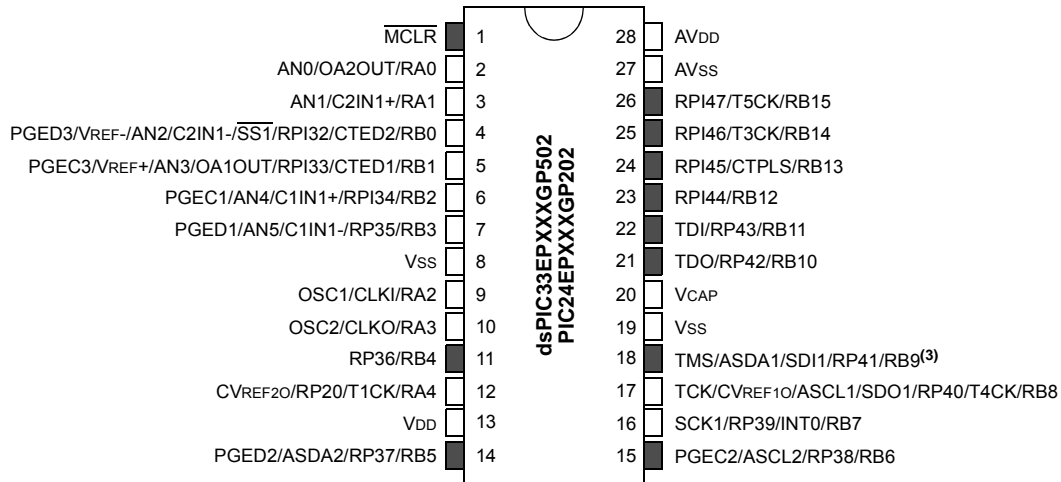
Details

| | |
|----------------------------|---|
| Product Status | Obsolete |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 60 MIPS |
| Connectivity | CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 32KB (10.7K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 9x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-TQFP |
| Supplier Device Package | 44-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep32mc504t-e-pt |

Pin Diagrams

28-Pin SPDIP/SOIC/SSOP^(1,2)

■ = Pins are up to 5V tolerant

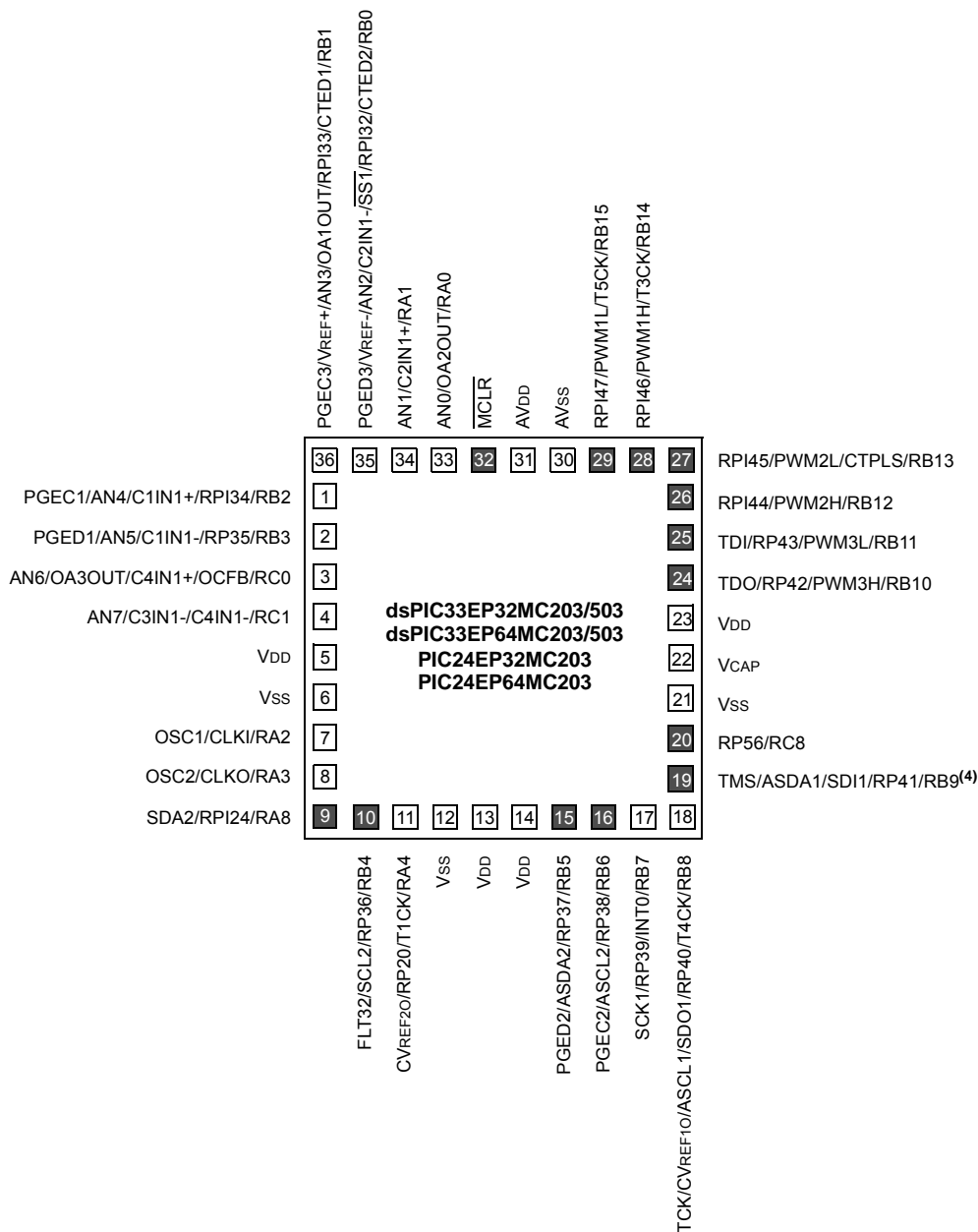


- Note 1:** The RPN/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

Pin Diagrams (Continued)

36-Pin VTLA^(1,2,3)

■ = Pins are up to 5V tolerant

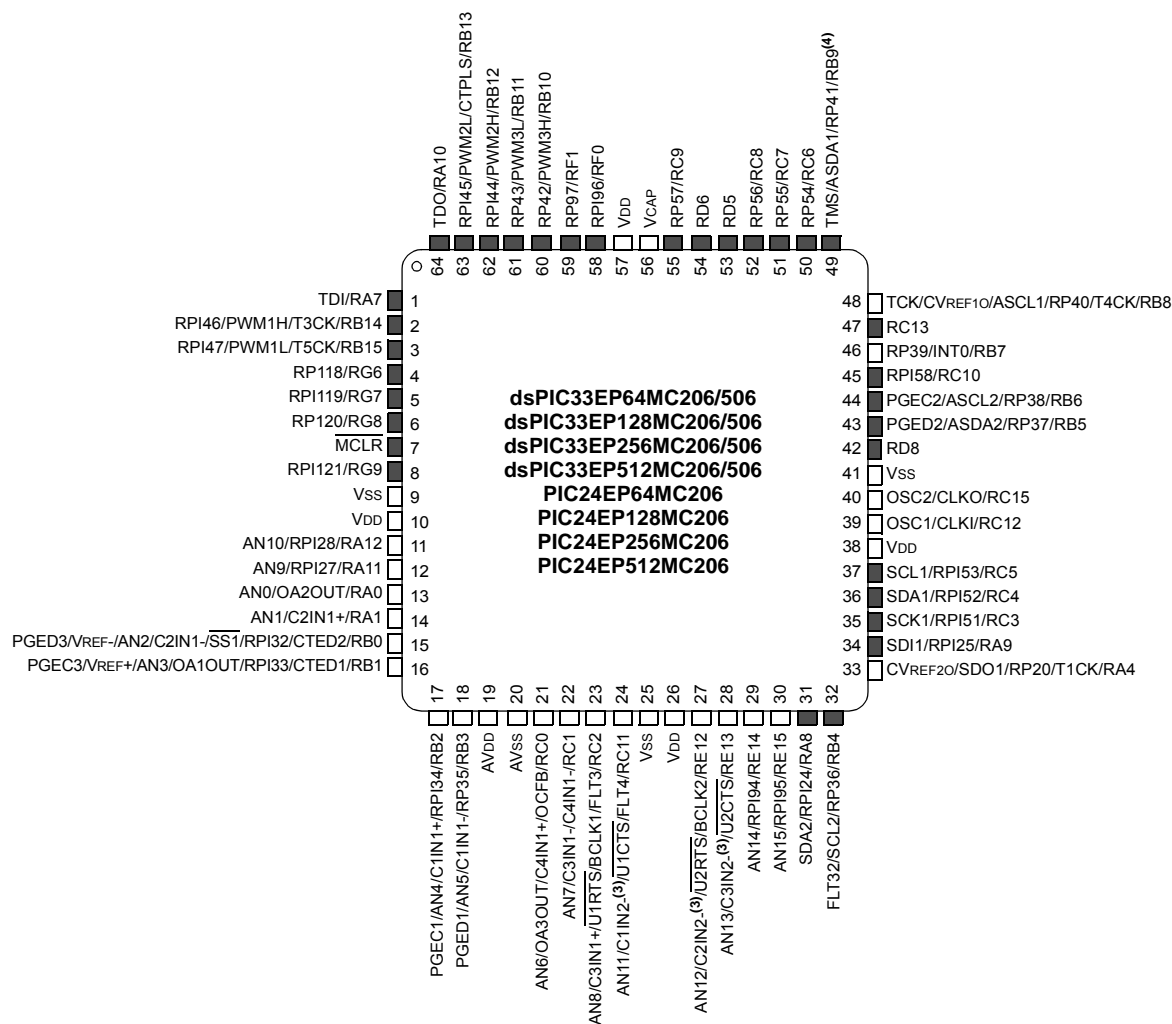


- Note**
- 1: The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
 - 3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
 - 4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

Pin Diagrams (Continued)

64-Pin TQFP^(1,2,3)

■ = Pins are up to 5V tolerant



- Note** 1: The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- 2: Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
- 3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
- 4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

| | |
|---------|---|
| bit 7-5 | IPL<2:0> : CPU Interrupt Priority Level Status bits ^(2,3) 111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled 110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12) 011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10) 001 = CPU Interrupt Priority Level is 1 (9) 000 = CPU Interrupt Priority Level is 0 (8) |
| bit 4 | RA : REPEAT Loop Active bit 1 = REPEAT loop in progress 0 = REPEAT loop not in progress |
| bit 3 | N : MCU ALU Negative bit 1 = Result was negative 0 = Result was non-negative (zero or positive) |
| bit 2 | OV : MCU ALU Overflow bit This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state. 1 = Overflow occurred for signed arithmetic (in this arithmetic operation) 0 = No overflow occurred |
| bit 1 | Z : MCU ALU Zero bit 1 = An operation that affects the Z bit has set it at some time in the past 0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result) |
| bit 0 | C : MCU ALU Carry/Borrow bit 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred |

- Note 1:** This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.
- 2:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
- 3:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- 4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

3.8 Arithmetic Logic Unit (ALU)

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X ALU is 16 bits wide, and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the “16-bit MCU and DSC Programmer's Reference Manual” (DS70157) for information on the SR bits affected by each instruction.

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.8.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier, the ALU supports unsigned, signed, or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.8.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned `DIV` instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.9 DSP Engine (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtractor (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are `ADD`, `SUB` and `NEG`.

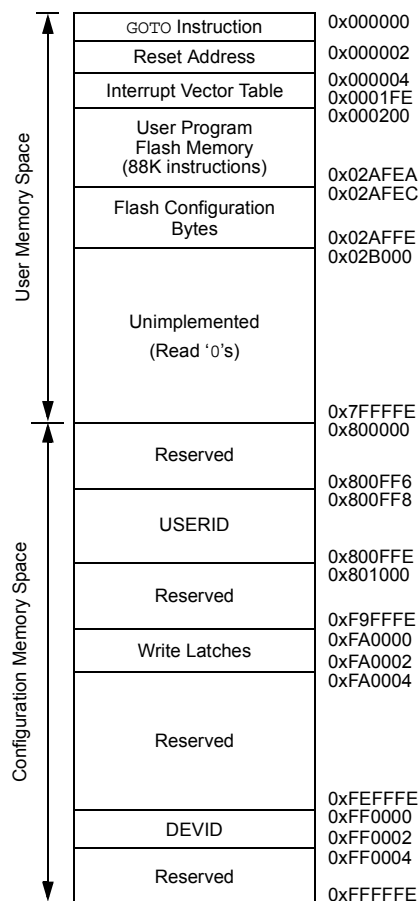
The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or integer DSP multiply (IF)
- Signed, unsigned or mixed-sign DSP multiply (US)
- Conventional or convergent rounding (RND)
- Automatic saturation on/off for ACCA (SATA)
- Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACCSAT)

TABLE 3-2: DSP INSTRUCTIONS SUMMARY

| Instruction | Algebraic Operation | ACC Write Back |
|-------------|-----------------------|----------------|
| CLR | $A = 0$ | Yes |
| ED | $A = (x - y)^2$ | No |
| EDAC | $A = A + (x - y)^2$ | No |
| MAC | $A = A + (x \cdot y)$ | Yes |
| MAC | $A = A + x^2$ | No |
| MOVSAC | No change in A | Yes |
| MPY | $A = x \cdot y$ | No |
| MPY | $A = x^2$ | No |
| MPY.N | $A = -x \cdot y$ | No |
| MSC | $A = A - x \cdot y$ | Yes |

FIGURE 4-4: PROGRAM MEMORY MAP FOR dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X AND PIC24EP256GP/MC20X DEVICES



Note: Memory areas are not shown to scale.

4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the `MUL` instruction), which writes the result to a register or register pair. The `MOV` instruction allows additional flexibility and can access the entire Data Space.

4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED

| Addressing Mode | Description |
|---|---|
| File Register Direct | The address of the file register is specified explicitly. |
| Register Direct | The contents of a register are accessed directly. |
| Register Indirect | The contents of Wn form the Effective Address (EA). |
| Register Indirect Post-Modified | The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value. |
| Register Indirect Pre-Modified | Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA. |
| Register Indirect with Register Offset (Register Indexed) | The sum of Wn and Wb forms the EA. |
| Register Indirect with Literal Offset | The sum of Wn and a literal forms the EA. |

12.0 TIMER1

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Timers**” (DS70362) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated in Asynchronous Counter mode from an external clock source
- The external clock input (T1CK) can optionally be synchronized to the internal device clock and the clock synchronization is performed after the prescaler

A block diagram of Timer1 is shown in Figure 12-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCy). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit setting for different operating modes are given in the Table 12-1.

TABLE 12-1: TIMER MODE SETTINGS

| Mode | TCS | TGATE | TSYNC |
|----------------------|-----|-------|-------|
| Timer | 0 | 0 | x |
| Gated Timer | 0 | 1 | x |
| Synchronous Counter | 1 | x | 1 |
| Asynchronous Counter | 1 | x | 0 |

FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM

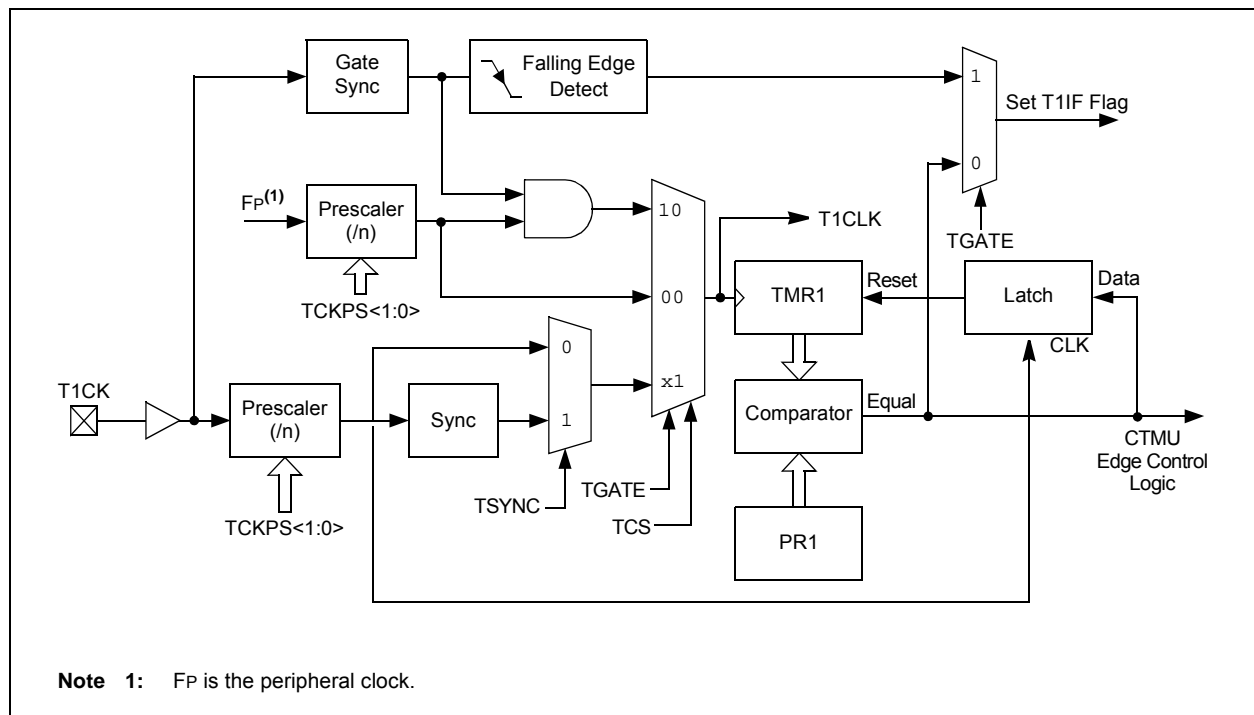
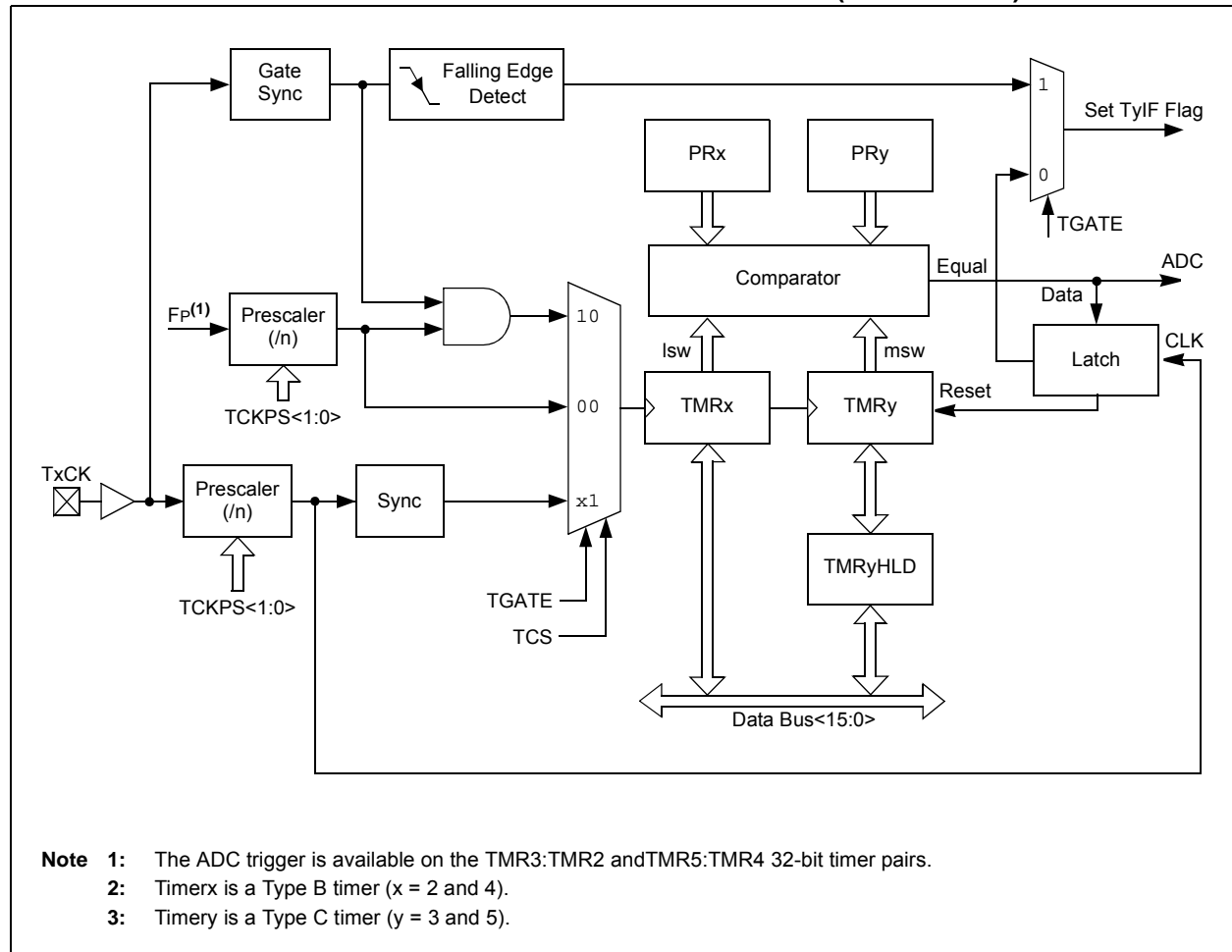


FIGURE 13-3: TYPE B/TIME C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)



13.1 Timerx/y Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

13.1.1 KEY RESOURCES

- “Timers” (DS70362) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools

REGISTER 16-13: IOCONx: PWMx I/O CONTROL REGISTER⁽²⁾ (CONTINUED)

- bit 1 **SWAP:** SWAP PWMxH and PWMxL Pins bit
 1 = PWMxH output signal is connected to PWMxL pins; PWMxL output signal is connected to PWMxH pins
 0 = PWMxH and PWMxL pins are mapped to their respective pins
- bit 0 **OSYNC:** Output Override Synchronization bit
 1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWMx period boundary
 0 = Output overrides via the OVDDAT<1:0> bits occur on the next CPU clock boundary

- Note 1:** These bits should not be changed after the PWMx module is enabled (PTEN = 1).
- 2:** If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

NOTES:

REGISTER 21-26: CxTRmnCON: ECANx TX/RX BUFFER mn CONTROL REGISTER
(m = 0,2,4,6; n = 1,3,5,7)

| | | | | | | | |
|--------|--------|---------|--------|--------|--------|---------|---------|
| R/W-0 | R-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| TXENn | TXABTn | TXLARBn | TXERRn | TXREQn | RTRENn | TXnPRI1 | TXnPRI0 |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----------------------|------------------------|-----------------------|--------|--------|---------|---------|
| R/W-0 | R-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| TXENm | TXABTm ⁽¹⁾ | TXLARBm ⁽¹⁾ | TXERRm ⁽¹⁾ | TXREQm | RTRENm | TXmPRI1 | TXmPRI0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-8 See Definition for bits<7:0>, Controls Buffer n
- bit 7 **TXENm:** TX/RX Buffer Selection bit
1 = Buffer TRBn is a transmit buffer
0 = Buffer TRBn is a receive buffer
- bit 6 **TXABTm:** Message Aborted bit⁽¹⁾
1 = Message was aborted
0 = Message completed transmission successfully
- bit 5 **TXLARBm:** Message Lost Arbitration bit⁽¹⁾
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent
- bit 4 **TXERRm:** Error Detected During Transmission bit⁽¹⁾
1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent
- bit 3 **TXREQm:** Message Send Request bit
1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent
0 = Clearing the bit to '0' while set requests a message abort
- bit 2 **RTRENm:** Auto-Remote Transmit Enable bit
1 = When a remote transmit is received, TXREQ will be set
0 = When a remote transmit is received, TXREQ will be unaffected
- bit 1-0 **TXmPRI<1:0>:** Message Transmission Priority bits
11 = Highest message priority
10 = High intermediate message priority
01 = Low intermediate message priority
00 = Lowest message priority

Note 1: This bit is cleared when TXREQ is set.

Note: The buffers, SID, EID, DLC, Data Field, and Receive Status registers are located in DMA RAM.

TABLE 24-1: PTG STEP COMMAND FORMAT (CONTINUED)

| bit 3-0 | Step Command | OPTION<3:0> | Option Description |
|---------|------------------------|-------------|--|
| | PTGCTRL ⁽¹⁾ | 0000 | Reserved. |
| | | 0001 | Reserved. |
| | | 0010 | Disable Step Delay Timer (PTGSD). |
| | | 0011 | Reserved. |
| | | 0100 | Reserved. |
| | | 0101 | Reserved. |
| | | 0110 | Enable Step Delay Timer (PTGSD). |
| | | 0111 | Reserved. |
| | | 1000 | Start and wait for the PTG Timer0 to match the Timer0 Limit Register. |
| | | 1001 | Start and wait for the PTG Timer1 to match the Timer1 Limit Register. |
| | | 1010 | Reserved. |
| | | 1011 | Wait for the software trigger bit transition from low-to-high before continuing (PTGSWT = 0 to 1). |
| | | 1100 | Copy contents of the Counter 0 register to the AD1CHS0 register. |
| | | 1101 | Copy contents of the Counter 1 register to the AD1CHS0 register. |
| | | 1110 | Copy contents of the Literal 0 register to the AD1CHS0 register. |
| | | 1111 | Generate triggers indicated in the Broadcast Trigger Enable register (PTGBTE). |
| | PTGADD ⁽¹⁾ | 0000 | Add contents of the PTGADJ register to the Counter 0 Limit register (PTGC0LIM). |
| | | 0001 | Add contents of the PTGADJ register to the Counter 1 Limit register (PTGC1LIM). |
| | | 0010 | Add contents of the PTGADJ register to the Timer0 Limit register (PTGT0LIM). |
| | | 0011 | Add contents of the PTGADJ register to the Timer1 Limit register (PTGT1LIM). |
| | | 0100 | Add contents of the PTGADJ register to the Step Delay Limit register (PTGSDLIM). |
| | | 0101 | Add contents of the PTGADJ register to the Literal 0 register (PTGL0). |
| | | 0110 | Reserved. |
| | | 0111 | Reserved. |
| | PTGCOPY ⁽¹⁾ | 1000 | Copy contents of the PTGHOLD register to the Counter 0 Limit register (PTGC0LIM). |
| | | 1001 | Copy contents of the PTGHOLD register to the Counter 1 Limit register (PTGC1LIM). |
| | | 1010 | Copy contents of the PTGHOLD register to the Timer0 Limit register (PTGT0LIM). |
| | | 1011 | Copy contents of the PTGHOLD register to the Timer1 Limit register (PTGT1LIM). |
| | | 1100 | Copy contents of the PTGHOLD register to the Step Delay Limit register (PTGSDLIM). |
| | | 1101 | Copy contents of the PTGHOLD register to the Literal 0 register (PTGL0). |
| | | 1110 | Reserved. |
| | | 1111 | Reserved. |

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 24-2 for the trigger output descriptions.

3: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

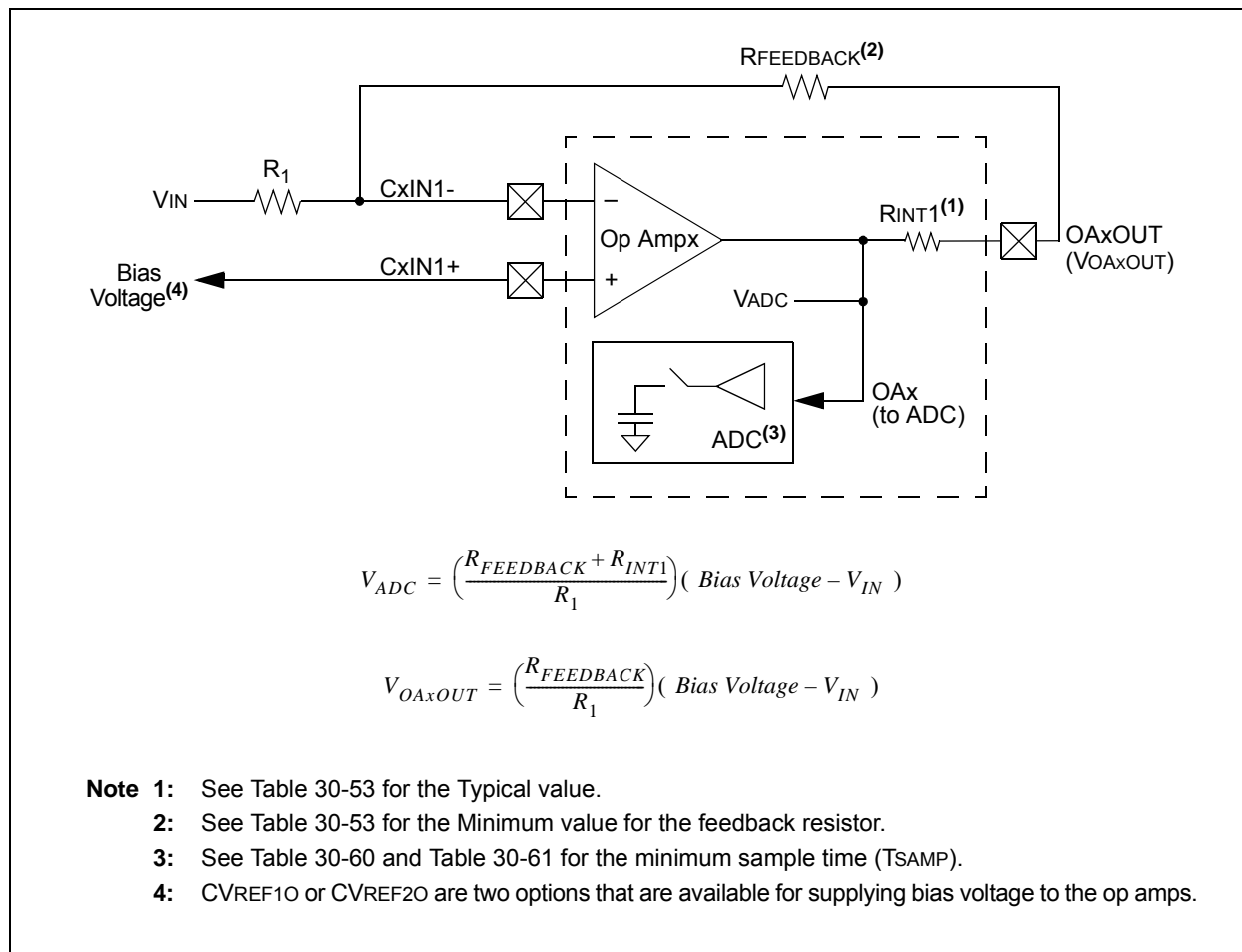
25.1 Op Amp Application Considerations

There are two configurations to take into consideration when designing with the op amp modules that are available in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices. Configuration A (see Figure 25-6) takes advantage of the internal connection to the ADC module to route the output of the op amp directly to the ADC for measurement. Configuration B (see Figure 25-7) requires that the designer externally route the output of the op amp (OAxOUT) to a separate analog input pin (ANy) on the device. Table 30-55 in **Section 30.0 “Electrical Characteristics”** describes the performance characteristics for the op amps, distinguishing between the two configuration types where applicable.

25.1.1 OP AMP CONFIGURATION A

Figure 25-6 shows a typical inverting amplifier circuit taking advantage of the internal connections from the op amp output to the input of the ADC. The advantage of this configuration is that the user does not need to consume another analog input (ANy) on the device, and allows the user to simultaneously sample all three op amps with the ADC module, if needed. However, the presence of the internal resistance, R_{INT1} , adds an error in the feedback path. Since R_{INT1} is an internal resistance, in relation to the op amp output (VO_{AXOUT}) and ADC internal connection (V_{ADC}), R_{INT1} must be included in the numerator term of the transfer function. See Table 30-53 in **Section 30.0 “Electrical Characteristics”** for the typical value of R_{INT1} . Table 30-60 and Table 30-61 in **Section 30.0 “Electrical Characteristics”** describe the minimum sample time (T_{SAMP}) requirements for the ADC module in this configuration. Figure 25-6 also defines the equations that should be used when calculating the expected voltages at points, V_{ADC} and VO_{AXOUT} .

FIGURE 25-6: OP AMP CONFIGURATION A



27.5 Watchdog Timer (WDT)

For dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

27.5.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a WDT Time-out period (TWDT), as shown in Parameter SY12 in Table 30-22.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

Note: The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

27.5.2 SLEEP AND IDLE MODES

If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes the device and code execution continues from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON<3,2>) needs to be cleared in software after the device wakes up.

27.5.3 ENABLING WDT

The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

27.5.4 WDT WINDOW

The Watchdog Timer has an optional Windowed mode, enabled by programming the WINDIS bit in the WDT Configuration register (FWDT<6>). In the Windowed mode (WINDIS = 0), the WDT should be cleared based on the settings in the programmable Watchdog Timer Window select bits (WDTWIN<1:0>).

FIGURE 27-2: WDT BLOCK DIAGRAM

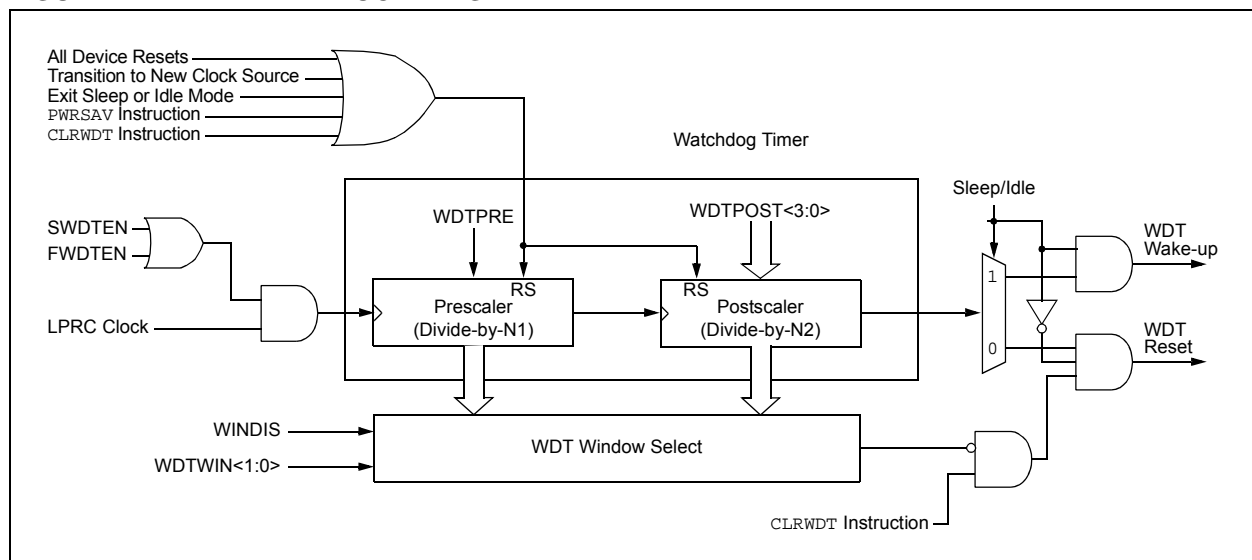


FIGURE 30-9: HIGH-SPEED PWMx MODULE FAULT TIMING CHARACTERISTICS
(dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

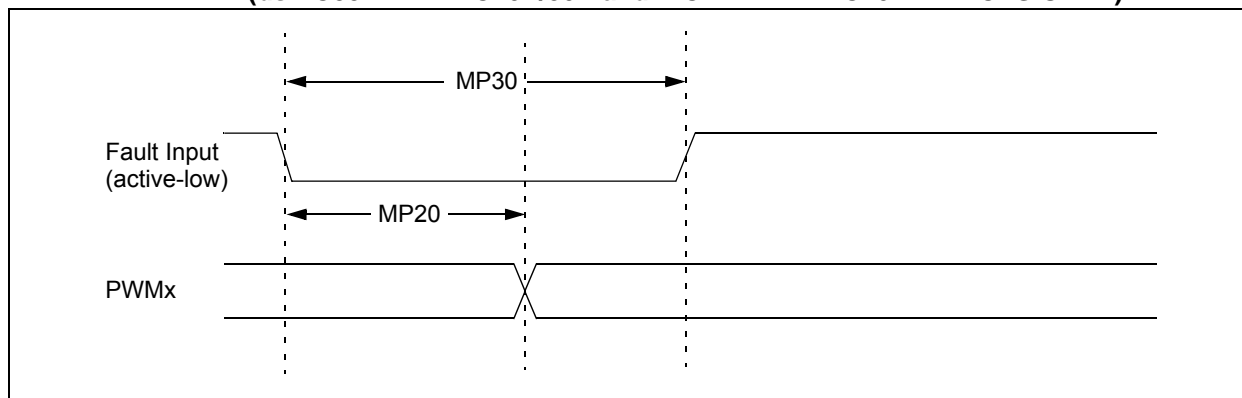


FIGURE 30-10: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS
(dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

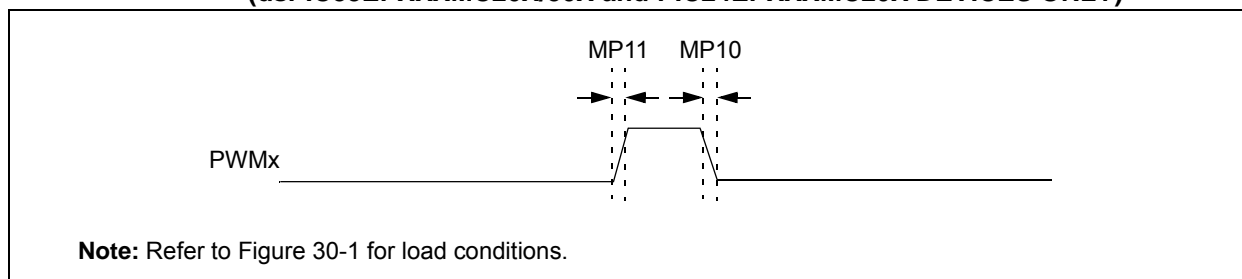


TABLE 30-29: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS
(dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|--------------------|-----------------|----------------------------------|---|------|------|-------|--------------------|
| Param No. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. | Max. | Units | Conditions |
| MP10 | TFPWM | PWMx Output Fall Time | — | — | — | ns | See Parameter DO32 |
| MP11 | TRPWM | PWMx Output Rise Time | — | — | — | ns | See Parameter DO31 |
| MP20 | T _{FD} | Fault Input ↓ to PWMx I/O Change | — | — | 15 | ns | |
| MP30 | T _{FH} | Fault Input Pulse Width | 15 | — | — | ns | |

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 30-58: ADC MODULE SPECIFICATIONS (12-BIT MODE)

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽¹⁾ Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|-----------------------------------|--------|---|--|------|------|-------|------------------------------|
| Param No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Conditions |
| ADC Accuracy (12-Bit Mode) | | | | | | | |
| AD20a | Nr | Resolution | 12 Data Bits | | | bits | |
| AD21a | INL | Integral Nonlinearity | -2.5 | — | 2.5 | LSb | -40°C ≤ TA ≤ +85°C (Note 2) |
| | | | -5.5 | — | 5.5 | LSb | +85°C < TA ≤ +125°C (Note 2) |
| AD22a | DNL | Differential Nonlinearity | -1 | — | 1 | LSb | -40°C ≤ TA ≤ +85°C (Note 2) |
| | | | -1 | — | 1 | LSb | +85°C < TA ≤ +125°C (Note 2) |
| AD23a | GERR | Gain Error ⁽³⁾ | -10 | — | 10 | LSb | -40°C ≤ TA ≤ +85°C (Note 2) |
| | | | -10 | — | 10 | LSb | +85°C < TA ≤ +125°C (Note 2) |
| AD24a | EOFF | Offset Error | -5 | — | 5 | LSb | -40°C ≤ TA ≤ +85°C (Note 2) |
| | | | -5 | — | 5 | LSb | +85°C < TA ≤ +125°C (Note 2) |
| AD25a | — | Monotonicity | — | — | — | — | Guaranteed |
| Dynamic Performance (12-Bit Mode) | | | | | | | |
| AD30a | THD | Total Harmonic Distortion ⁽³⁾ | — | 75 | — | dB | |
| AD31a | SINAD | Signal to Noise and Distortion ⁽³⁾ | — | 68 | — | dB | |
| AD32a | SFDR | Spurious Free Dynamic Range ⁽³⁾ | — | 80 | — | dB | |
| AD33a | FNYQ | Input Signal Bandwidth ⁽³⁾ | — | 250 | — | kHz | |
| AD34a | ENOB | Effective Number of Bits ⁽³⁾ | 11.09 | 11.3 | — | bits | |

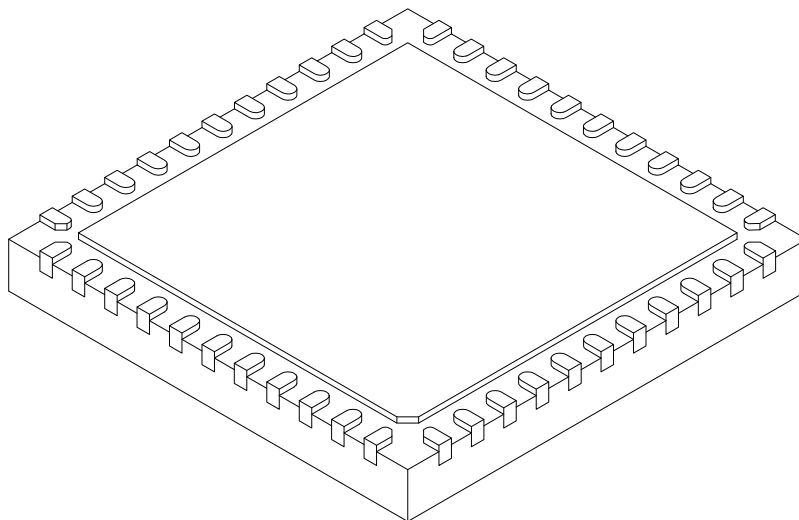
Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

3: Parameters are characterized but not tested in manufacturing.

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units | | MILLIMETERS | | |
|-------------------------|----|-------------|------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 44 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | 0.20 REF | | |
| Overall Width | E | 8.00 BSC | | |
| Exposed Pad Width | E2 | 6.25 | 6.45 | 6.60 |
| Overall Length | D | 8.00 BSC | | |
| Exposed Pad Length | D2 | 6.25 | 6.45 | 6.60 |
| Terminal Width | b | 0.20 | 0.30 | 0.35 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Terminal-to-Exposed-Pad | K | 0.20 | - | - |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M

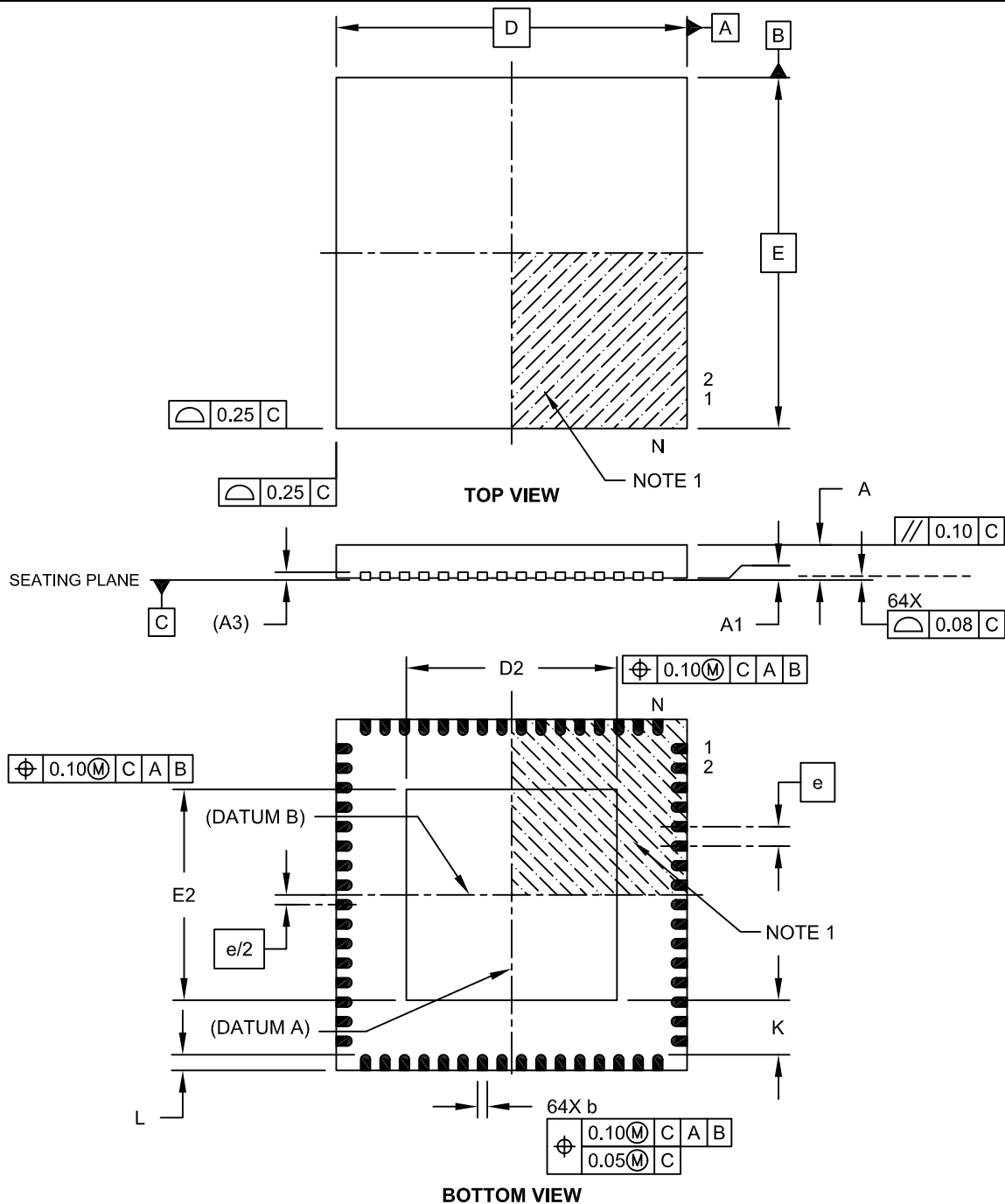
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension. usually without tolerance. for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2

**64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body
with 5.40 x 5.40 Exposed Pad [QFN]**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-154A Sheet 1 of 2

TABLE A-5: MAJOR SECTION UPDATES (CONTINUED)

| Section Name | Update Description |
|---|---|
| Section 30.0 “Electrical Characteristics” | <ul style="list-style-type: none"> • Throughout: qualifies all footnotes relating to the operation of analog modules below VDDMIN (replaces “will have” with “may have”) • Throughout: changes all references of SPI timing parameter symbol “TscP” to “FscP” • Table 30-1: changes VDD range to 3.0V to 3.6V • Table 30-4: removes Parameter DC12 (RAM Retention Voltage) • Table 30-7: updates Maximum values at 10 and 20 MIPS • Table 30-8: adds Maximum IPD values, and removes all ΔI_{WDT} entries • Adds new Table 30-9 (Watchdog Timer Delta Current) with consolidated values removed from Table 30-8. All subsequent tables are renumbered accordingly. • Table 30-10: adds footnote for all parameters for 1:2 Doze ratio • Table 30-11: <ul style="list-style-type: none"> - changes Minimum and Maximum values for D120 and D130 - adds Minimum and Maximum values for D131 - adds Minimum and Maximum values for D150 through D156, and removes Typical values • Table 30-12: <ul style="list-style-type: none"> - reformats table for readability - changes IOL conditions for DO10 • Table 30-14: adds footnote to D135 • Table 30-17: changes Minimum and Maximum values for OS30 • Table 30-19: <ul style="list-style-type: none"> - splits temperature range and adds new values for F20a - reduces temperature range for F20b to extended temperatures only • Table 30-20: <ul style="list-style-type: none"> - splits temperature range and adds new values for F21a - reduces temperature range for F20b to extended temperatures only • Table 30-53: <ul style="list-style-type: none"> - adds Maximum value to CM30 - adds footnote (“Parameter characterized...”) to multiple parameters • Table 30-55: adds Minimum and Maximum values for all CTMUI specifications, and removes Typical values • Table 30-57: adds new footnote to AD09 • Table 30-58: <ul style="list-style-type: none"> - removes all specifications for accuracy with external voltage references - removes Typical values for AD23a and AD24a - replaces Minimum and Maximum values for AD21a, AD22a, AD23a and AD24a with new values, split by Industrial and Extended temperatures - removes Maximum value of AD30 - removes Minimum values from AD31a and AD32a - adds or changes Typical values for AD30, AD31a, AD32a and AD33a • Table 30-59: <ul style="list-style-type: none"> - removes all specifications for accuracy with external voltage references - removes Maximum value of AD30 - removes Typical values for AD23b and AD24b - replaces Minimum and Maximum values for AD21b, AD22b, AD23b and AD24b with new values, split by Industrial and Extended temperatures - removes Minimum and Maximum values from AD31b, AD32b, AD33b and AD34b - adds or changes Typical values for AD30, AD31a, AD32a and AD33a • Table 30-61: Adds footnote to AD51 |
| Section 32.0 “DC and AC Device Characteristics Graphs” | <ul style="list-style-type: none"> • Updates Figure 32-6 (Typical IDD @ 3.3V) with individual current vs. processor speed curves for the different program memory sizes |
| Section 33.0 “Packaging Information” | <ul style="list-style-type: none"> • Replaces drawing C04-149C (64-pin QFN, 7.15 x 7.15 exposed pad) with C04-154A (64-pin QFN, 5.4 x 5.4 exposed pad) |