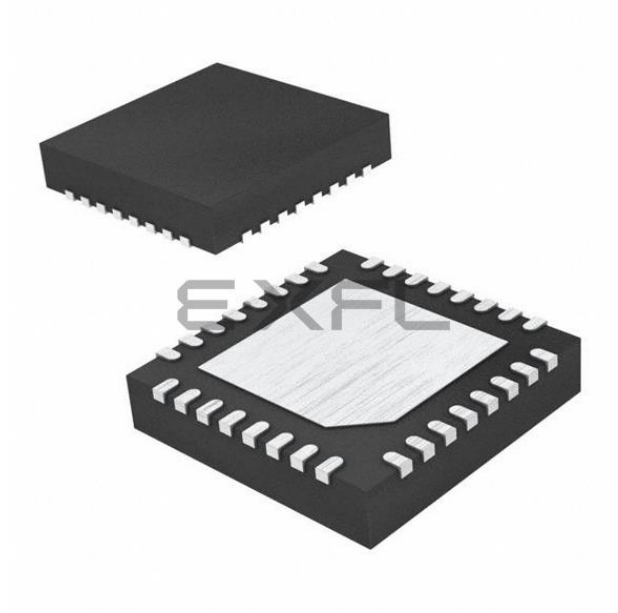
# Microchip Technology - DSPIC33EP512GP502-E/MM Datasheet



**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 60 MIPs |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 512KB (170K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 24K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 6x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VQFN Exposed Pad |
| Supplier Device Package | 28-QFN-S (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gp502-e-mm |

**TABLE 4-39: PMD REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMD1 | 0760 | T5MD | T4MD | T3MD | T2MD | T1MD | — | — | — | I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | — | C1MD | AD1MD | 0000 |
| PMD2 | 0762 | — | — | — | — | IC4MD | IC3MD | IC2MD | IC1MD | — | — | — | — | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | 0764 | — | — | — | — | — | CMPMD | — | — | CRCMD | — | — | — | — | — | I2C2MD | — | 0000 |
| PMD4 | 0766 | — | — | — | — | — | — | — | — | — | — | — | — | REFOMD | CTMUMD | — | — | 0000 |
| PMD6 | 076A | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| PMD7 | 076C | — | — | — | — | — | — | — | — | — | — | — | DMA0MD<br>DMA1MD<br>DMA2MD<br>DMA3MD | PTGMD | — | — | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-40: PMD REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMD1 | 0760 | T5MD | T4MD | T3MD | T2MD | T1MD | QEI1MD | PWMMD | — | I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | — | C1MD | AD1MD | 0000 |
| PMD2 | 0762 | — | — | — | — | IC4MD | IC3MD | IC2MD | IC1MD | — | — | — | — | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | 0764 | — | — | — | — | — | CMPMD | — | — | CRCMD | — | — | — | — | — | I2C2MD | — | 0000 |
| PMD4 | 0766 | — | — | — | — | — | — | — | — | — | — | — | — | REFOMD | CTMUMD | — | — | 0000 |
| PMD6 | 076A | — | — | — | — | — | PWM3MD | PWM2MD | PWM1MD | — | — | — | — | — | — | — | — | 0000 |
| PMD7 | 076C | — | — | — | — | — | — | — | — | — | — | — | DMA0MD<br>DMA1MD<br>DMA2MD<br>DMA3MD | PTGMD | — | — | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 7-1: INTERRUPT VECTOR DETAILS**

| Interrupt Source | Vector # | IRQ # | IVT Address | Interrupt Bit Location | | |
|---|---|---|---|---|---|---|
| | | | | Flag | Enable | Priority |
| Highest Natural Order Priority | | | | | | |
| INT0 – External Interrupt 0 | 8 | 0 | 0x000014 | IFS0<0> | IEC0<0> | IPC0<2:0> |
| IC1 – Input Capture 1 | 9 | 1 | 0x000016 | IFS0<1> | IEC0<1> | IPC0<6:4> |
| OC1 – Output Compare 1 | 10 | 2 | 0x000018 | IFS0<2> | IEC0<2> | IPC0<10:8> |
| T1 – Timer1 | 11 | 3 | 0x00001A | IFS0<3> | IEC0<3> | IPC0<14:12> |
| DMA0 – DMA Channel 0 | 12 | 4 | 0x00001C | IFS0<4> | IEC0<4> | IPC1<2:0> |
| IC2 – Input Capture 2 | 13 | 5 | 0x00001E | IFS0<5> | IEC0<5> | IPC1<6:4> |
| OC2 – Output Compare 2 | 14 | 6 | 0x000020 | IFS0<6> | IEC0<6> | IPC1<10:8> |
| T2 – Timer2 | 15 | 7 | 0x000022 | IFS0<7> | IEC0<7> | IPC1<14:12> |
| T3 – Timer3 | 16 | 8 | 0x000024 | IFS0<8> | IEC0<8> | IPC2<2:0> |
| SPI1E – SPI1 Error | 17 | 9 | 0x000026 | IFS0<9> | IEC0<9> | IPC2<6:4> |
| SPI1 – SPI1 Transfer Done | 18 | 10 | 0x000028 | IFS0<10> | IEC0<10> | IPC2<10:8> |
| U1RX – UART1 Receiver | 19 | 11 | 0x00002A | IFS0<11> | IEC0<11> | IPC2<14:12> |
| U1TX – UART1 Transmitter | 20 | 12 | 0x00002C | IFS0<12> | IEC0<12> | IPC3<2:0> |
| AD1 – ADC1 Convert Done | 21 | 13 | 0x00002E | IFS0<13> | IEC0<13> | IPC3<6:4> |
| DMA1 – DMA Channel 1 | 22 | 14 | 0x000030 | IFS0<14> | IEC0<14> | IPC3<10:8> |
| Reserved | 23 | 15 | 0x000032 | — | — | — |
| SI2C1 – I2C1 Slave Event | 24 | 16 | 0x000034 | IFS1<0> | IEC1<0> | IPC4<2:0> |
| MI2C1 – I2C1 Master Event | 25 | 17 | 0x000036 | IFS1<1> | IEC1<1> | IPC4<6:4> |
| CM – Comparator Combined Event | 26 | 18 | 0x000038 | IFS1<2> | IEC1<2> | IPC4<10:8> |
| CN – Input Change Interrupt | 27 | 19 | 0x00003A | IFS1<3> | IEC1<3> | IPC4<14:12> |
| INT1 – External Interrupt 1 | 28 | 20 | 0x00003C | IFS1<4> | IEC1<4> | IPC5<2:0> |
| Reserved | 29-31 | 21-23 | 0x00003E-0x000042 | — | — | — |
| DMA2 – DMA Channel 2 | 32 | 24 | 0x000044 | IFS1<8> | IEC1<8> | IPC6<2:0> |
| OC3 – Output Compare 3 | 33 | 25 | 0x000046 | IFS1<9> | IEC1<9> | IPC6<6:4> |
| OC4 – Output Compare 4 | 34 | 26 | 0x000048 | IFS1<10> | IEC1<10> | IPC6<10:8> |
| T4 – Timer4 | 35 | 27 | 0x00004A | IFS1<11> | IEC1<11> | IPC6<14:12> |
| T5 – Timer5 | 36 | 28 | 0x00004C | IFS1<12> | IEC1<12> | IPC7<2:0> |
| INT2 – External Interrupt 2 | 37 | 29 | 0x00004E | IFS1<13> | IEC1<13> | IPC7<6:4> |
| U2RX – UART2 Receiver | 38 | 30 | 0x000050 | IFS1<14> | IEC1<14> | IPC7<10:8> |
| U2TX – UART2 Transmitter | 39 | 31 | 0x000052 | IFS1<15> | IEC1<15> | IPC7<14:12> |
| SPI2E – SPI2 Error | 40 | 32 | 0x000054 | IFS2<0> | IEC2<0> | IPC8<2:0> |
| SPI2 – SPI2 Transfer Done | 41 | 33 | 0x000056 | IFS2<1> | IEC2<1> | IPC8<6:4> |
| C1RX – CAN1 RX Data Ready(1) | 42 | 34 | 0x000058 | IFS2<2> | IEC2<2> | IPC8<10:8> |
| C1 – CAN1 Event(1) | 43 | 35 | 0x00005A | IFS2<3> | IEC2<3> | IPC8<14:12> |
| DMA3 – DMA Channel 3 | 44 | 36 | 0x00005C | IFS2<4> | IEC2<4> | IPC9<2:0> |
| IC3 – Input Capture 3 | 45 | 37 | 0x00005E | IFS2<5> | IEC2<5> | IPC9<6:4> |
| IC4 – Input Capture 4 | 46 | 38 | 0x000060 | IFS2<6> | IEC2<6> | IPC9<10:8> |
| Reserved | 47-56 | 39-48 | 0x000062-0x000074 | — | — | — |
| SI2C2 – I2C2 Slave Event | 57 | 49 | 0x000076 | IFS3<1> | IEC3<1> | IPC12<6:4> |
| MI2C2 – I2C2 Master Event | 58 | 50 | 0x000078 | IFS3<2> | IEC3<2> | IPC12<10:8> |
| Reserved | 59-64 | 51-56 | 0x00007A-0x000084 | — | — | — |
| PSEM – PWM Special Event Match(2) | 65 | 57 | 0x000086 | IFS3<9> | IEC3<9> | IPC14<6:4> |

**Note 1:** This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

**2:** This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

## 8.0 DIRECT MEMORY ACCESS (DMA)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Direct Memory Access (DMA)"** (DS70348) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The DMA Controller transfers data between Peripheral Data registers and Data Space SRAM

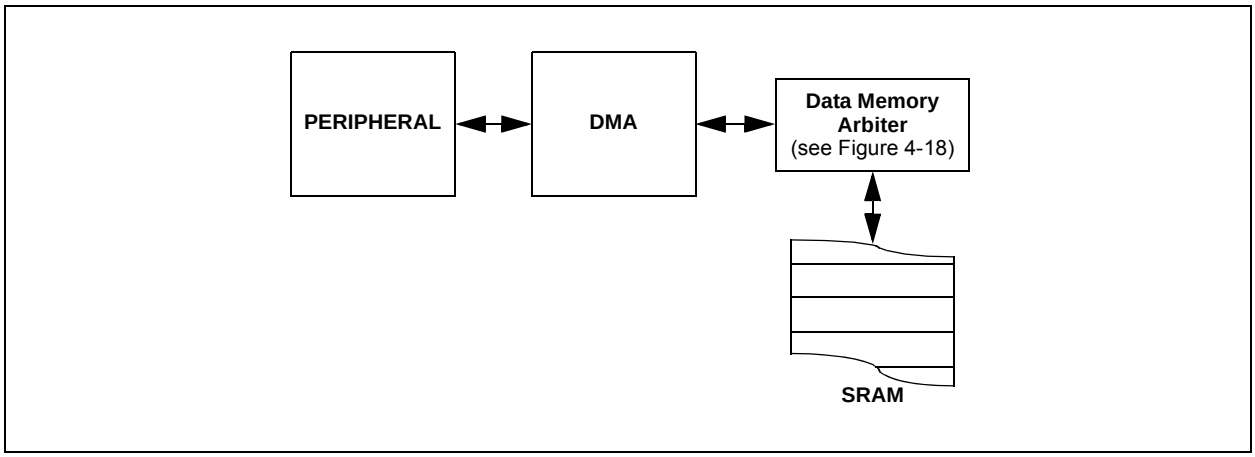
In addition, DMA can access the entire data memory space. The Data Memory Bus Arbiter is utilized when either the CPU or DMA attempts to access SRAM, resulting in potential DMA or CPU stalls.

The DMA Controller supports 4 independent channels. Each channel can be configured for transfers to or from selected peripherals. Some of the peripherals supported by the DMA Controller include:

- ECAN™
- Analog-to-Digital Converter (ADC)
- Serial Peripheral Interface (SPI)
- UART
- Input Capture
- Output Compare

Refer to Table 8-1 for a complete list of supported peripherals.

**FIGURE 8-1: DMA CONTROLLER MODULE**



**REGISTER 16-7: PWMCONx: PWMx CONTROL REGISTER**

| HS/HC-0 | HS/HC-0 | HS/HC-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FLTSTAT(1) | CLSTAT(1) | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB(2) | MDCS(2) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DTC1 | DTC0 | DTCP(3) | — | MTBS | CAM(2,4) | XPRES(5) | IUE(2) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FLTSTAT:** Fault Interrupt Status bit(1)
1 = Fault interrupt is pending
0 = No Fault interrupt is pending
This bit is cleared by setting FLTIEN = 0.

bit 14 **CLSTAT:** Current-Limit Interrupt Status bit(1)
1 = Current-limit interrupt is pending
0 = No current-limit interrupt is pending
This bit is cleared by setting CLIEN = 0.

bit 13 **TRGSTAT:** Trigger Interrupt Status bit
1 = Trigger interrupt is pending
0 = No trigger interrupt is pending
This bit is cleared by setting TRGIEN = 0.

bit 12 **FLTIEN:** Fault Interrupt Enable bit
1 = Fault interrupt is enabled
0 = Fault interrupt is disabled and the FLTSTAT bit is cleared

bit 11 **CLIEN:** Current-Limit Interrupt Enable bit
1 = Current-limit interrupt is enabled
0 = Current-limit interrupt is disabled and the CLSTAT bit is cleared

bit 10 **TRGIEN:** Trigger Interrupt Enable bit
1 = A trigger event generates an interrupt request
0 = Trigger event interrupts are disabled and the TRGSTAT bit is cleared

bit 9 **ITB:** Independent Time Base Mode bit(2)
1 = PHASEx register provides time base period for this PWM generator
0 = PTPER register provides timing for this PWM generator

bit 8 **MDCS:** Master Duty Cycle Register Select bit(2)
1 = MDC register provides duty cycle information for this PWM generator
0 = PDCx register provides duty cycle information for this PWM generator

**Note 1:** Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
**2:** These bits should not be changed after the PWMx is enabled (PTEN = 1).
**3:** DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.
**4:** The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
**5:** To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

## 18.0 SERIAL PERIPHERAL INTERFACE (SPI)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Serial Peripheral Interface (SPI)"** (DS70569) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with Motorola® SPI and SIOP interfaces.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X device family offers two SPI modules on a single device. These modules, which are designated as SPI1 and SPI2, are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

**Note:** In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 and SPI2 modules.

The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of the SPI2 module, but results in a lower maximum speed for SPI2. See **Section 30.0 "Electrical Characteristics"** for more information.

The SPIx serial interface consists of four pins, as follows:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- $\overline{SS}$x/FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, $\overline{SS}$x is not used. In 2-pin mode, neither SDOx nor $\overline{SS}$x is used.

Figure 18-1 illustrates the block diagram of the SPIx module in Standard and Enhanced modes.

## 20.1 UART Helpful Tips

1. In multi-node, direct-connect UART networks, UART receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
   a) If URXINV = 0, use a pull-up resistor on the RX pin.
   b) If URXINV = 1, use a pull-down resistor on the RX pin.
2. The first character received on a wake-up from Sleep mode caused by activity on the UxRX pin of the UARTx module will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid; this is to be expected.

## 20.2 UART Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 20.2.1 KEY RESOURCES

- **"UART"** (DS70582) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

**REGISTER 21-3: CxVEC: ECANx INTERRUPT CODE REGISTER**

| U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | FILHIT4 | FILHIT3 | FILHIT2 | FILHIT1 | FILHIT0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | R-1 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | ICODE6 | ICODE5 | ICODE4 | ICODE3 | ICODE2 | ICODE1 | ICODE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Number bits

10000-11111 = Reserved
01111 = Filter 15
•
•
•
00001 = Filter 1
00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ICODE<6:0>:** Interrupt Flag Code bits

1000101-1111111 = Reserved
1000100 = FIFO almost full interrupt
1000011 = Receiver overflow interrupt
1000010 = Wake-up interrupt
1000001 = Error interrupt
1000000 = No interrupt
•
•
•
0010000-0111111 = Reserved
0001111 = RB15 buffer interrupt
•
•
•
0001001 = RB9 buffer interrupt
0001000 = RB8 buffer interrupt
0000111 = TRB7 buffer interrupt
0000110 = TRB6 buffer interrupt
0000101 = TRB5 buffer interrupt
0000100 = TRB4 buffer interrupt
0000011 = TRB3 buffer interrupt
0000010 = TRB2 buffer interrupt
0000001 = TRB1 buffer interrupt
0000000 = TRB0 buffer interrupt

## 22.2 CTMU Control Registers

**REGISTER 22-1: CTMUCON1: CTMU CONTROL REGISTER 1**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CTMUEN | — | CTMUSIDL | TGEN | EDGEN | EDGSEQEN | IDISSEN(1) | CTTRIG |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CTMUEN:** CTMU Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CTMUSIDL:** CTMU Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **TGEN:** Time Generation Enable bit
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11 **EDGEN:** Edge Enable bit
1 = Hardware modules are used to trigger edges (TMRx, CTEDx, etc.)
0 = Software is used to trigger edges (manual set of EDGxSTAT)

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge 1 event must occur before Edge 2 event can occur
0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit(1)
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** ADC Trigger Control bit
1 = CTMU triggers ADC start of conversion
0 = CTMU does not trigger ADC start of conversion

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** The ADC module Sample-and-Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitance measurement must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

**REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER**

| R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CH0NB | — | — | CH0SB4(1) | CH0SB3(1) | CH0SB2(1) | CH0SB1(1) | CH0SB0(1) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CH0NA | — | — | CH0SA4(1) | CH0SA3(1) | CH0SA2(1) | CH0SA1(1) | CH0SA0(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CH0NB:** Channel 0 Negative Input Select for Sample MUXB bit
1 = Channel 0 negative input is AN1(1)
0 = Channel 0 negative input is VREFL

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **CH0SB<4:0>:** Channel 0 Positive Input Select for Sample MUXB bits(1)
11111 = Open; use this selection with CTMU capacitive and time measurement
11110 = Channel 0 positive input is connected to the CTMU temperature measurement diode (CTMU TEMP)
11101 = Reserved
11100 = Reserved
11011 = Reserved
11010 = Channel 0 positive input is the output of OA3/AN6(2,3)
11001 = Channel 0 positive input is the output of OA2/AN0(2)
11000 = Channel 0 positive input is the output of OA1/AN3(2)
10111 = Reserved
•
•
•
10000 = Reserved
01111 = Channel 0 positive input is AN15(3)
01110 = Channel 0 positive input is AN14(3)
01101 = Channel 0 positive input is AN13(3)
•
•
•
00010 = Channel 0 positive input is AN2(3)
00001 = Channel 0 positive input is AN1(3)
00000 = Channel 0 positive input is AN0(3)

bit 7 **CH0NA:** Channel 0 Negative Input Select for Sample MUXA bit
1 = Channel 0 negative input is AN1(1)
0 = Channel 0 negative input is VREFL

bit 6-5 **Unimplemented:** Read as '0'

**Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

**2:** The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

**3:** See the **"Pin Diagrams"** section for the available analog channels for each device.

**REGISTER 24-2: PTGCON: PTG CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGCLK2 | PTGCLK1 | PTGCLK0 | PTGDIV4 | PTGDIV3 | PTGDIV2 | PTGDIV1 | PTGDIV0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGPWD3 | PTGPWD2 | PTGPWD1 | PTGPWD0 | — | PTGWDT2 | PTGWDT1 | PTGWDT0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-13 **PTGCLK<2:0>:** Select PTG Module Clock Source bits
111 = Reserved
110 = Reserved
101 = PTG module clock source will be T3CLK
100 = PTG module clock source will be T2CLK
011 = PTG module clock source will be T1CLK
010 = PTG module clock source will be TAD
001 = PTG module clock source will be FOSC
000 = PTG module clock source will be FP

bit 12-8 **PTGDIV<4:0>:** PTG Module Clock Prescaler (divider) bits
11111 = Divide-by-32
11110 = Divide-by-31
•
•
•
00001 = Divide-by-2
00000 = Divide-by-1

bit 7-4 **PTGPWD<3:0>:** PTG Trigger Output Pulse-Width bits
1111 = All trigger outputs are 16 PTG clock cycles wide
1110 = All trigger outputs are 15 PTG clock cycles wide
•
•
•
0001 = All trigger outputs are 2 PTG clock cycles wide
0000 = All trigger outputs are 1 PTG clock cycle wide

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **PTGWDT<2:0>:** Select PTG Watchdog Timer Time-out Count Value bits
111 = Watchdog Timer will time-out after 512 PTG clocks
110 = Watchdog Timer will time-out after 256 PTG clocks
101 = Watchdog Timer will time-out after 128 PTG clocks
100 = Watchdog Timer will time-out after 64 PTG clocks
011 = Watchdog Timer will time-out after 32 PTG clocks
010 = Watchdog Timer will time-out after 16 PTG clocks
001 = Watchdog Timer will time-out after 8 PTG clocks
000 = Watchdog Timer is disabled

**REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER(1,2) (CONTINUED)**

bit 4 **OC1CS:** Clock Source for OC1 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

bit 3 **OC4TSS:** Trigger/Synchronization Source for OC4 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

bit 2 **OC3TSS:** Trigger/Synchronization Source for OC3 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

bit 1 **OC2TSS:** Trigger/Synchronization Source for OC2 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

bit 0 **OC1TSS:** Trigger/Synchronization Source for OC1 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**2:** This register is only used with the PTGCTRL OPTION = 1111 Step command.

## 30.1 DC Characteristics

**TABLE 30-1: OPERATING MIPS VS. VOLTAGE**

| Characteristic | VDD Range (in Volts) | Temp Range (in °C) | Maximum MIPS |
|---|---|---|---|
| | | | dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X |
| — | 3.0V to 3.6V(1) | -40°C to +85°C | 70 |
| — | 3.0V to 3.6V(1) | -40°C to +125°C | 60 |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**TABLE 30-2: THERMAL OPERATING CONDITIONS**

| Rating | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Industrial Temperature Devices | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +125 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +85 | °C |
| Extended Temperature Devices | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +140 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +125 | °C |
| Power Dissipation:<br>Internal chip power dissipation:<br>PINT = VDD x (IDD – Σ IOH)<br>I/O Pin Power Dissipation:<br>I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL) | PD | PINT + PI/O | | | W |
| Maximum Allowed Power Dissipation | PDMAX | (TJ – TA)/θJA | | | W |

**TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS**

| Characteristic | Symbol | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Package Thermal Resistance, 64-Pin QFN | θJA | 28.0 | — | °C/W | 1 |
| Package Thermal Resistance, 64-Pin TQFP 10x10 mm | θJA | 48.3 | — | °C/W | 1 |
| Package Thermal Resistance, 48-Pin UQFN 6x6 mm | θJA | 41 | — | °C/W | 1 |
| Package Thermal Resistance, 44-Pin QFN | θJA | 29.0 | — | °C/W | 1 |
| Package Thermal Resistance, 44-Pin TQFP 10x10 mm | θJA | 49.8 | — | °C/W | 1 |
| Package Thermal Resistance, 44-Pin VTLA 6x6 mm | θJA | 25.2 | — | °C/W | 1 |
| Package Thermal Resistance, 36-Pin VTLA 5x5 mm | θJA | 28.5 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin QFN-S | θJA | 30.0 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin SSOP | θJA | 71.0 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin SOIC | θJA | 69.7 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin SPDIP | θJA | 60.0 | — | °C/W | 1 |

**Note 1:** Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

**FIGURE 30-2: EXTERNAL CLOCK TIMING**

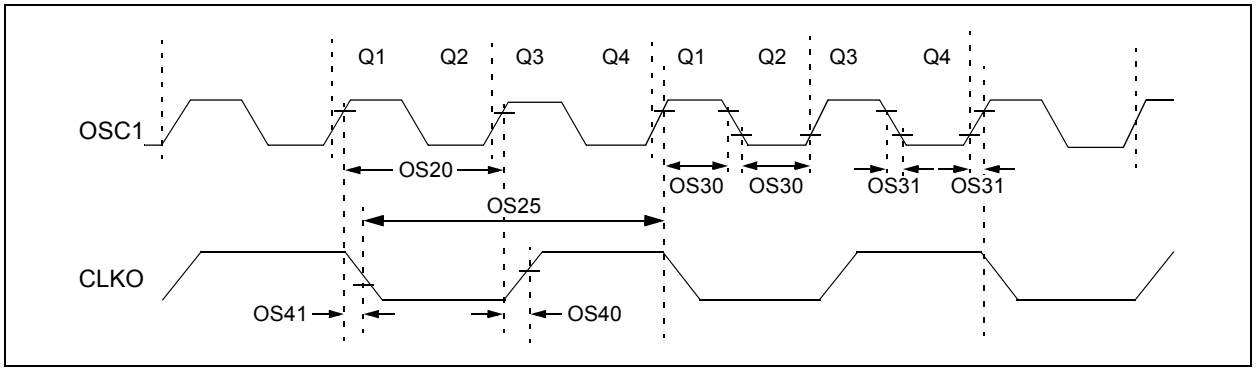



**TABLE 30-17: EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symb** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| OS10 | FIN | External CLKI Frequency (External clocks allowed only in EC and ECPLL modes) | DC | — | 60 | MHz | EC |
| | | Oscillator Crystal Frequency | 3.5<br>10 | —<br>— | 10<br>25 | MHz<br>MHz | XT<br>HS |
| OS20 | TOSC | TOSC = 1/FOSC | 8.33 | — | DC | ns | +125ºC |
| | | TOSC = 1/FOSC | 7.14 | — | DC | ns | +85ºC |
| OS25 | TCY | Instruction Cycle Time(2) | 16.67 | — | DC | ns | +125ºC |
| | | Instruction Cycle Time(2) | 14.28 | — | DC | ns | +85ºC |
| OS30 | TosL, TosH | External Clock in (OSC1) High or Low Time | 0.45 x TOSC | — | 0.55 x TOSC | ns | EC |
| OS31 | TosR, TosF | External Clock in (OSC1) Rise or Fall Time | — | — | 20 | ns | EC |
| OS40 | TckR | CLKO Rise Time(3,4) | — | 5.2 | — | ns | |
| OS41 | TckF | CLKO Fall Time(3,4) | — | 5.2 | — | ns | |
| OS42 | GM | External Oscillator Transconductance(4) | — | 12 | — | mA/V | HS, VDD = 3.3V, TA = +25ºC |
| | | | — | 6 | — | mA/V | XT, VDD = 3.3V, TA = +25ºC |

**Note 1:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**2:** Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Minimum" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Maximum" cycle time limit is "DC" (no clock) for all devices.

**3:** Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

**4:** This parameter is characterized, but not tested in manufacturing.

**TABLE 30-58: ADC MODULE SPECIFICATIONS (12-BIT MODE)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[1]<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **ADC Accuracy (12-Bit Mode)** | | | | | | | |
| AD20a | Nr | Resolution | 12 Data Bits | | | bits | |
| AD21a | INL | Integral Nonlinearity | -2.5 | — | 2.5 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -5.5 | — | 5.5 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD22a | DNL | Differential Nonlinearity | -1 | — | 1 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -1 | — | 1 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD23a | GERR | Gain Error[3] | -10 | — | 10 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -10 | — | 10 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD24a | EOFF | Offset Error | -5 | — | 5 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -5 | — | 5 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD25a | — | Monotonicity | — | — | — | — | Guaranteed |
| **Dynamic Performance (12-Bit Mode)** | | | | | | | |
| AD30a | THD | Total Harmonic Distortion[3] | — | 75 | — | dB | |
| AD31a | SINAD | Signal to Noise and Distortion[3] | — | 68 | — | dB | |
| AD32a | SFDR | Spurious Free Dynamic Range[3] | — | 80 | — | dB | |
| AD33a | FNYQ | Input Signal Bandwidth[3] | — | 250 | — | kHz | |
| AD34a | ENOB | Effective Number of Bits[3] | 11.09 | 11.3 | — | bits | |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

**3:** Parameters are characterized but not tested in manufacturing.

**TABLE 31-11: INTERNAL RC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Characteristic | Min | Typ | Max | Units | Conditions | |
| | **LPRC @ 32.768 kHz(1,2)** | | | | | | |
| HF21 | LPRC | -30 | — | +30 | % | -40°C ≤ TA ≤ +150°C | VDD = 3.0-3.6V |

**Note 1:** Change of LPRC frequency as VDD changes.

**2:** LPRC accuracy impacts the Watchdog Timer Time-out Period (TWDT). See **Section 27.5 "Watchdog Timer (WDT)"** for more information.

**TABLE 31-12: ADC MODULE SPECIFICATIONS (12-BIT MODE)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ | Max | Units | Conditions |
| **ADC Accuracy (12-Bit Mode)(1)** | | | | | | | |
| HAD20a | Nr | Resolution(3) | 12 Data Bits | | | bits | |
| HAD21a | INL | Integral Nonlinearity | -5.5 | — | 5.5 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD22a | DNL | Differential Nonlinearity | -1 | — | 1 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD23a | GERR | Gain Error | -10 | — | 10 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD24a | EOFF | Offset Error | -5 | — | 5 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| **Dynamic Performance (12-Bit Mode)(2)** | | | | | | | |
| HAD33a | FNYQ | Input Signal Bandwidth | — | — | 200 | kHz | |

**Note 1:** These parameters are characterized, but are tested at 20 ksps only.

**2:** These parameters are characterized by similarity, but are not tested in manufacturing.

**3:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

**TABLE 31-13: ADC MODULE SPECIFICATIONS (10-BIT MODE)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ | Max | Units | Conditions |
| **ADC Accuracy (10-Bit Mode)(1)** | | | | | | | |
| HAD20b | Nr | Resolution(3) | 10 Data Bits | | | bits | |
| HAD21b | INL | Integral Nonlinearity | -1.5 | — | 1.5 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD22b | DNL | Differential Nonlinearity | -0.25 | — | 0.25 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD23b | GERR | Gain Error | -2.5 | — | 2.5 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD24b | EOFF | Offset Error | -1.25 | — | 1.25 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| **Dynamic Performance (10-Bit Mode)(2)** | | | | | | | |
| HAD33b | FNYQ | Input Signal Bandwidth | — | — | 400 | kHz | |

**Note 1:** These parameters are characterized, but are tested at 20 ksps only.

**2:** These parameters are characterized by similarity, but are not tested in manufacturing.

**3:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

**FIGURE 32-9: TYPICAL FRC FREQUENCY @ $V_{DD}$ = 3.3V**

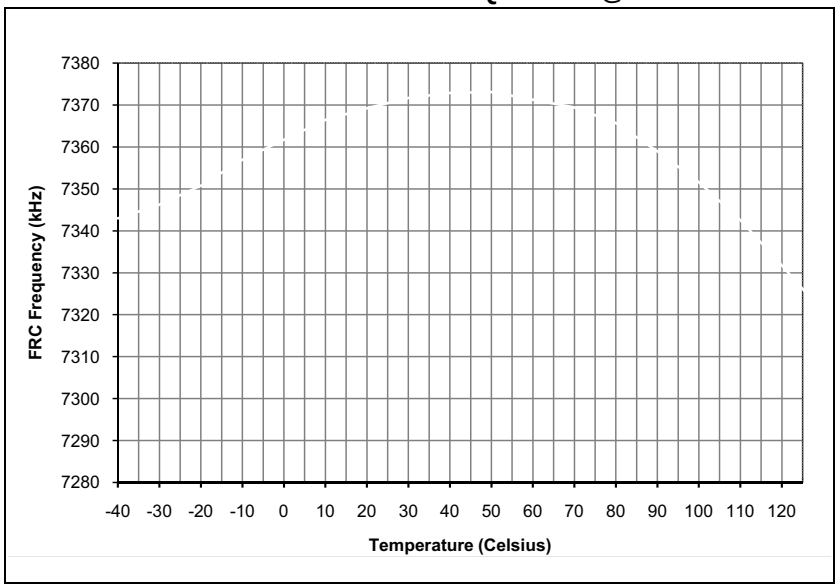



**FIGURE 32-10: TYPICAL LPRC FREQUENCY @ $V_{DD}$ = 3.3V**

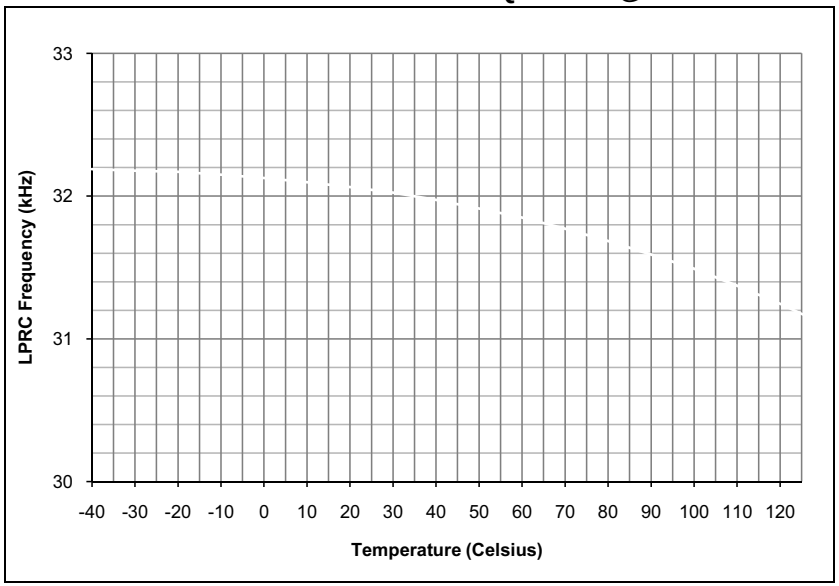
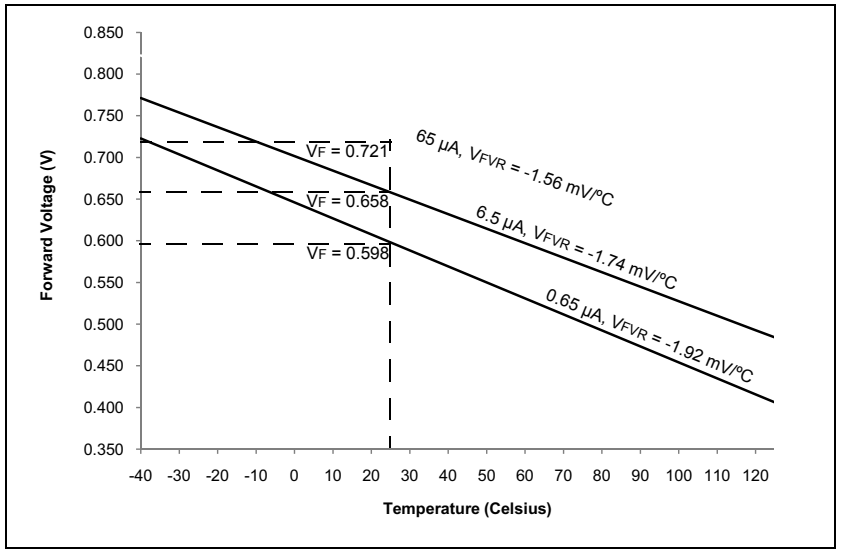
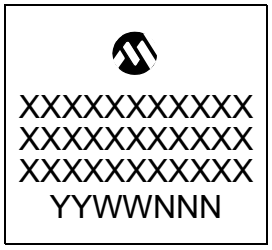



**FIGURE 32-11: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE**



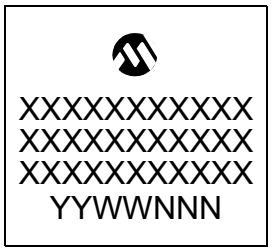
### 33.1 Package Marking Information (Continued)

48-Lead UQFN (6x6x0.5 mm)



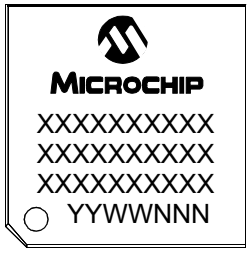

Example


64-Lead QFN (9x9x0.9 mm)

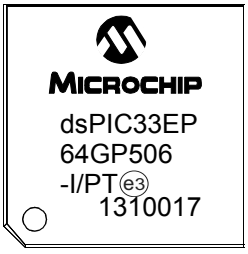



Example


64-Lead TQFP (10x10x1 mm)

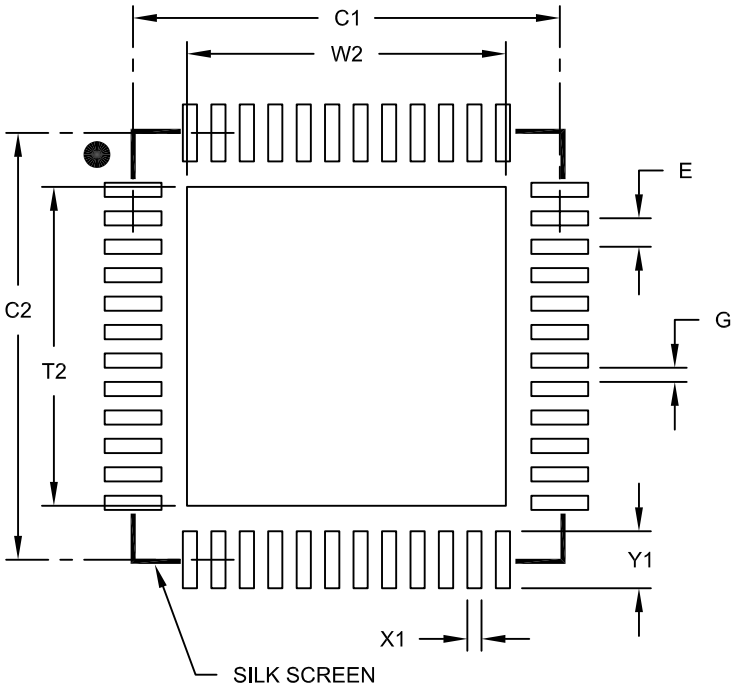



Example



48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN]
With 0.40 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.40 BSC | |
| Optional Center Pad Width | W2 | | | 4.45 |
| Optional Center Pad Length | T2 | | | 4.45 |
| Contact Pad Spacing | C1 | | 6.00 | |
| Contact Pad Spacing | C2 | | 6.00 | |
| Contact Pad Width (X28) | X1 | | | 0.20 |
| Contact Pad Length (X28) | Y1 | | | 0.80 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A

**TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 30.0 "Electrical Characteristics"** | Removed Voltage on VCAP with respect to Vss and added Note 5 in Absolute Maximum Ratings(1).<br><br>Removed Parameter DC18 (VCORE) and Note 3 from the DC Temperature and Voltage Specifications (see Table 30-4).<br><br>Updated Note 1 in the DC Characteristics: Operating Current (IDD) (see Table 30-6).<br><br>Updated Note 1 in the DC Characteristics: Idle Current (IIDLE) (see Table 30-7).<br><br>Changed the Typical values for Parameters DC60a-DC60d and updated Note 1 in the DC Characteristics: Power-down Current (IPD) (see Table 30-8).<br><br>Updated Note 1 in the DC Characteristics: Doze Current (IDOZE) (see Table 30-9).<br><br>Updated Note 2 in the Electrical Characteristics: BOR (see Table 30-12).<br><br>Updated Parameters CM20 and CM31, and added Parameters CM44 and CM45 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14).<br><br>Added the Op amp/Comparator Reference Voltage Settling Time Specifications (see Table 30-15).<br><br>Added Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16).<br><br>Updated Internal FRC Accuracy Parameter F20a (see Table 30-21).<br><br>Updated the Typical value and Units for Parameter CTMUI1, and added Parameters CTMUI4, CTMUFV1, and CTMUFV2 to the CTMU Current Source Specifications (see Table 30-55). |
| **Section 31.0 "Packaging Information"** | Updated packages by replacing references of VLAP with TLA. |
| **"Product Identification System"** | Changed VLAP to TLA. |