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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gp502-h-mm

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μ F to 47 μ F.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 1 Ohm) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must have a capacitor greater than 4.7 μ F (10 μ F is recommended), 16V connected to ground. The type can be ceramic or tantalum. See **Section 30.0** "**Electrical Characteristics**" for additional information.

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See **Section 27.3 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

- Device Reset
- Device Programming and Debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor, C, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.





3.0 CPU

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "CPU" (DS70359) in the "dsPIC33/PIC24 Family Reference Manual', which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

3.1 Registers

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can act as a data, address or address offset register. The 16th working register (W15) operates as a Software Stack Pointer for interrupts and calls.

3.2 Instruction Set

The instruction set for dsPIC33EPXXXGP50X and dsPIC33EPXXXMC20X/50X devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. The instruction set for PIC24EPXXXGP/MC20X devices has the MCU class of instructions only and does not support DSP instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3 Data Space Addressing

The base Data Space can be addressed as 64 Kbytes (32K words).

The Data Space includes two ranges of memory, referred to as X and Y data memory. Each memory range is accessible through its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Spaces have memory locations that are device-specific, and are described further in the data memory maps in **Section 4.2 "Data Address Space"**.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space (PS) at any 32-Kbyte aligned program word boundary. The Program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to the "**Data Memory**" (DS70595) and "**Program Memory**" (DS70613) sections in the "*dsPIC33/PIC24 Family Reference Manual*" for more details on EDS, PSV and table accesses.

On the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data re-ordering for radix-2 FFT algorithms. PIC24EPXXXGP/MC20X devices do not support Modulo and Bit-Reversed Addressing.

3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- · Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.





TABLE 4-39: PMD REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	—	—	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD	AD1MD	0000
PMD2	0762	_	_	_	_	IC4MD	IC3MD	IC2MD	IC1MD	_	_	_	_	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	_	_	_	_	_	CMPMD	_	_	CRCMD	_	_	_	_	_	I2C2MD	_	0000
PMD4	0766	_	_	_	_	_	_	_	_	_	_	_	_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
PMD7	076C		_			_		_		_	_		DMA0MD DMA1MD DMA2MD DMA3MD	PTGMD	_	_	_	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-40: PMD REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD	AD1MD	0000
PMD2	0762	_	_	_	_	IC4MD	IC3MD	IC2MD	IC1MD	_	_	—	_	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	_	_	_	_	_	CMPMD	_	_	CRCMD	_	—	_	—	_	I2C2MD	_	0000
PMD4	0766	_	_	_	_	_	_	_	—	_	_	—	_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	_	_	_	_	_	PWM3MD	PWM2MD	PWM1MD	_	_	—	_	—	_	_	_	0000
													DMA0MD					
	0760												DMA1MD	DTOMD				
PIVID7	0760	_	_	_	_	_	_	_	_	_	_	_	DMA2MD	PIGMD	_	_	_	0000
													DMA3MD]				

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-42: OP AMP/COMPARATOR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	0A80	PSIDL	—	—	—	C4EVT	C3EVT	C2EVT	C1EVT	—	-	—	—	C4OUT	C3OUT	C2OUT	C10UT	0000
CVRCON	0A82	_	CVR2OE	_	—	_	VREFSEL	_	—	CVREN	CVR10E	CVRR	CVRSS		CVR<	3:0>		0000
CM1CON	0A84	CON	COE	CPOL	—		OPMODE	CEVT	COUT	EVPO	_<1:0>	—	CREF		_	CCH	<1:0>	0000
CM1MSKSRC	0A86		—		—		SELSR	CC<3:0>			SELSRC	B<3:0>			SELSRC	A<3:0>		0000
CM1MSKCON	0A88	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM1FLTR	0A8A		—		—		—		—		C	FSEL<2:0	>	CFLTREN	0	CFDIV<2:0	>	0000
CM2CON	0A8C	CON	COE	CPOL	—		OPMODE	CEVT	COUT	EVPO	_<1:0>	—	CREF		_	CCH	<1:0>	0000
CM2MSKSRC	0A8E		—		—		SELSR	CC<3:0>			SELSRC	B<3:0>			SELSRC	A<3:0>		0000
CM2MSKCON	0A90	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM2FLTR	0A92		—		—		—		—		C	FSEL<2:0	>	CFLTREN	0	CFDIV<2:0	>	0000
CM3CON ⁽¹⁾	0A94	CON	COE	CPOL	—		OPMODE	CEVT	COUT	EVPO	_<1:0>	—	CREF		_	CCH	<1:0>	0000
CM3MSKSRC(1)	0A96		—		—		SELSR	CC<3:0>			SELSRC	B<3:0>			SELSRC	A<3:0>		0000
CM3MSKCON ⁽¹⁾	0A98	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM3FLTR ⁽¹⁾	0A9A	_	_	_	_	_	_	_	_	_	C	FSEL<2:0	>	CFLTREN	(CFDIV<2:0	>	0000
CM4CON	0A9C	CON	COE	CPOL	_	_	_	CEVT	COUT	EVPO	_<1:0>	_	CREF	_	_	CCH	<1:0>	0000
CM4MSKSRC	0A9E		—		—		SELSR	CC<3:0>			SELSRC	B<3:0>			SELSRC	A<3:0>		0000
CM4MSKCON	0AA0	HLMS	_	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM4FLTR	0AA2	_	—	—	—	—	-	—	_	—	C	FSEL<2:0	>	CFLTREN	(CFDIV<2:0	>	0000

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are unavailable on dsPIC33EPXXXGP502/MC502/MC502/MC202 and PIC24EP256GP/MC202 (28-pin) devices.

TABLE 4-43: CTMU REGISTER MAP

File	Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CTML	JCON1	033A	CTMUEN	-	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	—	—	-	—			—	—	0000
CTML	JCON2	033C	EDG1MOD	EDG1POL		EDG1	SEL<3:0>		EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL		EDG2S	EL<3:0>		_		0000
CTML	JICON	033E			ITRIM<5	5:0>			IRNG	6<1:0>	—	_		_	_	_			0000

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-44: JTAG INTERFACE REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
JDATAH	0FF0	—	_	—	—						JDATAH	<27:16>						xxxx
JDATAL	0FF2						JDATAL<15:0> 0000							0000				

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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4.8.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit-wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

- TBLRDL (Table Read Low):
 - In Word mode, this instruction maps the lower word of the Program Space location (P<15:0>) to a data address (D<15:0>)

- In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.
- TBLRDH (Table Read High):
 - In Word mode, this instruction maps the entire upper word of a program address (P<23:16>) to a data address. The 'phantom' byte (D<15:8>) is always '0'.
 - In Byte mode, this instruction maps the upper or lower byte of the program word to D<7:0> of the data address in the TBLRDL instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.



FIGURE 4-23: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 3	SLEEP: Wake-up from Sleep Flag bit 1 = Device has been in Sleep mode 0 = Device has not been in Sleep mode
bit 2	IDLE: Wake-up from Idle Flag bit
	1 = Device was in Idle mode0 = Device was not in Idle mode
bit 1	BOR: Brown-out Reset Flag bit 1 = A Brown-out Reset has occurred 0 = A Brown-out Reset has not occurred
bit 0	POR: Power-on Reset Flag bit 1 = A Power-on Reset has occurred 0 = A Power-on Reset has not occurred

- **Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
 - 2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 8-9: DSADRH: DMA MOST RECENT RAM HIGH ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_	—	—	_	—	—	—
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSADR	<23:16>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable bi	t	U = Unimpler	mented bit, read	as '0'	

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 DSADR<23:16>: Most Recent DMA Address Accessed by DMA bits

REGISTER 8-10: DSADRL: DMA MOST RECENT RAM LOW ADDRESS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSAI	DR<15:8>			
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSA	DR<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable bit		U = Unimplemer	nted bit, re	ad as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleare	d	x = Bit is unknown	

bit 15-0 DSADR<15:0>: Most Recent DMA Address Accessed by DMA bits

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	1, 2
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	1
Low-Power RC Oscillator (LPRC)	Internal	xx	101	1
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	
Primary Oscillator (EC) with PLL (ECPLL)	Primary	0.0	011	1
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	1
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)	Internal	xx	001	1
Fast RC Oscillator (FRC)	Internal	xx	000	1

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

9.2 Oscillator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

9.2.1 KEY RESOURCES

- "Oscillator" (DS70580) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- · Development Tools

10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the powersaving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the ECAN[™] module has been configured for 500 kbps, based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the ECAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC[®] DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note:	If a PMD bit is set, the corresponding
	module is disabled after a delay of one
	instruction cycle. Similarly, if a PMD bit is
	cleared, the corresponding module is
	enabled after a delay of one instruction
	cycle (assuming the module control regis-
	ters are already configured to enable
	module operation).

10.5 Power-Saving Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.



10.5.1 KEY RESOURCES

- "Watchdog Timer and Power-Saving Modes" (DS70615) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)

bit 6-4	SYNCSRC<2:0>: Synchronous Source Selection bits ⁽¹⁾ 111 = Reserved
	•
	• 100 = Reserved 011 = PTGO17 ⁽²⁾ 010 = PTGO16 ⁽²⁾ 001 = Reserved 000 = SYNCI1 input from PPS
bit 3-0	<pre>SEVTPS<3:0>: PWMx Special Event Trigger Output Postscaler Select bits⁽¹⁾ 1111 = 1:16 Postscaler generates Special Event Trigger on every sixteenth compare match event</pre>
	0001 = 1:2 Postscaler generates Special Event Trigger on every second compare match event 0000 = 1:1 Postscaler generates Special Event Trigger on every compare match event

- **Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.
 - 2: See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

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R/W-0	R/W	-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0				
VCFG2	VCFC	G1	VCFG0		_	CSCNA	CHPS1	CHPS0				
bit 15								bit 8				
R-0	R/W	-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
BUFS	SMPI4		SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS				
bit 7								bit 0				
Legend:												
R = Readable	e bit		W = Writable	bit	U = Unimpl	emented bit, read	d as '0'					
-n = Value at	POR		'1' = Bit is set		'0' = Bit is c	cleared	x = Bit is unk	nown				
bit 15-13	VCFG<	VCFG<2:0>: Converter Voltage Reference Configuration bits										
	Value		VREFH	VREFL								
	000		Avdd	Avss								
	001	Ext	ernal VREF+	Avss								
	010		Avdd	External VRE	F-							
	011	Ext	ernal VREF+	External VRE	F-							
	lxx		Avdd	Avss								
bit 12-11	Unimple	emen	ted: Read as '	0'								
bit 10	CSCNA	CSCNA: Input Scan Select bit										
	1 = Sca 0 = Doe	ns inp s not	outs for CH0+ o scan inputs	luring Sample N	<i>I</i> UXA							
bit 9-8	CHPS<	1:0>:	Channel Selec	t bits								
	<u>In 12-bit</u>	tmode	e (AD21B = 1)	the CHPS<1:0	> bits are U	nimplemented ar	nd are Read as	<u>'0':</u>				
	1x = Converts CH0, CH1, CH2 and CH3 01 = Converts CH0 and CH1 00 = Converts CH0											
bit 7	BUFS:	BUFS: Buffer Fill Status bit (only valid when BUFM = 1)										
	1 = ADC is currently filling the second half of the buffer; the user application should access data in the											
	 first half of the buffer 0 = ADC is currently filling the first half of the buffer; the user application should access data in the second half of the buffer 											
bit 6-2	SMPI<4	SMPI<4:0>: Increment Rate bits										
	When A	When ADDMAEN = 0:										
	x1111 =	x1111 = Generates interrupt after completion of every 16th sample/conversion operation										
	x1110 =	= Gen	erates interrup	t after completion	on of every	15th sample/conv	ersion operation	on				
	•											
	•											
	x0001 = x0000 =	= Gen = Gen	erates interrup erates interrup	t after completion t after completion	on of every 2 on of every 3	2nd sample/conv sample/conversic	ersion operation	n				
	When A	When ADDMAEN = 1:										
	11111 =	= Incre	ements the DM	IA address after	completion	of every 32nd sa	ample/conversi	ion operation				
	11110 =	= Incre	ements the DM	IA address after	r completion	of every 31st sa	mple/conversion	on operation				
	•											
	•											
	00001 = Increments the DMA address after completion of every 2nd sample/conversion operation											

. . ACOND. ADCA CONTROL DECISTED 2

24.3 PTG Control Registers

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGEN	—	PTGSIDL	PTGTOGL	—	PTGSWT ⁽²⁾	PTGSSEN ⁽³⁾	PTGIVIS
bit 15							bit 8
R/W-0	HS-0	U-0	U-0	U-0	U-0	R/V	V-0
PTGSTRT	PTGWDTO	_	_	_	_	PTGITM1 ⁽¹⁾	PTGITM0 ⁽¹⁾

h	it	7
υ	π.	1

Legend:	HS = Hardware Settable bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15		PTGEN: Module Enable bit
		1 = PTG module is enabled
		0 = PTG module is disabled
bit 14		Unimplemented: Read as '0'
bit 13		PTGSIDL: PTG Stop in Idle Mode bit
		 1 = Discontinues module operation when device enters Idle mode 0 = Continues module operation in Idle mode
bit 12		PTGTOGL: PTG TRIG Output Toggle Mode bit
		 1 = Toggle state of the PTGOx for each execution of the PTGTRIG command 0 = Each execution of the PTGTRIG command will generate a single PTGOx pulse determined by the value in the PTGPWDx bits
bit 11		Unimplemented: Read as '0'
bit 10		PTGSWT: PTG Software Trigger bit ⁽²⁾
		1 = Triggers the PTG module
		0 = No action (clearing this bit will have no effect)
bit 9		PTGSSEN: PTG Enable Single-Step bit ⁽³⁾
		1 = Enables Single-Step mode
		0 = Disables Single-Step mode
bit 8		PTGIVIS: PTG Counter/Timer Visibility Control bit
		1 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the current values of their corresponding counter/timer registers (PTGSD, PTGCx, PTGTx)
		 Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the value previously written to those limit registers
bit 7		PTGSTRT: PTG Start Sequencer bit
		1 = Starts to sequentially execute commands (Continuous mode)0 = Stops executing commands
bit 6		PTGWDTO: PTG Watchdog Timer Time-out Status bit
		1 = PTG Watchdog Timer has timed out
		0 = PTG watchdog Timer has not timed out.
bit 5-2		Unimplemented: Read as '0'
Note	1: Th	nese bits apply to the PTGWHI and PTGWLO commands only.
	2: Th	is bit is only used with the PTGCTRL step command software trigger option.

3: Use of the PTG Single-Step mode is reserved for debugging tools only.

bit 0

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER (CONTINUED)

- PTGITM<1:0>: PTG Input Trigger Command Operating Mode bits⁽¹⁾
 - 11 = Single level detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
 - 10 = Single level detect with Step delay executed on exit of command
 - 01 = Continuous edge detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
 - 00 = Continuous edge detect with Step delay executed on exit of command
- Note 1: These bits apply to the PTGWHI and PTGWLO commands only.

bit 1-0

- **2:** This bit is only used with the PTGCTRL step command software trigger option.
- **3:** Use of the PTG Single-Step mode is reserved for debugging tools only.

Base Instr #	Assembly Mnemonic	/ Assembly Syntax		Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
25	DAW	DAW	Wn	Wn = decimal adjust Wn	1	1	С
26	DEC	DEC	f	f = f - 1	1	1	C,DC,N,OV,Z
		DEC	f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws - 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2	f	f = f – 2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws - 2	1	1	C,DC,N,OV,Z
28	DISI	DISI	#lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF	Wm, Wn ⁽¹⁾	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO	#lit15,Expr ⁽¹⁾	Do code to PC + Expr, lit15 + 1 times	2	2	None
		DO	Wn, Expr ⁽¹⁾	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED	Wm*Wm,Acc,Wx,Wy,Wxd ⁽¹⁾	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB
33	EDAC	EDAC	Wm*Wm,Acc,Wx,Wy,Wxd ⁽¹⁾	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB
34	EXCH	EXCH	Wns,Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL	Ws,Wnd	Find Bit Change from Left (MSb) Side	1	1	С
36	FF1L	FF1L	Ws,Wnd	Find First One from Left (MSb) Side	1	1	С
37	FF1R	FF1R	Ws,Wnd	Find First One from Right (LSb) Side	1	1	С
38	GOTO	GOTO	Expr	Go to address	2	4	None
		GOTO	Wn	Go to indirect	1	4	None
		GOTO.L	Wn	Go to indirect (long address)	1	4	None
39	INC	INC	f	f = f + 1	1	1	C,DC,N,OV,Z
		INC	f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC	Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
40	INC2	INC2	f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2	f,WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2	Ws,Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
41	IOR	IOR	f	f = f .IOR. WREG	1	1	N,Z
		IOR	f,WREG	WREG = f.IOR. WREG	1	1	N,Z
		IOR	#lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N,Z
42	LAC	LAC	Wso,#Slit4,Acc	Load Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
43	LNK	LNK	#lit14	Link Frame Pointer	1	1	SFA
44	LSR	LSR	f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR f, WREG WREG = Logical Right Shift f		1	1	C,N,OV,Z	
		LSR	Ws,Wd	Wd = Logical Right Shift Ws		1	C,N,OV,Z
		LSR	Wb,Wns,Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR	Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB ⁽¹⁾	Multiply and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
		MAC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd ⁽¹⁾	Square and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias	40°C to +125°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to Vss ⁽³⁾	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when $VDD \ge 3.0V^{(3)}$	0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when $VDD < 3.0V^{(3)}$	-0.3V to +3.6V
Maximum current out of Vss pin	
Maximum current into VDD pin ⁽²⁾	
Maximum current sunk/sourced by any 4x I/O pin	
Maximum current sunk/sourced by any 8x I/O pin	25 mA
Maximum current sunk by all ports ^(2,4)	200 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
 - 2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).
 - 3: See the "Pin Diagrams" section for the 5V tolerant pins.
 - 4: Exceptions are: dsPIC33EPXXXGP502, dsPIC33EPXXXMC202/502 and PIC24EPXXXGP/MC202 devices, which have a maximum sink/source capability of 130 mA.





FIGURE 30-10: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)



TABLE 30-29: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Min. Typ. Max. Units Conditi				
MP10	TFPWM	PWMx Output Fall Time	_	—		ns	See Parameter DO32	
MP11	TRPWM	PWMx Output Rise Time	—	_		ns	See Parameter DO31	
MP20	TFD	Fault Input ↓ to PWMx I/O Change	-		15	ns		
MP30	Tfh	Fault Input Pulse Width	15	—		ns		

Note 1: These parameters are characterized but not tested in manufacturing.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X



FIGURE 30-34: ECAN_x MODULE I/O TIMING CHARACTERISTICS

TABLE 30-51: ECANx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions
CA10	TIOF	Port Output Fall Time		_	_	ns	See Parameter DO32
CA11	TIOR	Port Output Rise Time		_	_	ns	See Parameter DO31
CA20	TCWF	Pulse Width to Trigger CAN Wake-up Filter	120			ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 30-35: UARTX MODULE I/O TIMING CHARACTERISTICS



TABLE 30-52: UARTX MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions
UA10	TUABAUD	UARTx Baud Time	66.67	_	_	ns	
UA11	FBAUD	UARTx Baud Frequency	—	—	15	Mbps	
UA20	TCWF	Start Bit Pulse Width to Trigger UARTx Wake-up	500	_	_	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A

	Units		MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	
Number of Pins	Ν	36			
Number of Pins per Side	ND	10			
Number of Pins per Side	NE	8			
Pitch	е	0.50 BSC			
Overall Height	А	0.80	0.90	1.00	
Standoff	A1	0.025	-	0.075	
Overall Width	E	5.00 BSC			
Exposed Pad Width	E2	3.60	3.75	3.90	
Overall Length	D	5.00 BSC			
Exposed Pad Length	D2	3.60	3.75	3.90	
Contact Width	b	0.20	0.25	0.30	
Contact Length	L	0.20	0.25	0.30	
Contact-to-Exposed Pad	K	0.20	-	-	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

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TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description		
Section 30.0 "Electrical Characteristics"	Removed Voltage on VCAP with respect to Vss and added Note 5 in Absolute Maximum Ratings ⁽¹⁾ .		
	Removed Parameter DC18 (VCORE) and Note 3 from the DC Temperature and Voltage Specifications (see Table 30-4).		
	Updated Note 1 in the DC Characteristics: Operating Current (IDD) (see Table 30-6).		
	Updated Note 1 in the DC Characteristics: Idle Current (IIDLE) (see Table 30-7).		
	Changed the Typical values for Parameters DC60a-DC60d and updated Note 1 in the DC Characteristics: Power-down Current (IPD) (see Table 30-8).		
	Updated Note 1 in the DC Characteristics: Doze Current (IDOZE) (see Table 30-9).		
	Updated Note 2 in the Electrical Characteristics: BOR (see Table 30-12).		
	Updated Parameters CM20 and CM31, and added Parameters CM44 and CM45 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14).		
	Added the Op amp/Comparator Reference Voltage Settling Time Specifications (see Table 30-15).		
	Added Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16).		
	Updated Internal FRC Accuracy Parameter F20a (see Table 30-21).		
	Updated the Typical value and Units for Parameter CTMUI1, and added Parameters CTMUI4, CTMUFV1, and CTMUFV2 to the CTMU Current Source Specifications (see Table 30-55).		
Section 31.0 "Packaging Information"	Updated packages by replacing references of VLAP with TLA.		
"Product Identification System"	Changed VLAP to TLA.		