



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gp504-e-mv

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.0 CPU

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "CPU" (DS70359) in the "dsPIC33/PIC24 Family Reference Manual', which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

3.1 Registers

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can act as a data, address or address offset register. The 16th working register (W15) operates as a Software Stack Pointer for interrupts and calls.

3.2 Instruction Set

The instruction set for dsPIC33EPXXXGP50X and dsPIC33EPXXXMC20X/50X devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. The instruction set for PIC24EPXXXGP/MC20X devices has the MCU class of instructions only and does not support DSP instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3 Data Space Addressing

The base Data Space can be addressed as 64 Kbytes (32K words).

The Data Space includes two ranges of memory, referred to as X and Y data memory. Each memory range is accessible through its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Spaces have memory locations that are device-specific, and are described further in the data memory maps in **Section 4.2 "Data Address Space"**.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space (PS) at any 32-Kbyte aligned program word boundary. The Program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to the "**Data Memory**" (DS70595) and "**Program Memory**" (DS70613) sections in the "*dsPIC33/PIC24 Family Reference Manual*" for more details on EDS, PSV and table accesses.

On the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data re-ordering for radix-2 FFT algorithms. PIC24EPXXXGP/MC20X devices do not support Modulo and Bit-Reversed Addressing.

3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- · Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

4.2.5 X AND Y DATA SPACES

The dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X core has two Data Spaces, X and Y. These Data Spaces can be considered either separate (for some DSP instructions) or as one unified linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X Data Space is used by all instructions and supports all addressing modes. X Data Space has separate read and write data buses. The X read data bus is the read data path for all instructions that view Data Space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y Data Space is used in concert with the X Data Space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY. N and MSC) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X Data Space. Modulo Addressing and Bit-Reversed Addressing are not present in PIC24EPXXXGP/MC20X devices.

All data memory writes, including in DSP instructions, view Data Space as combined X and Y address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

4.3 Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

4.3.1 KEY RESOURCES

- "Program Memory" (DS70613) in the "dsPIC33/ PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	_	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—		—		_	—	—	-	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	_		—		QEI1IF	PSEMIF	—		—		—		MI2C2IF	SI2C2IF		0000
IFS4	0808	_	-	CTMUIF	_		—	_	_		C1TXIF		_	CRCIF	U2EIF	U1EIF		0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—	_	—	—	—	_	—	—	_	0000
IFS6	080C	—	—	—	—	—	—	—	—	_	—	—	—	_	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF		_		—	_	_		_		_		—	—		0000
IFS9	0812	_	-		_		—	_	_		PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF		0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	_	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	_	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	QEI1IE	PSEMIE	—	_	—	—	—	_	MI2C2IE	SI2C2IE	_	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	_	C1TXIE	—	—	CRCIE	U2EIE	U1EIE	_	0000
IEC5	082A	PWM2IE	PWM1IE	_	—	_	—	—	—	_	—	_	—	_	_	—	_	0000
IEC6	082C	—	—	_	—	_	—	—	—	_	—	_	—	_	_	—	PWM3IE	0000
IEC7	082E	—	—	_	—	_	—	—	—	_	—	_	—	_	—	—	_	0000
IEC8	0830	JTAGIE	ICDIE	_	—	_	—	—	—	_	—	_	—	_	—	—	_	0000
IEC9	0832	—	—	_	—	_	—		—	_	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	_	0000
IPC0	0840	—		T1IP<2:0>		_		OC1IP<2:0)>	_	IC1IP<2:0>		_	- INT0IP<2:0>			4444	
IPC1	0842	—		T2IP<2:0>		_		OC2IP<2:0)>	_		IC2IP<2:0>		_	DMA0IP<2:0>			4444
IPC2	0844	—		U1RXIP<2:0)>	_		SPI1IP<2:0)>	_		SPI1EIP<2:0	>	_		T3IP<2:0>		4444
IPC3	0846	—	—	_	—	_	0)MA1IP<2:	0>	_		AD1IP<2:0>		_		U1TXIP<2:0>		0444
IPC4	0848			CNIP<2:0>		_		CMIP<2:0	>			MI2C1IP<2:0	>	_	:	SI2C1IP<2:0>		4444
IPC5	084A	—	—	_	—	_	—		—	_	—	_	—	_		INT1IP<2:0>		0004
IPC6	084C	—		T4IP<2:0>		_		OC4IP<2:0)>	_		OC3IP<2:0>		_	1	DMA2IP<2:0>		4444
IPC7	084E	—		U2TXIP<2:0	>	_	ι	J2RXIP<2:(0>	_		INT2IP<2:0>		_		T5IP<2:0>		4444
IPC8	0850	—		C1IP<2:0>	-	_	0	C1RXIP<2:(0>	_		SPI2IP<2:0>		_		SPI2EIP<2:0>		4444
IPC9	0852	—	—	_	—	_		IC4IP<2:0	>	_		IC3IP<2:0>		_	1	DMA3IP<2:0>		0444
IPC12	0858	—	—	_	—	_	N	112C2IP<2:	0>	_		SI2C2IP<2:0	>	_	—	—	_	0440
IPC14	085C	—	_	—	—	—	(QEI1IP<2:0)>	_		PSEMIP<2:0	>	—	—	—	—	0440
IPC16	0860	_		CRCIP<2:0	>	_		U2EIP<2:0	>	_		U1EIP<2:0>		_	_	_	_	4440
IPC17	0862	_	—	_	—	_	(C1TXIP<2:0	0>	_	—	—	—	_	_	_	_	0400
IPC19	0866	—	—	_	—	_	—	—	—	_		CTMUIP<2:0	>	_	—	—	_	0040

TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

DS70000657H-page 73

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTGCST	0AC0	PTGEN		PTGSIDL	PTGTOGL	_	PTGSWT	PTGSSEN	PTGIVIS	PTGSTRT	PTGWTO	_	_	—	—	PTGIT	M<1:0>	0000
PTGCON	0AC2	PTGCLK<2:0> PTGDIV<4:0>						PTGPWD<3:0> — PTGWDT<2:0>					0>	0000				
PTGBTE	0AC4		ADCTS<4:1> IC4TSS IC3TSS IC2TSS IC1TSS						OC4CS	OC3CS	OC2CS	OC1CS	OC4TSS	OC3TSS	OC2TSS	OC1TSS	0000	
PTGHOLD	0AC6	PTGHOLD<15:0>														0000		
PTGT0LIM	0AC8		PTGT0LIM<15:0> 0C											0000				
PTGT1LIM	0ACA								PTGT1LIN	1<15:0>								0000
PTGSDLIM	0ACC								PTGSDLIN	1<15:0>								0000
PTGC0LIM	0ACE		PTGC0LIM<15:0> 00											0000				
PTGC1LIM	0AD0								PTGC1LIN	1<15:0>								0000
PTGADJ	0AD2								PTGADJ•	<15:0>								0000
PTGL0	0AD4								PTGL0<	15:0>								0000
PTGQPTR	0AD6	_	_	_	_	_	_	_	_	_	_	_		P	TGQPTR<4	4:0>		0000
PTGQUE0	0AD8				STEP	21<7:0>				STEP0<7:0>						0000		
PTGQUE1	0ADA				STEP	93<7:0>							STEP2	2<7:0>				0000
PTGQUE2	0ADC				STEP	95<7:0>							STEP4	<7:0>				0000
PTGQUE3	0ADE				STEP	7<7:0>							STEP6	6<7:0>				0000
PTGQUE4	0AE0				STEP	9<7:0>							STEP8	3<7:0>				0000
PTGQUE5	0AE2				STEP	11<7:0>							STEP1	0<7:0>				0000
PTGQUE6	0AE4				STEP	13<7:0>							STEP1	2<7:0>				0000
PTGQUE7	0AE6				STEP	15<7:0>							STEP1	4<7:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

DS70000657H-page 78

4.4.1 PAGED MEMORY SCHEME

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre-modified and post-modified Effective Addresses (EA). The upper half of the base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Read Page register (DSRPAG) or the 9-bit Write Page register (DSWPAG), to form an Extended Data Space (EDS) address or Program Space Visibility (PSV) address. The Data Space Page registers are located in the SFR space.

Construction of the EDS address is shown in Example 4-1. When DSRPAG<9> = 0 and the base address bit, EA<15> = 1, the DSRPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit EDS read address. Similarly, when base address bit, EA<15> = 1, DSWPAG<8:0> are concatenated onto EA<14:0> to form the 24-bit EDS write address.





4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- · Register Indirect
- · Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal
- Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

5.2 RTSP Operation

RTSP allows the user application to erase a single page of memory and to program two instruction words at a time. See the General Purpose and Motor Control Family tables (Table 1 and Table 2, respectively) for the page sizes of each device.

For more information on erasing and programming Flash memory, refer to "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual".

5.3 **Programming Operations**

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

For erase and program times, refer to Parameters D137a and D137b (Page Erase Time), and D138a and D138b (Word Write Cycle Time) in Table 30-14 in **Section 30.0 "Electrical Characteristics"**.

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of program Flash memory at a time on every other word address boundary (0x000002, 0x000006, 0x00000A, etc.). To do this, it is necessary to erase the page that contains the desired address of the location the user wants to change.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPS.

Refer to **Flash Programming**" (DS70609) in the "*dsPIC33/PIC24 Family Reference Manual*" for details and codes examples on programming using RTSP.

5.4 Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

5.4.1 KEY RESOURCES

- "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

5.5 Control Registers

Four SFRs are used to erase and write the program Flash memory: NVMCON, NVMKEY, NVMADRH and NVMADRL.

The NVMCON register (Register 5-1) enables and initiates Flash memory erase and write operations.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRH and NVMADRL. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word for programming operations or the selected page for erase operations.

The NVMADRH register is used to hold the upper 8 bits of the EA, while the NVMADRL register is used to hold the lower 16 bits of the EA.

	Vector	IRQ		Inte	errupt Bit L	ocation	
Interrupt Source	#	#	IVI Address	Flag	Enable	Priority	
QEI1 – QEI1 Position Counter Compare ⁽²⁾	66	58	0x000088	IFS3<10>	IEC3<10>	IPC14<10:8>	
Reserved	67-72	59-64	0x00008A-0x000094	_	_	—	
U1E – UART1 Error Interrupt	73	65	0x000096	IFS4<1>	IEC4<1>	IPC16<6:4>	
U2E – UART2 Error Interrupt	74	66	0x000098	IFS4<2>	IEC4<2>	IPC16<10:8>	
CRC – CRC Generator Interrupt	75	67	0x00009A	IFS4<3>	IEC4<3>	IPC16<14:12>	
Reserved	76-77	68-69	0x00009C-0x00009E	_	_	—	
C1TX – CAN1 TX Data Request ⁽¹⁾	78	70	0x000A0	IFS4<6>	IEC4<6>	IPC17<10:8>	
Reserved	79-84	71-76	0x0000A2-0x0000AC	_	_	_	
CTMU – CTMU Interrupt	85	77	0x0000AE	IFS4<13>	IEC4<13>	IPC19<6:4>	
Reserved	86-101	78-93	0x0000B0-0x0000CE	_	_	—	
PWM1 – PWM Generator 1 ⁽²⁾	102	94	0x0000D0	IFS5<14>	IEC5<14>	IPC23<10:8>	
PWM2 – PWM Generator 2 ⁽²⁾	103	95	0x0000D2	IFS5<15>	IEC5<15>	IPC23<14:12>	
PWM3 – PWM Generator 3 ⁽²⁾	104	96	0x0000D4	IFS6<0>	IEC6<0>	IPC24<2:0>	
Reserved	105-149	97-141	0x0001D6-0x00012E	—	—	—	
ICD – ICD Application	150	142	0x000142	IFS8<14>	IEC8<14>	IPC35<10:8>	
JTAG – JTAG Programming	151	143	0x000130	IFS8<15>	IEC8<15>	IPC35<14:12>	
Reserved	152	144	0x000134	—	—	—	
PTGSTEP – PTG Step	153	145	0x000136	IFS9<1>	IEC9<1>	IPC36<6:4>	
PTGWDT – PTG Watchdog Time-out	154	146	0x000138	IFS9<2>	IEC9<2>	IPC36<10:8>	
PTG0 – PTG Interrupt 0	155	147	0x00013A	IFS9<3>	IEC9<3>	IPC36<14:12>	
PTG1 – PTG Interrupt 1	156	148	0x00013C	IFS9<4>	IEC9<4>	IPC37<2:0>	
PTG2 – PTG Interrupt 2	157	149	0x00013E	IFS9<5>	IEC9<5>	IPC37<6:4>	
PTG3 – PTG Interrupt 3	158	150	0x000140	IFS9<6>	IEC9<6>	IPC37<10:8>	
Reserved	159-245	151-245	0x000142-0x0001FE	_	_	_	
	Lowe	est Natura	I Order Priority				

TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

Note 1: This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

2: This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/S-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
FORCE ⁽¹⁾	—	—	_	_	—	—	—				
bit 15		·			·		bit 8				
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
IRQSEL7	IRQSEL7 IRQSEL6		IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0				
bit 7		•			·		bit 0				
Legend:		S = Settable b	oit								
R = Readable	bit	W = Writable	W = Writable bit U = Unimplemented bit, read as '0'								
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown					
bit 15	FORCE: Forc	e DMA Transfe	er bit ⁽¹⁾								
	1 = Forces a	single DMA tra	insfer (Manua	l mode)							
	0 = Automati	c DMA transfer	initiation by D	MA request							
bit 14-8	Unimplemen	ted: Read as '	י)								
bit 7-0	IRQSEL<7:0>	-: DMA Periphe	eral IRQ Numl	ber Select bits							
	01000110 =	ECAN1 – TX D	ata Request ⁽²	2)							
	00100110 =	IC4 – Input Caj	oture 4								
	00100101 =	IC3 – Input Ca	oture 3								
	00100010 =	ECAN1 – RX D	Data Ready(2)								
	00100001 = 3	SPIZ Transfer I	Jone NDT2 Transmi	ittor							
	00011111 =	UART2RX – UART2 Receiver									
	0001110 = 00011100 = 000011100 = 000011000 = 00000000	TMR5 – Timer	5								
	00011011 =	TMR4 – Timer4	1								
	00011010 =	OC4 – Output	Compare 4								
	00011001 =	OC3 – Output (Compare 3								
	00001101 =	ADC1 – ADC1	Convert done	•							
	00001100 =	UART1TX – U/	ART1 Transm	itter							
	00001011 =	UART1RX – U	ART1 Receive	er							
	00001010 =	SPI1 – Transfe	r Done								
	00001000 =	TMR3 – Timera	3								
	00000111 =	100RZ - 100RZ	<u>Compore 2</u>								
	00000110 = 0	IC2 – Duipui V	oture 2								
	00000101 = 0	OC1 = Outout 0	Compare 1								
	00000001 =	IC1 – Input Ca	oture 1								
	00000000 =	INT0 – Externa	I Interrupt 0								

REGISTER 8-2: DMAXREQ: DMA CHANNEL x IRQ SELECT REGISTER

- **Note 1:** The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).
 - 2: This selection is available in dsPIC33EPXXXGP/MC50X devices only.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
_	—	—	_	—	PWM3MD ⁽¹⁾	PWM2MD ⁽¹⁾	PWM1MD ⁽¹⁾	
bit 15							bit 8	
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
—	—		_		_			
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit			bit	U = Unimplen	nented bit, read	l as '0'		
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unknown		
bit 15-11	Unimplemen	ted: Read as '	0'					
bit 10	PWM3MD: P	WM3 Module D)isable bit ⁽¹⁾					
	1 = PWM3 mo	odule is disable	ed					
	0 = PWM3 mo	odule is enable	d					
bit 9	PWM2MD: P	WM2 Module D	isable bit ⁽¹⁾					
	1 = PWM2 mo	odule is disable	ed					
	0 = PWM2 mc	odule is enable	d					
bit 8	PWM1MD: P	WM1 Module D	isable bit ⁽¹⁾					
	1 = PWM1 mo	odule is disable	ed					
	0 = PWM1 mo	odule is enable	d					
bit 7-0	Unimplemen	ted: Read as '	0'					

REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

Note 1: This bit is available on dsPIC33EPXXXMC50X/20X and PIC24EPXXXMC20X devices only.

11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx and TRISx registers for data control, port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs other than VDD by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum VIH specification for that particular pin.

See the **"Pin Diagrams"** section for the available 5V tolerant pins and Table 30-11 for the maximum VIH specification for each pin.

11.2 Configuring Analog and Digital Port Pins

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of analog in the Pinout I/O Descriptions (see Table 1-1).

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or comparator module.

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP, as shown in Example 11-1.

11.3 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the Change Notification (CN) functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups and pulldowns act as a current source or sink source connected to the pin and eliminate the need for external resistors when push button, or keypad devices are connected. The pull-ups and pull-downs are enabled separately, using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note:	Pull-ups and pull-downs on Change Noti-
	fication pins should always be disabled
	when the port pin is configured as a digital
	output.

EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

MOV	0xFF00, W0	; Configure PORTB<15:8>
		; as inputs
MOV	W0, TRISB	; and PORTB<7:0>
		; as outputs
NOP		; Delay 1 cycle
BTSS	PORTB, #13	; Next Instruction

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
_				IC4R<6:0>									
bit 15							bit 8						
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0						
_				IC3R<6:0>									
bit 7							bit 0						
Legend:													
R = Readat	ole bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'							
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown						
bit 15	Unimpleme	ented: Read as '	0'										
bit 14-8	IC4R<6:0>: (see Table 2	IC4R<6:0>: Assign Input Capture 4 (IC4) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)											
	1111001 =	1111001 = Input tied to RPI121											
	•												
	•												
	0000001 =	Input tied to CM	P1										
bit 7		nput tied to vss	, 0,										
bit 6-0		Assign Input Ca	o unture 3 (IC3)) to the Correspo	ondina RPn P	in hits							
bit 0 0	(see Table 1	11-2 for input pin	selection nu	mbers)		in bits							
	1111001 =	Input tied to RPI	121	,									
	•												
	0000001 =	Input tied to CM	P1										
	0000000 =	Input tied to Vss	5										

REGISTER 11-5: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

REGISTER 11-8: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
				QEB1R<6:0>	•					
bit 15							bit 8			
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
				QEA1R<6:0>	•					
bit 7							bit 0			
Legend:	-1:+		L :4							
R = Readad		VV = VVritable bit		U = Unimplemented bit, rea						
-n = Value a	at POR	'1' = Bit is set		0° = Bit is clea	ared	x = Bit is unknown				
bit 15	Unimplome	ntod: Dood os '	0'							
		nteu: Reau as			- Dia kita					
DIL 14-8	(see Table 1	QEB1R<6:0>: Assign B (QEB) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)								
	1111001 =	1111001 = Input tied to RPI121								
	•									
	•									
	0000001 =	0000001 = Input tied to CMP1								
	0000000 =	Input tied to Vss	5							
bit 7	Unimpleme	ented: Read as '	0'							
bit 6-0	QEA1R<6:0	D>: Assign A (QE	EA) to the Cor	responding RP	n Pin bits					
	(see Table ?	(see Table 11-2 for input pin selection numbers)								
	1111001 =	Input tied to RPI	121							
	•									
	0000001 =	Input tied to CM	P1							
	0000000 =	Input tied to Vss	5							



FIGURE 13-3: TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)

3: Timery is a Type C timer (y = 3 and 5).

Timerx/y Resources 13.1

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/
	wwwproducts/Devices.aspx?d
	DocName=en555464

KEY RESOURCES 13.1.1

- "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- · Software Libraries
- · Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

						D 444 A				
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
-	—	—	DISSCK	DISSDO	MODE16	SMP	CKE(")			
bit 15							bit 8			
		DAAUO		DAMA		DAM 0				
	2) R/VV-U	R/W-U		R/W-U	R/W-0		R/W-0			
SSEN ⁽⁴⁾ CKP MSTEN SPRE2 ⁽³⁾ SPRE1 ⁽³⁾ SPRE0 ⁽³⁾ PPR						PPRET	PPREU			
DIT 7							DITU			
Legend:										
R = Read	able bit	W = Writable	bit	U = Unimpler	mented bit read	1 as '0'				
-n = Value	at POR	(1) = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown				
			•	0 2.1.10 0.10						
bit 15-13	Unimplemer	nted: Read as '	0'							
bit 12	DISSCK: Dis	able SCKx Pin	bit (SPIx Mas	ter modes only	<i>'</i>)					
	1 = Internal S	SPIx clock is dis	sabled, pin fun	ctions as I/O						
	0 = Internal S	SPIx clock is er	abled							
bit 11	DISSDO: Dis	able SDOx Pir	ı bit							
	1 = SDOx pir	n is not used by	the module; p	oin functions as	s I/O					
bit 10		ord/Byte Com	y the moutle	oct bit						
1 = Communication is word-wide (16 bits)										
	0 = Commun	ication is byte-	wide (8 bits)							
bit 9	SMP: SPIx D	ata Input Sam	ole Phase bit							
	Master mode	<u>):</u>								
	1 = Input dat	a is sampled at	end of data of	utput time						
	0 – Input data Slave mode:	a is sampled at		a output time						
	SMP must be	e cleared when	SPIx is used i	n Slave mode.						
bit 8	CKE: SPIx C	lock Edge Sele	ect bit ⁽¹⁾							
	1 = Serial ou	tput data chang	ges on transitio	on from active	clock state to Id	lle clock state (i	refer to bit 6)			
	0 = Serial ou	tput data chang	ges on transitio	on from Idle clo	ock state to activ	ve clock state (refer to bit 6)			
bit 7 SSEN: Slave Select Enable bit (Slave mode) ⁽²⁾										
	$1 = \frac{SSx}{SSx}$ pin is	s used for Slav	e mode he module: nir	is controlled h	w port function					
bit 6	o = 55x pin is not used by the module, pin is controlled by port function									
1 = Idle state for clock is a high level: active state is a low level										
	0 = Idle state	for clock is a l	ow level; active	e state is a higl	h level					
bit 5 MSTEN: Master Mode Enable bit										
	1 = Master m	1 = Master mode								
	0 = Slave mo	ode								
Note 1:	The CKE bit is not	used in Frame	d SPI modes. I	Program this bi	t to '0' for Fram	ed SPI modes (FRMEN = 1).			
2:	2: This bit must be cleared when FRMEN = 1.									

REGISTER 18-2: SPIXCON1: SPIX CONTROL REGISTER 1

- **3:** Do not set both primary and secondary prescalers to the value of 1:1.

20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "UART" (DS70582) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X family of devices contains two UART modules.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the UxCTS and UxRTS pins, and also includes an IrDA[®] encoder and decoder.

Note: <u>Hardware</u> flow control using UxRTS and UxCTS is not available on all pin count devices. See the "**Pin Diagrams**" section for availability.

The primary features of the UARTx module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with UxCTS and UxRTS Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 4.375 Mbps to 67 bps at 16x mode at 70 MIPS
- Baud Rates Ranging from 17.5 Mbps to 267 bps at 4x mode at 70 MIPS
- 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- · Transmit and Receive Interrupts
- A Separate Interrupt for all UARTx Error Conditions
- · Loopback mode for Diagnostic Support
- · Support for Sync and Break Characters
- Support for Automatic Baud Rate Detection
- IrDA[®] Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UARTx module is shown in Figure 20-1. The UARTx module consists of these key hardware elements:

- · Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

FIGURE 20-1: UARTx SIMPLIFIED BLOCK DIAGRAM



© 2011-2013 Microchip Technology Inc.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB		_	CH0SB4 ⁽¹⁾	CH0SB3 ⁽¹⁾	CH0SB2 ⁽¹⁾	CH0SB1 ⁽¹⁾	CH0SB0 ⁽¹⁾
bit 15	bit 15						
R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA		_	CH0SA4 ⁽¹⁾	CH0SA3 ⁽¹⁾	CH0SA2 ⁽¹⁾	CH0SA1 ⁽¹⁾	CH0SA0 ⁽¹⁾
bit 7							bit 0
Legend:							
R = Read	able bit	W = Writable b	bit	U = Unimpler	nented bit. read	as '0'	
-n = Value	at POR	'1' = Bit is set		 O' = Bit is cleared 		x = Bit is unknown	
bit 15	CHONB. Cha	nnel () Negative	Innut Select fo	r Sample MLIX	(B hit		
Sit 10	1 = Channel (negative input	is AN1(1)				
	0 = Channel (0 negative input	is Vrefl				
bit 14-13	Unimplemen	ted: Read as '0'					
bit 12-8	CH0SB<4:0>	Channel 0 Pos	itive Input Sele	ect for Sample	MUXB bits ⁽¹⁾		
	11111 = Ope	en; use this seled	tion with CTM	U capacitive ar	nd time measure	ement	
	11110 = Cha	nnel 0 positive inp	out is connected	to the CTMU te	emperature mea	surement diode	(CTMU TEMP)
	11101 = Res	erved					
	11100 = Res	erved					
	11011 = Res 11010 = Cha	innel 0 positive ir	nout is the outp	out of OA3/AN6	_ວ (2,3)		
	11001 = Cha	innel 0 positive ir	nput is the outp	out of OA2/AN	(2)		
	11000 = Cha	innel 0 positive ir	nput is the outp	out of OA1/AN3	₃ (2)		
	10111 = Res	erved					
	•						
	•						
	10000 = Res	erved					
	01111 = Cha	innel 0 positive ir	1put is AN15 ⁽³⁾				
	01110 = Cha	innel 0 positive ir	1put is AN14(°)				
	•		iput is AN 15.				
	•						
	•		(2)				
	00010 = Cha	innel 0 positive ir	nput is $AN2^{(3)}$				
	00001 = Cha	innel 0 positive ir	$\frac{1000 \text{ is AN } (3)}{1000 \text{ is AN } (3)}$				
hit 7	CHONA: Cha	nnel 0 Negative	Input Select fo	r Samole MLIX	(A hit		
	1 = Channel (negative input	is ANI1(1)				
	0 = Channel (0 negative input	is Vrefl				
bit 6-5	bit 6-5 Unimplemented: Read as '0'						
Net: 4		17				in an alt of C	
Note 1:	ANU through AN	v are repurpose	a wnen compa ticular on amn	arator and op a	mp runctionality	is enabled. Se	e ⊢igure 23-1
	and 3.		uculai op amp				1, 2
2:	The OAx input is	s used if the corr	esponding op	amp is selecte	d (OPMODE (C	MxCON<10>) =	= 1);

REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER

3: See the "**Pin Diagrams**" section for the available analog channels for each device.

otherwise, the ANx input is used.

Bit Field	Description
GCP	General Segment Code-Protect bit 1 = User program memory is not code-protected 0 = Code protection is enabled for the entire program memory space
GWRP	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	 Two-Speed Oscillator Start-up Enable bit 1 = Start up device with FRC, then automatically switch to the user-selected oscillator source when ready 0 = Start up device with user-selected oscillator source
PWMLOCK ⁽¹⁾	PWM Lock Enable bit 1 = Certain PWM registers may only be written after a key sequence 0 = PWM registers may be written without a key sequence
FNOSC<2:0>	Oscillator Selection bits 111 = Fast RC Oscillator with Divide-by-N (FRCDIVN) 110 = Fast RC Oscillator with Divide-by-16 (FRCDIV16) 101 = Low-Power RC Oscillator (LPRC) 100 = Reserved; do not use 011 = Primary Oscillator with PLL module (XT + PLL, HS + PLL, EC + PLL) 010 = Primary Oscillator (XT, HS, EC) 001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCPLL) 000 = Fast RC Oscillator (FRC)
FCKSM<1:0>	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	Peripheral Pin Select Configuration bit 1 = Allow only one reconfiguration 0 = Allow multiple reconfigurations
OSCIOFNC	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is a general purpose digital I/O pin
POSCMD<1:0>	Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode
FWDTEN	 Watchdog Timer Enable bit 1 = Watchdog Timer is always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.) 0 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)
WINDIS	Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode
PLLKEN	PLL Lock Enable bit 1 = PLL lock is enabled 0 = PLL lock is disabled

TABLE 27-2: CONFIGURATION BITS DESCRIPTION

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

2: When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

DC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	am o. Symbol Characteristic			Тур.	Max.	Units	Conditions
	lı∟	Input Leakage Current ^(1,2)					
DI50		I/O Pins 5V Tolerant ⁽³⁾	-1	—	+1	μA	$Vss \le VPIN \le VDD$, Pin at high-impedance
DI51		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	$\label{eq:VSS} \begin{split} &Vss \leq V \text{PIN} \leq V \text{DD}, \\ &\text{Pin at high-impedance}, \\ &-40^\circ\text{C} \leq \text{TA} \leq +85^\circ\text{C} \end{split}$
DI51a		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	Analog pins shared with external reference pins, $-40^{\circ}C \le TA \le +85^{\circ}C$
DI51b		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	$\label{eq:VSS} \begin{array}{l} VSS \leq VPIN \leq VDD, \\ Pin \text{ at high-impedance}, \\ -40^\circC \leq TA \leq +125^\circC \end{array}$
DI51c		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	Analog pins shared with external reference pins, $-40^{\circ}C \le TA \le +125^{\circ}C$
DI55		MCLR	-5	_	+5	μA	$Vss \leq V \text{PIN} \leq V \text{DD}$
DI56		OSC1	-5	_	+5	μA	$\label{eq:VSS} \begin{array}{l} VSS \leq VPIN \leq VDD, \\ XT \text{ and } HS \text{ modes} \end{array}$

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 2: Negative current is defined as current sourced by the pin.
- 3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 4: VIL source < (Vss 0.3). Characterized but not tested.
- **5:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.
- 6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

NOTES: