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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

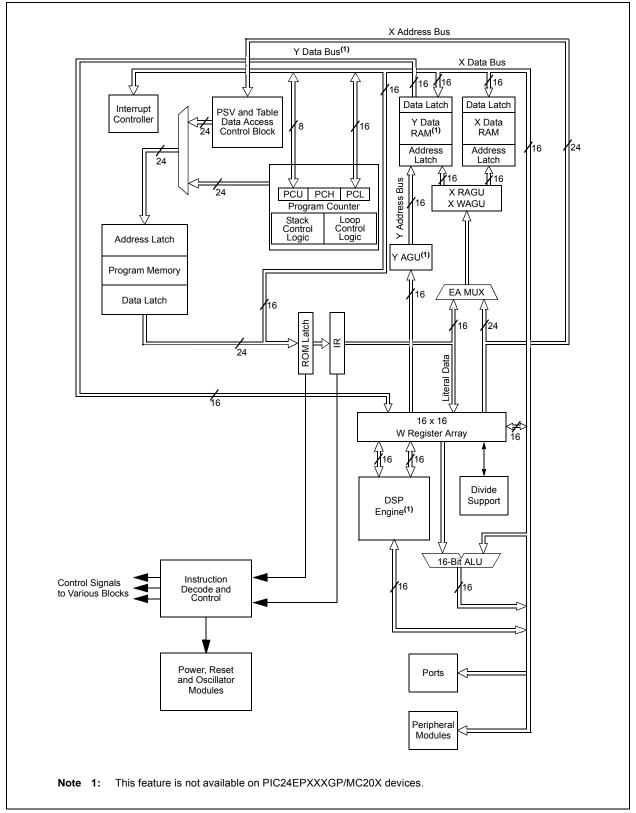
E·XFI

2 0 0 0 0 0 0	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gp504-i-mv

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

FIGURE 3-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X CPU BLOCK DIAGRAM



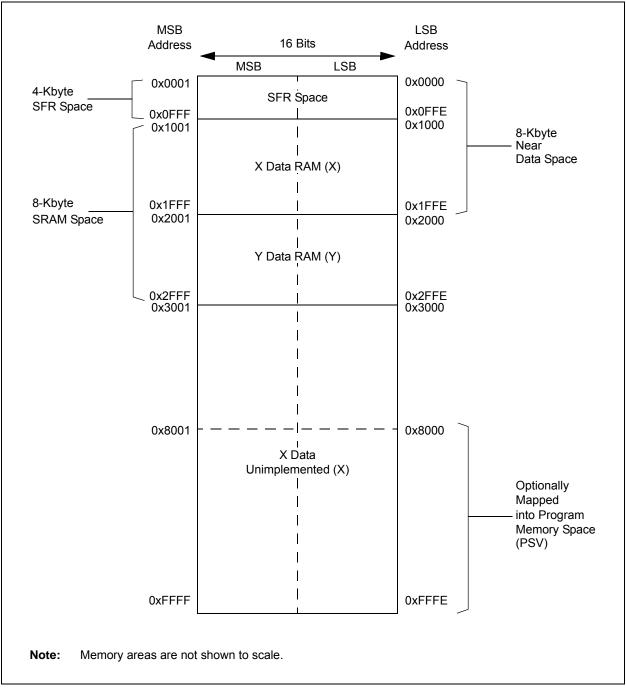


FIGURE 4-8: DATA MEMORY MAP FOR dsPIC33EP64MC20X/50X AND dsPIC33EP64GP50X DEVICES

TABLE 4	4-31:	PER	IPHERA	L PIN S	ELECT	INPUT F	REGISTI	ER MAP	FOR de	sPIC33E	EPXXXG	P50X D	EVICES	SONLY	

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—				INT1R<6:0>				_	_	—	—	—	—	—	_	0000
RPINR1	06A2		_	_	_	_	_	_	_	_				INT2R<6:0>	•			0000
RPINR3	06A6		_	_	_	_	_	_	_	_			٦	[2CKR<6:0	>			0000
RPINR7	06AE					IC2R<6:0>				_				IC1R<6:0>				0000
RPINR8	06B0					IC4R<6:0>				_				IC3R<6:0>				0000
RPINR11	06B6		_	_	_	_	_	_	_	_			(DCFAR<6:0	>			0000
RPINR18	06C4		_	_	_	_	_	_	_	_			ι	J1RXR<6:0	>			0000
RPINR19	06C6		_	_	_	_	_	_	_	_			ι	J2RXR<6:0	>			0000
RPINR22	06CC				S	CK2INR<6:0)>			_	SDI2R<6:0>				0000			
RPINR23	06CE	_	_	_	—	—	_	_	—	—	SS2R<6:0>				0000			
RPINR26	06D4	—	_	_	-	_	_	—		—	C1RXR<6:0>				0000			

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-32: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	_				INT1R<6:0>				—	—	—	—	—	—	—	_	0000
RPINR1	06A2		_	_	_	_	_	_	_	_				INT2R<6:0>				0000
RPINR3	06A6		_	_	_	_	_	_	_	_			-	F2CKR<6:0	>			0000
RPINR7	06AE					IC2R<6:0>				_				IC1R<6:0>				0000
RPINR8	06B0					IC4R<6:0>				_				IC3R<6:0>				0000
RPINR11	06B6		_	_	_	_	_	_	_	_			(DCFAR<6:0	>			0000
RPINR12	06B8					FLT2R<6:0>	•			_				FLT1R<6:0>	•			0000
RPINR14	06BC				(QEB1R<6:0	>			_	QEA1R<6:0>					0000		
RPINR15	06BE				Н	OME1R<6:0)>			_			I	NDX1R<6:0	>			0000
RPINR18	06C4		_	_	_	_	_	_	_	_			ι	J1RXR<6:0	>			0000
RPINR19	06C6		_	_	_	_	_	_	_	_			ι	J2RXR<6:0	>			0000
RPINR22	06CC	_			S	CK2INR<6:()>			—				SDI2R<6:0>	•			0000
RPINR23	06CE	_	—	—		—	—		—	—				SS2R<6:0>				0000
RPINR26	06D4	_	_	_		—	—		—	—			(C1RXR<6:0	>			0000
RPINR37	06EA	_			S	YNCI1R<6:0)>			—					0000			
RPINR38	06EC	_			D	CMP1R<6:	0>			—					0000			
RPINR39	06EE	_			D	FCMP3R<6:	0>			_			D	CMP2R<6:	0>			0000

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0 U-0 U-0 R-0 R-0 R-0 R-0 - - - - RQCOL3 RQCOL2 RQCOL1 RQCOL0 bit 7 - - - RQCOL3 RQCOL2 RQCOL1 RQCOL0 bit 7 - - - RQCOL3 RQCOL2 RQCOL1 RQCOL0 Legend: R Readable bit W = Writable bit U = Unimplemented bit, read as '0' n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15-4 Unimplemented: Read as '0' bit 3 RQCOL3: DMA Channel 3 Transfer Request Collision Flag bit 1 = User force and interrupt-based request collision is detected bit 2 RQCOL2: DMA Channel 2 Transfer Request Collision Flag bit 1 = User force and interrupt-based request collision is detected bit 2 RQCOL2: DMA Channel 2 Transfer Request collision is detected 0 = No request collision is detected bit 2 RQCOL2: DMA Channel 2 Transfer Request collision is detected 0 = No request collision is detected								
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
—	—	—	—	—	—	—	—	
bit 15							bit 8	
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0	
—		—	—	RQCOL3	RQCOL2	RQCOL1	RQCOL0	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'		
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown				
bit 15-4	Unimplemen	ted: Read as '	כ'					
bit 3	RQCOL3: DN	/IA Channel 3 T	ransfer Requ	est Collision F	ag bit			
				st collision is d	etected			
h # 0	•			est Callisian Fl	aa hit			
DIL Z			•		0			
		•			elecieu			
bit 1	RQCOL1: DN	/IA Channel 1 T	ransfer Requ	est Collision F	ag bit			
	1 = User for	e and interrupt	-based reque	st collision is d	etected			
	0 = No reque	est collision is d	etected					
bit 0	RQCOLO: DN	/IA Channel 0 T	ransfer Requ	est Collision F	lag bit			
	1 = User force	e and interrupt	-based reque	st collision is d	etected			

REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER

0 = No request collision is detected

REGISTER 11-7: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				FLT2R<6:0>			
bit 15							bit 8
	D 444 A	D 444 0	D 444 A	Date	D 444 0	DAVA	D # 44 0
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				FLT1R<6:0>			
bit 7							bit C
Legend:							
R = Readabl	le bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 14-8	FLT2R<6:0> (see Table 11	-2 for input pin	Fault 2 (FLT2)) to the Corresp nbers)	onding RPn F	Pin bits	
bit 14-8	FLT2R<6:0> (see Table 11 1111001 = h	: Assign PWM I	Fault 2 (FLT2) selection nur 121		onding RPn F	Pin bits	
bit 14-8	FLT2R<6:0> (see Table 11 1111001 = h	: Assign PWM I I-2 for input pin nput tied to RPI	Fault 2 (FLT2) selection nur 121 P1		onding RPn F	Pin bits	
bit 14-8 bit 7	FLT2R<6:0> (see Table 11 1111001 = h	: Assign PWM I I-2 for input pin nput tied to RPI nput tied to CM	Fault 2 (FLT2 selection nur 121 P1		onding RPn F	Pin bits	

NOTES:

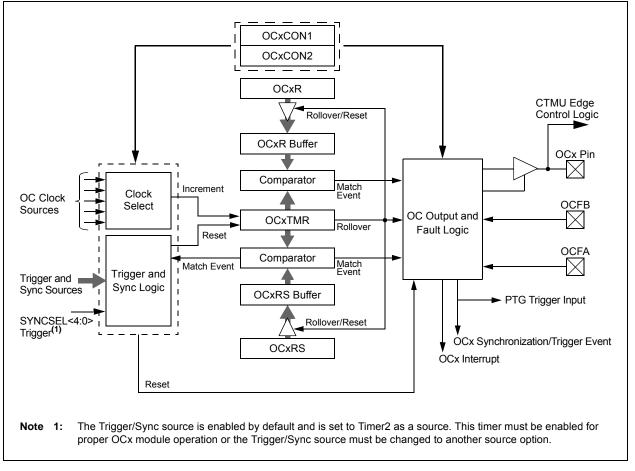
15.0 OUTPUT COMPARE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The output compare module can select one of seven available clock sources for its time base. The module compares the value of the timer with the value of one or two compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the compare register value. The output compare module generates either a single output pulse or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Note: See "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual" for OCxR and OCxRS register restrictions.





15.2 Output Compare Control Registers

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
	0-0	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0		ENFLTB
 bit 15		COOIDE		OUTOLLI	OUTOLLU		bit 8
Sit 10							bit 0
R/W-0	U-0	R/W-0, HSC	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0
ENFLT		OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0
bit 7							bit 0
Legend:		HSC = Hardw	are Settable/Cl	earable bit			
R = Read	able bit	W = Writable I	oit	U = Unimplem	nented bit, read	as '0'	
-n = Value	e at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own
bit 15-14	Unimplemen	ted: Read as 'o)'				
bit 13	OCSIDL: Out	tput Compare x	Stop in Idle Mo	de Control bit			
		ompare x Halts					
	•	compare x conti	•		ode		
bit 12-10)>: Output Com	pare x Clock S	elect bits			
	111 = Periph 110 = Reserv	eral clock (FP)					
	101 = PTGO						
		is the clock so			hronous clock	is supported)	
		is the clock so					
		(is the clock so (is the clock so					
		is the clock so					
bit 9	Unimplemen	ted: Read as '0)'				
bit 8	ENFLTB: Fau	ult B Input Enab	le bit				
		compare Fault B compare Fault B					
bit 7	-	ult A Input Enab					
	1 = Output C	ompare Fault A compare Fault A	input (OCFA)				
bit 6	•	ted: Read as '0	• • •				
bit 5	OCFLTB: PW	M Fault B Con	dition Status bit				
		ult B condition of Fault B condition					
bit 4		/M Fault A Cond	•				
		ult A condition o					
Note 1:	OCxR and OCxF	29 are double h	uffered in D\\//	/ mode only			
Note 1. 2:	Each Output Cor			-	irce. See Secti	on 24.0 "Perin	heral Trigger
2.	Generator (PTG					5.1 2 7.0 1 611p	
	PTGO4 = OC1	-					
	PTGO5 = OC2						
	PTGO6 = OC3 PTGO7 = OC4						

18.3 SPIx Control Registers

R/W-0 U-0 R/W-0 U-0 R/W-0 R/W-0 R/W-0 U-0 SPIEN SPISIDL SPIBEC<2:0> _____ bit 15 R/W-0 R/W-0 R/W-0 R/C-0, HS R/W-0 R/W-0 R-0, HS, HC R-0, HS, HC SRMPT SPIROV SRXMPT SISEL2 SISEL1 SISEL0 SPITBF SPIRBF bit 7 Legend: C = Clearable bit HS = Hardware Settable bit HC = Hardware Clearable bit R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 SPIEN: SPIx Enable bit 1 = Enables the module and configures SCKx, SDOx, SDIx and \overline{SSx} as serial port pins 0 = Disables the module bit 14 Unimplemented: Read as '0' bit 13 SPISIDL: SPIx Stop in Idle Mode bit 1 = Discontinues the module operation when device enters Idle mode 0 = Continues the module operation in Idle mode bit 12-11 Unimplemented: Read as '0' bit 10-8 SPIBEC<2:0>: SPIx Buffer Element Count bits (valid in Enhanced Buffer mode) Master mode: Number of SPIx transfers that are pending. Slave mode: Number of SPIx transfers that are unread. SRMPT: SPIx Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode) bit 7 1 = SPIx Shift register is empty and Ready-To-Send or receive the data 0 = SPIx Shift register is not empty bit 6 SPIROV: SPIx Receive Overflow Flag bit

REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER

1 = A new byte/word is completely received and discarded; the user application has not read the previous data in the SPIxBUF register 0 = No overflow has occurred SRXMPT: SPIx Receive FIFO Empty bit (valid in Enhanced Buffer mode)

- 1 = RX FIFO is empty
- 0 = RX FIFO is not empty

bit 4-2 SISEL<2:0>: SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)

- 111 = Interrupt when the SPIx transmit buffer is full (SPITBF bit is set)
 - 110 = Interrupt when last bit is shifted into SPIxSR and as a result, the TX FIFO is empty
 - 101 = Interrupt when the last bit is shifted out of SPIxSR and the transmit is complete
 - 100 = Interrupt when one data is shifted into the SPIxSR and as a result, the TX FIFO has one open memory location
 - 011 = Interrupt when the SPIx receive buffer is full (SPIRBF bit is set)
 - 010 = Interrupt when the SPIx receive buffer is 3/4 or more full
 - 001 = Interrupt when data is available in the receive buffer (SRMPT bit is set)
 - 000 = Interrupt when the last data in the receive buffer is read and as a result, the buffer is empty (SRXMPT bit is set)

bit 5

bit 8

bit 0

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 6	STREN: SCLx Clock Stretch Enable bit (when operating as I ² C slave) Used in conjunction with the SCLREL bit. 1 = Enables software or receives clock stretching 0 = Disables software or receives clock stretching
bit 5	ACKDT: Acknowledge Data bit (when operating as I ² C master, applicable during master receive)
	Value that is transmitted when the software initiates an Acknowledge sequence. 1 = Sends NACK during Acknowledge 0 = Sends ACK during Acknowledge
bit 4	ACKEN: Acknowledge Sequence Enable bit (when operating as I ² C master, applicable during master receive)
	 1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit. Hardware is clear at the end of the master Acknowledge sequence. 0 = Acknowledge sequence is not in progress
bit 3	RCEN: Receive Enable bit (when operating as I ² C master)
	 1 = Enables Receive mode for I²C. Hardware is clear at the end of the eighth bit of the master receive data byte. 0 = Receive sequence is not in progress
bit 2	PEN: Stop Condition Enable bit (when operating as I^2C master)
511 2	1 = Initiates Stop condition on SDAx and SCLx pins. Hardware is clear at the end of the master Stop sequence.
h :+ 4	0 = Stop condition is not in progress
bit 1	RSEN: Repeated Start Condition Enable bit (when operating as I ² C master)
	 1 = Initiates Repeated Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Repeated Start sequence. 0 = Repeated Start condition is not in progress
bit 0	SEN: Start Condition Enable bit (when operating as l^2C master)
	 1 = Initiates Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Start sequence. 0 = Start condition is not in progress

Note 1: When performing master operations, ensure that the IPMIEN bit is set to '0'.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 21-16: CxRXFnSID: ECANx ACCEPTANCE FILTER n STANDARD IDENTIFIER REGISTER (n = 0-15)

RW-x R/W-x R/W-x R/W-x R/W-x R/W-x R/W-x R/W-x SID10 SID9 SID8 SID7 SID6 SID5 SID4 SID3 bit 15 bit 15 bit 8 bit 8 bit 8 bit 8 bit 8 R/W-x R/W-x R/W-x U-0 R/W-x U-0 R/W-x R/W-x SID2 SID1 SID0 - EXIDE - EID17 EID16 bit 7 5ID2 SID1 SID0 - EXIDE - EID17 EID16 bit 7 - - EID17 EID16 bit 0 bit 0 Legend: R Readable bit W = Writable bit U = Unimplemented bit, read as '0' - <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th>								
bit 15 bit 2 bit 3 bit 8 bit 8 bit 8 bit 7 bit 7 bit 9 bit 7 bit 0 bit 0 bit 7 bit 0 bit 0 bit 7 bit 0 bit 0 bit 0 bit 1 bit 9 bit 1 bit 9 bit 1 bit 1 bit 9 bit 1	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
R/W-x R/W-x U-0 R/W-x U-0 R/W-x R/W-x SID2 SID1 SID0 - EXIDE - EID17 EID16 bit 7 bit 0 Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15-5 SID<10:>: Standard Identifier bits 1 = Message address bit, SIDx, must be '1' to match filter 0 = Message address bit, SIDx, must be '0' to match filter bit 4 Unimplemented: Read as '0' bit 3 EXIDE: Extended Identifier Enable bit If MIDE = 1: 1 = Matches only messages with Extended Identifier addresses 0 = Matches only messages with Standard Identifier addresses 0 = Matches only messages with Standard Identifier addresses Ignores EXIDE bit. Ignores EXIDE bit. bit 2 Unimplemented: Read as '0' Ignores Extended Identifier bits 1 = Message address bit, EIDx, must be '1' to match filter	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
SID2 SID1 SID0 — EXIDE — EID17 EID16 bit 7 bit 0	bit 15	÷						bit 8
SID2 SID1 SID0 — EXIDE — EID17 EID16 bit 7 bit 0								
bit 7 bit 0 Legend: W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15-5 SID<10:0>: Standard Identifier bits 1 = Message address bit, SIDx, must be '1' to match filter x = Bit is unknown bit 15-5 SID<10:0>: Standard Identifier bits 1 = Message address bit, SIDx, must be '1' to match filter x = Bit is unknown bit 4 Unimplemented: Read as '0' bit 3 EXIDE: Extended Identifier Enable bit If MIDE = 1: 1 = Matches only messages with Extended Identifier addresses 0 = Matches only messages with Standard Identifier addresses 0 = Matches only messages with Standard Identifier addresses If MIDE = 0: Ignores EXIDE bit. bit 2 Unimplemented: Read as '0' bit 1-0 EID<17:16>: Extended Identifier bits 1 = Message address bit, EIDx, must be '1' to match filter 1 = Message address bit, EIDx, must be '1' to match filter	R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15-5 SID<10:0>: Standard Identifier bits 1 = Message address bit, SIDx, must be '1' to match filter 0 = Message address bit, SIDx, must be '1' to match filter 0 = Message address bit, SIDx, must be '0' to match filter bit 4 Unimplemented: Read as '0' bit 3 EXIDE: Extended Identifier Enable bit If MIDE = 1: 1 = Matches only messages with Extended Identifier addresses 0 = Matches only messages with Standard Identifier addresses If MIDE = 0: Ignores EXIDE bit. bit 2 Unimplemented: Read as '0' bit 1-0 EID<17:16>: Extended Identifier bits 1 = Message address bit, EIDx, must be '1' to match filter	SID2	SID1	SID0	_	EXIDE		EID17	EID16
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15-5 SID<10:0>: Standard Identifier bits 1 = Message address bit, SIDx, must be '1' to match filter 0 = Message address bit, SIDx, must be '1' to match filter 0 = Message address bit, SIDx, must be '0' to match filter bit 4 Unimplemented: Read as '0' bit 3 EXIDE: Extended Identifier Enable bit If MIDE = 1: 1 = Matches only messages with Extended Identifier addresses 0 = Matches only messages with Standard Identifier addresses 0 = Matches only messages with Standard Identifier addresses 1f MIDE = 0: Ignores EXIDE bit. bit 2 Unimplemented: Read as '0' bit 1-0 EID a Matches bit, EIDx, must be '1' to match filter	bit 7							bit 0
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15-5 SID<10:0>: Standard Identifier bits 1 = Message address bit, SIDx, must be '1' to match filter 0 = Message address bit, SIDx, must be '1' to match filter 0 = Message address bit, SIDx, must be '0' to match filter bit 4 Unimplemented: Read as '0' bit 3 EXIDE: Extended Identifier Enable bit If MIDE = 1: 1 = Matches only messages with Extended Identifier addresses 0 = Message Sit, SIDE 5 bit 2 Unimplemented: Read as '0' bit 2 Unimplemented: Read as '0' bit 4 Unimplemented: Read as '0' bit 1-0 EID if MIDE = 0: Ignores EXIDE bit. bit 2 Unimplemented: Read as '0' bit 1-0 EID a Message address bit, EIDx, must be '1' to match filter								
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15-5 SID<10:0>: Standard Identifier bits 1 = Message address bit, SIDx, must be '1' to match filter o = Message address bit, SIDx, must be '1' to match filter 0' = Bit is cleared x = Bit is unknown bit 4 Unimplemented: Read as '0' bit 3 EXIDE: Extended Identifier Enable bit If MIDE = 1: 1 = Matches only messages with Extended Identifier addresses 0 = Matches only messages with Standard Identifier addresses If MIDE = 0: Ignores EXIDE bit. If MIDE = 0: Ignores EXIDE bit. bit 2 Unimplemented: Read as '0' EID<17:16>: Extended Identifier bits 1 = Message address bit, EIDx, must be '1' to match filter 1 = Message address bit, EIDx, must be '1' to match filter	Legend:							
bit 15-5 SID<10:0>: Standard Identifier bits 1 = Message address bit, SIDx, must be '1' to match filter 0 = Message address bit, SIDx, must be '0' to match filter bit 4 Unimplemented: Read as '0' bit 3 EXIDE: Extended Identifier Enable bit If MIDE = 1: 1 = Matches only messages with Extended Identifier addresses 0 = Matches only messages with Standard Identifier addresses 0 = Matches only messages with Standard Identifier addresses 1 f MIDE = 0: Ignores EXIDE bit. bit 2 Unimplemented: Read as '0' bit 1-0 EID<17:16>: Extended Identifier bits 1 = Message address bit, EIDx, must be '1' to match filter	R = Readable	e bit	W = Writable	bit	U = Unimpler	nented bit, read	d as '0'	
1 = Message address bit, SIDx, must be '1' to match filter 0 = Message address bit, SIDx, must be '0' to match filter bit 4 Unimplemented: Read as '0' bit 3 EXIDE: Extended Identifier Enable bit If MIDE = 1: 1 = Matches only messages with Extended Identifier addresses 0 = Matches only messages with Standard Identifier addresses 0 = Matches only messages with Standard Identifier addresses If MIDE = 0: Ignores EXIDE bit. bit 2 Unimplemented: Read as '0' bit 1-0 EID I= Message address bit, EIDx, must be '1' to match filter	-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
If MIDE = 1: 1 = Matches only messages with Extended Identifier addresses 0 = Matches only messages with Standard Identifier addresses If MIDE = 0: Ignores EXIDE bit. bit 2 Unimplemented: Read as '0' bit 1-0 EID<17:16>: Extended Identifier bits 1 = Message address bit, EIDx, must be '1' to match filter	bit 4	0 = Message	address bit, SI	Dx, must be '				
bit 1-0 EID<17:16>: Extended Identifier bits 1 = Message address bit, EIDx, must be '1' to match filter	bit 3	<u>If MIDE = 1:</u> 1 = Matches 0 = Matches <u>If MIDE = 0:</u>	only messages only messages	with Extende				
1 = Message address bit, EIDx, must be '1' to match filter	bit 2	Unimplemen	ted: Read as '	כ'				
	bit 1-0	EID<17:16>:	Extended Iden	tifier bits				
		•						

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 21-20:	CxRXMnSID: ECANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER
	REGISTER (n = 0-2)

		-	-						
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3		
bit 15							bit 8		
R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x		
SID2	SID1	SID0	-	MIDE	_	EID17	EID16		
bit 7							bit C		
<u> </u>									
Legend:									
R = Readab	ole bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'			
-n = Value a	at POR	'1' = Bit is set	:	'0' = Bit is cleared x = Bit is unknown					
bit 15-5	SID<10:0>: S	Standard Identi	fier bits						
		bit, SIDx, in filte is a don't care i							
bit 4	Unimplemer	nted: Read as '	0'						
bit 3	MIDE: Identif	fier Receive Mo	de bit						
	0 = Matches		or extended a	d or extended ac address messag SID/EID))		•			
bit 2	Unimplemer	nted: Read as '	0'						
bit 1-0	EID<17:16>:	Extended Iden	tifier bits						
		bit, EIDx, in fill is a don't care							

REGISTER 21-21: CxRXMnEID: ECANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8	
bit 15				·			bit 8	
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0	
bit 7						•	bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'				

R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 EID<15:0>: Extended Identifier bits

1 = Includes bit, EIDx, in filter comparison

0 = EIDx bit is a don't care in filter comparison

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8
R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0

REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

RXOVF4

bit 7			bit 0
Legend:	C = Writable bit, but or	nly '0' can be written to clear the bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	

RXOVF3

RXOVF2

R = Readable bit	vv = vvritable bit	U = Unimplemented bit, read	d as 0
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 RXOVF<15:0>: Receive Buffer n Overflow bits

RXOVF6

RXOVF7

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

RXOVF5

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but or	C = Writable bit, but only '0' can be written to clear the bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit	t, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15-0 RXOVF<31:16>: Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

RXOVF0

RXOVF1

22.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Charge Time Measurement Unit (CTMU)" (DS70661) in the "dsPIC33/PIC24 Family Reference Manual", which is available on the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Charge Time Measurement Unit is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. Its key features include:

- Four Edge Input Trigger Sources
- Polarity Control for Each Edge Source
- Control of Edge Sequence
- Control of Response to Edges
- · Precise Time Measurement Resolution of 1 ns
- Accurate Current Source Suitable for Capacitive Measurement
- On-Chip Temperature Measurement using a Built-in Diode

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock.

The CTMU module is ideal for interfacing with capacitive-based sensors. The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 and CTMUCON2 enable the module and control edge source selection, edge source polarity selection and edge sequencing. The CTMUICON register controls the selection and trim of the current source.

REGISTER 25-5:	CMxMSKCON: COMPARATOR x MASK GATING
	CONTROL REGISTER

R/W-0							
	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15							bit
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7							bit
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle		x = Bit is unk	nown
			-				
bit 15	HLMS: High	or Low-Level N	/lasking Select	bits			
	•		•		erted ('0') compa	rator signal from	m propagatin
					erted ('1') compa		
bit 14	Unimplemen	ted: Read as	ʻ0'				
bit 13	OCEN: OR G	Sate C Input Er	nable bit				
	1 = MCI is co	nnected to OR	t gate				
	0 = MCI is no	ot connected to	OR gate				
bit 12		Gate C Input I					
		MCI is connect					
		MCI is not con	-	jate			
bit 11	OBEN: OR Gate B Input Enable bit						
		nnected to OR	gate				
bit 10	0 = MBI is no	t connected to	gate OR gate	e hit			
bit 10	0 = MBI is no OBNEN: OR	t connected to Gate B Input I	gate OR gate nverted Enable				
bit 10	0 = MBI is no OBNEN: OR 1 = Inverted I	t connected to	gate OR gate nverted Enable ed to OR gate				
bit 10 bit 9	0 = MBI is no OBNEN: OR 1 = Inverted I 0 = Inverted I	t connected to Gate B Input I MBI is connect	gate OR gate nverted Enable ed to OR gate nected to OR g				
	0 = MBI is no OBNEN: OR 1 = Inverted I 0 = Inverted I OAEN: OR G 1 = MAI is co	t connected to Gate B Input I MBI is connect MBI is not conr Gate A Input Er nnected to OR	gate OR gate nverted Enable ed to OR gate nected to OR g nable bit gate				
	0 = MBI is no OBNEN: OR 1 = Inverted I 0 = Inverted I OAEN: OR G 1 = MAI is co 0 = MAI is no	t connected to Gate B Input I MBI is connect MBI is not conn Gate A Input Er nnected to OR t connected to	gate OR gate nverted Enable ed to OR gate nected to OR g nable bit gate OR gate	jate			
	0 = MBI is no OBNEN: OR 1 = Inverted I 0 = Inverted I OAEN: OR G 1 = MAI is no OANEN: OR	t connected to Gate B Input I MBI is connect MBI is not conn Gate A Input Er nnected to OR t connected to Gate A Input I	gate OR gate nverted Enable ed to OR gate nected to OR g nable bit gate OR gate nverted Enable	jate e bit			
bit 9	0 = MBI is no OBNEN: OR 1 = Inverted I 0 = Inverted I OAEN: OR G 1 = MAI is no OANEN: OR 1 = Inverted I	t connected to Gate B Input I MBI is connect MBI is not com Gate A Input Er nnected to OR t connected to Gate A Input I MAI is connect	gate OR gate nverted Enable ed to OR gate nected to OR g nable bit gate OR gate nverted Enable ed to OR gate	jate e bit			
bit 9 bit 8	0 = MBI is no OBNEN: OR 1 = Inverted I 0 = Inverted I OAEN: OR G 1 = MAI is no OANEN: OR 1 = Inverted I 0 = Inverted I	t connected to Gate B Input I MBI is connect MBI is not com Gate A Input Er nnected to OR t connected to Gate A Input I MAI is connect MAI is not com	gate OR gate nverted Enable ed to OR gate nected to OR gate bit gate OR gate nverted Enable ed to OR gate	gate e bit gate			
bit 9	0 = MBI is no OBNEN: OR 1 = Inverted I 0 = Inverted I OAEN: OR G 1 = MAI is no OANEN: OR 1 = Inverted I 0 = Inverted I NAGS: AND	t connected to Gate B Input I MBI is connect MBI is not com Gate A Input Er nnected to OR t connected to Gate A Input I MAI is connect MAI is not com Gate Output Ir	gate OR gate nverted Enable ed to OR gate nected to OR gate bit gate OR gate nverted Enable nected to OR gate nected to OR gate	gate e bit gate e bit			
bit 9 bit 8	0 = MBI is no OBNEN: OR 1 = Inverted I 0 = Inverted I OAEN: OR G 1 = MAI is co 0 = MAI is no OANEN: OR 1 = Inverted I 0 = Inverted I NAGS: AND 1 = Inverted I	t connected to Gate B Input I MBI is connect MBI is not com Gate A Input Er nnected to OR t connected to Gate A Input I MAI is connect MAI is not connect Gate Output Ir ANDI is connect	gate OR gate nverted Enable ed to OR gate nected to OR gate oR gate OR gate nverted Enable nected to OR gate nected to OR gate	gate e bit gate e bit e			
bit 9 bit 8	0 = MBI is no OBNEN: OR 1 = Inverted I 0 = Inverted I OAEN: OR G 1 = MAI is no 0 = MAI is no OANEN: OR 1 = Inverted I 0 = Inverted I 0 = Inverted I 0 = Inverted I	t connected to Gate B Input I MBI is connect MBI is not conn Gate A Input Er nnected to OR t connected to Gate A Input I MAI is connect MAI is not connect ANDI is not connect ANDI is not connect	gate OR gate nverted Enable ed to OR gate nected to OR g able bit gate OR gate Nverted Enable nverted Enable nverted Enable cted to OR gate	gate e bit gate e bit e			
bit 9 bit 8 bit 7	0 = MBI is no OBNEN: OR 1 = Inverted I 0 = Inverted I OAEN: OR G 1 = MAI is no OANEN: OR 1 = Inverted I 0 = Inverted I NAGS: AND 1 = Inverted I PAGS: AND 1 = ANDI is no	t connected to Gate B Input I MBI is connect MBI is not conn Gate A Input Er nnected to OR t connected to Gate A Input I MAI is connect MAI is not connect ANDI is not connect Gate Output Ir ANDI is not connect Gate Output E connected to O	gate OR gate nverted Enable ed to OR gate nected to OR g able bit gate OR gate nverted Enable ed to OR gate nected to OR gat nected to OR gat	gate e bit gate e bit e			
bit 9 bit 8 bit 7	0 = MBI is no OBNEN: OR 1 = Inverted I 0 = Inverted I OAEN: OR 1 = MAI is co 0 = MAI is no OANEN: OR 1 = Inverted I 0 = Inverted I NAGS: AND 1 = Inverted I 0 = Inverted I	t connected to Gate B Input I MBI is connect MBI is not com Gate A Input Er nnected to OR t connected to Gate A Input I MAI is connect MAI is not com Gate Output Ir ANDI is not con Gate Output E connected to O tot connected t	gate OR gate nverted Enable ed to OR gate nected to OR gate oR gate OR gate nverted Enable ed to OR gate nected to OR gate	gate e bit gate e bit e			
bit 9 bit 8 bit 7	0 = MBI is no OBNEN: OR 1 = Inverted I 0 = Inverted I OAEN: OR 1 = MAI is co 0 = MAI is no OANEN: OR 1 = Inverted I NAGS: AND 1 = Inverted I NAGS: AND 1 = Inverted I PAGS: AND 1 = ANDI is co 0 = ANDI is no	t connected to Gate B Input I MBI is connect MBI is not com Gate A Input Er nnected to OR t connected to Gate A Input I MAI is connect MAI is not connected ANDI is not connected ANDI is not connected to Gate Output E connected to O tot connected to Gate C Input E	gate OR gate nverted Enable ed to OR gate nected to OR gate oR gate OR gate nverted Enable ed to OR gate nected bit R gate to OR gate nable bit	gate e bit gate e bit e			
bit 9 bit 8 bit 7 bit 6	0 = MBI is no OBNEN: OR 1 = Inverted I 0 = Inverted I OAEN: OR G 1 = MAI is co 0 = MAI is no OANEN: OR 1 = Inverted I 0 = Inverted I NAGS: AND 1 = Inverted I 0 = Inverted I PAGS: AND 1 = ANDI is co 0 = ANDI is co 1 = MCI is co	t connected to Gate B Input I MBI is connect MBI is not com Gate A Input Er nnected to OR t connected to Gate A Input I MAI is connect MAI is not com Gate Output Ir ANDI is connect ANDI is not con Gate Output E connected to O tot connected to Gate C Input E	a gate OR gate Nverted Enable ed to OR gate nected to OR gate OR gate OR gate Nverted Enable ed to OR gate nected to OR gate nected to OR gate the de to OR gate the for OR gate cable bit R gate to OR gate Enable bit D gate	gate e bit gate e bit e			
bit 9 bit 8 bit 7 bit 6 bit 5	0 = MBI is no OBNEN: OR 1 = Inverted I 0 = Inverted I OAEN: OR G 1 = MAI is co 0 = MAI is no OANEN: OR 1 = Inverted I 0 = Inverted I NAGS: AND 1 = Inverted I PAGS: AND 1 = ANDI is co 0 = ANDI is no 0 = MCI is no 0 = MCI is no	t connected to Gate B Input I MBI is connect MBI is not conn Gate A Input Er nnected to OR t connected to Gate A Input I MAI is connect MAI is not connect ANDI is not connected to Gate Output E connected to O tot connected to Gate C Input E mnected to AN of connected to	gate OR gate nverted Enable ed to OR gate nected to OR gate oR gate OR gate nverted Enable ed to OR gate nected to OR gate nected to OR gate the dto OR gate nected to OR gate chable bit R gate to OR gate nable bit R gate to OR gate anable bit D gate AND gate	gate e bit gate e gate			
bit 9 bit 8 bit 7 bit 6	0 = MBI is no OBNEN: OR 1 = Inverted I 0 = Inverted I OAEN: OR G 1 = MAI is co 0 = MAI is no OANEN: OR 1 = Inverted I 0 = Inverted I NAGS: AND 1 = Inverted I PAGS: AND 1 = ANDI is co 0 = ANDI is no ACEN: AND 1 = MCI is co 0 = MCI is no ACNEN: AND	t connected to Gate B Input I MBI is connect MBI is not com Gate A Input Er nnected to OR t connected to Gate A Input I MAI is connect MAI is not com Gate Output Ir ANDI is connect ANDI is not con Gate Output E connected to O tot connected to Gate C Input E	gate OR gate nverted Enable ed to OR gate nected to OR gate oR gate OR gate nverted Enable ed to OR gate nected to OR gate nected to OR gate the dto OR gate nected to OR gate co OR gate nable bit R gate o OR gate anable bit D gate AND gate	gate e bit gate e bit gate			

DC CH	ARACTE	RISTICS	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic	Min.	Units	Conditions		
	liL	Input Leakage Current ^(1,2)					
DI50		I/O Pins 5V Tolerant ⁽³⁾	-1	—	+1	μA	$\label{eq:VSS} \begin{split} &V{\sf SS} \leq V{\sf PIN} \leq V{\sf DD}, \\ &P{\sf in at high-impedance} \end{split}$
DI51		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	$\label{eq:VSS} \begin{array}{l} VSS \leq VPIN \leq VDD, \\ Pin \text{ at high-impedance}, \\ -40^\circC \leq TA \leq +85^\circC \end{array}$
DI51a		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	Analog pins shared with external reference pins, $-40^{\circ}C \le TA \le +85^{\circ}C$
DI51b		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	$Vss \le VPIN \le VDD,$ Pin at high-impedance, -40°C ≤ TA ≤ +125°C
DI51c		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	Analog pins shared with external reference pins, $-40^{\circ}C \le TA \le +125^{\circ}C$
DI55		MCLR	-5	—	+5	μA	$Vss \leq V \text{PIN} \leq V \text{DD}$
DI56		OSC1	-5	—	+5	μΑ	$\label{eq:VSS} \begin{array}{l} VSS \leq VPIN \leq VDD, \\ XT \text{ and } HS \text{ modes} \end{array}$

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 2: Negative current is defined as current sourced by the pin.
- 3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 4: VIL source < (Vss 0.3). Characterized but not tested.
- **5:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.
- 6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

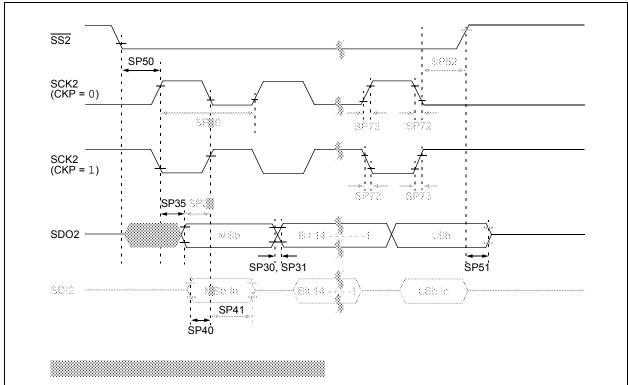


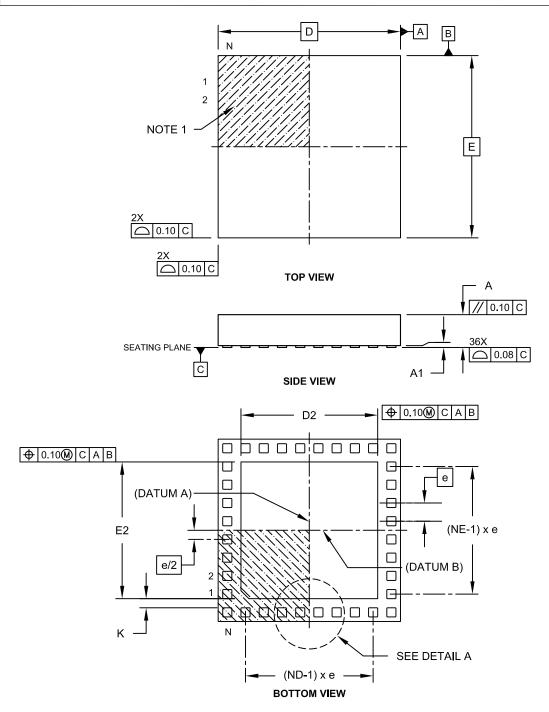
FIGURE 30-21: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



FIGURE 30-29: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-187C Sheet 1 of 2

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