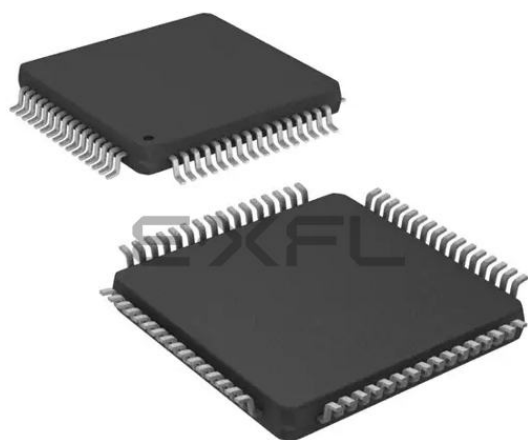




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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gp506-e-pt

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name ⁽⁴⁾	Pin Type	Buffer Type	PPS	Description
AN0-AN15	I	Analog	No	Analog input channels.
CLKI	I	ST/ CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/ CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
REFCLKO	O	—	Yes	Reference clock output.
IC1-IC4	I	ST	Yes	Capture Inputs 1 through 4.
OCFA	I	ST	Yes	Compare Fault A input (for Compare channels).
OCFB	I	ST	No	Compare Fault B input (for Compare channels).
OC1-OC4	O	—	Yes	Compare Outputs 1 through 4.
INT0	I	ST	No	External Interrupt 0.
INT1	I	ST	Yes	External Interrupt 1.
INT2	I	ST	Yes	External Interrupt 2.
RA0-RA4, RA7-RA12	I/O	ST	No	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port.
RC0-RC13, RC15	I/O	ST	No	PORTC is a bidirectional I/O port.
RD5, RD6, RD8	I/O	ST	No	PORTD is a bidirectional I/O port.
RE12-RE15	I/O	ST	No	PORT E is a bidirectional I/O port.
RF0, RF1	I/O	ST	No	PORTF is a bidirectional I/O port.
RG6-RG9	I/O	ST	No	PORTG is a bidirectional I/O port.
T1CK	I	ST	No	Timer1 external clock input.
T2CK	I	ST	Yes	Timer2 external clock input.
T3CK	I	ST	No	Timer3 external clock input.
T4CK	I	ST	No	Timer4 external clock input.
T5CK	I	ST	No	Timer5 external clock input.
CTPLS	O	ST	No	CTMU pulse output.
CTED1	I	ST	No	CTMU External Edge Input 1.
CTED2	I	ST	No	CTMU External Edge Input 2.
U1CTS	I	ST	No	UART1 Clear-To-Send.
U1RTS	O	—	No	UART1 Ready-To-Send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
BCLK1	O	ST	No	UART1 IrDA [®] baud clock output.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
PPS = Peripheral Pin Select TTL = TTL input buffer

- Note 1:** This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- 2:** This pin is available on dsPIC33EPXXXGP/MC50X devices only.
- 3:** This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 “High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”** for more information.
- 4:** Not all pins are available in all packages variants. See the **“Pin Diagrams”** section for pin availability.
- 5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

3.5 Programmer's Model

The programmer's model for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X is shown in Figure 3-2. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/

MC20X devices contain control registers for Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only), Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only) and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory mapped, as shown in Table 4-1.

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Register(s) Name	Description
W0 through W15	Working Register Array
ACCA, ACBB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
DSRPAG	Extended Data Space (EDS) Read Page Register
DSWPAG	Extended Data Space (EDS) Write Page Register
RCOUNT	REPEAT Loop Count Register
DCOUNT ⁽¹⁾	D0 Loop Count Register
DOSTARTH ^(1,2) , DOSTARTL ^(1,2)	D0 Loop Start Address Register (High and Low)
DOENDH ⁽¹⁾ , DOENDL ⁽¹⁾	D0 Loop End Address Register (High and Low)
CORCON	Contains DSP Engine, D0 Loop Control and Trap Status bits

Note 1: This register is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

2: The DOSTARTH and DOSTARTL registers are read-only.

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	DMA3IF	—	—	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	QE11IF	PSEMIF	—	—	—	—	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	CTMUIF	—	—	—	—	—	—	—	—	—	CRCIF	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	DMA3IE	—	—	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	QE11IE	PSEMIE	—	—	—	—	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	—	—	—	—	—	CRCIE	U2EIE	U1EIE	0000
IEC5	082A	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IE	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTIEIE	—	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	—	—	—	—	—	—	—	—	SPI2IP<2:0>			—	SPI2EIP<2:0>			0044
IPC9	0852	—	—	—	—	—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			0444
IPC12	0858	—	—	—	—	—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	—	—	—	0440
IPC14	085C	—	—	—	—	—	QE11IP<2:0>			—	PSEMIP<2:0>			—	—	—	—	0440
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP<2:0>			—	—	—	—	0040
IPC23	086E	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC24	0870	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IP<2:0>			4004

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY (CONTINUED)

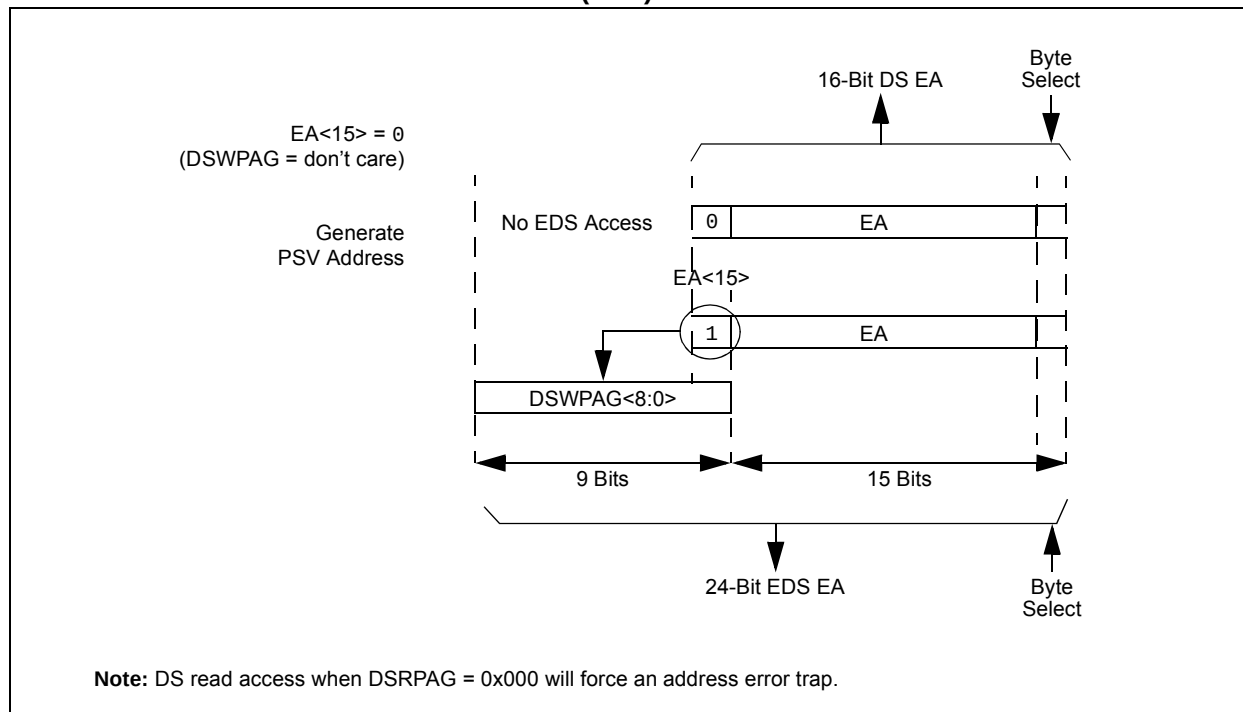
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC35	0886	—	JTAGIP<2:0>			—	ICDIP<2:0>			—	—	—	—	—	—	—	—	4400
IPC36	0888	—	PTG0IP<2:0>			—	PTGWDIP<2:0>			—	PTGSTEIP<2:0>			—	—	—	—	4440
IPC37	088A	—	—	—	—	—	PTG3IP<2:0>			—	PTG2IP<2:0>			—	PTG1IP<2:0>			0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	—	—	—	—	—	—	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	—	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	ILR<3:0>			VECNUM<7:0>									0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-16: QE1 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
QE1CON	01C0	QE1EN	—	QE1SIDL	PIMOD<2:0>			IMV<1:0>		—	INTDIV<2:0>			CNTPOL	GATEN	CCM<1:0>		0000
QE1IOC	01C2	QCAPEN	FLTREN	QFDIV<2:0>			OUTFNC<1:0>		SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	000x
QE1STAT	01C4	—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN	PCIIRQ	PCIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
POS1CNTL	01C6	POSCNT<15:0>																0000
POS1CNTH	01C8	POSCNT<31:16>																0000
POS1HLD	01CA	POSHLD<15:0>																0000
VEL1CNT	01CC	VELCNT<15:0>																0000
INT1TMRL	01CE	INTTMR<15:0>																0000
INT1TMRH	01D0	INTTMR<31:16>																0000
INT1HLDL	01D2	INTHLD<15:0>																0000
INT1HLDH	01D4	INTHLD<31:16>																0000
INDX1CNTL	01D6	INDXCNT<15:0>																0000
INDX1CNTH	01D8	INDXCNT<31:16>																0000
INDX1HLD	01DA	INDXHLD<15:0>																0000
QE1GECL	01DC	QEIGEC<15:0>																0000
QE1ICL	01DC	QEIIC<15:0>																0000
QE1GECH	01DE	QEIGEC<31:16>																0000
QE1ICH	01DE	QEIIC<31:16>																0000
QE1LECL	01E0	QEILEC<15:0>																0000
QE1LECH	01E2	QEILEC<31:16>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

EXAMPLE 4-2: EXTENDED DATA SPACE (EDS) WRITE ADDRESS GENERATION

The paged memory scheme provides access to multiple 32-Kbyte windows in the EDS and PSV memory. The Data Space Page registers, DSxPAG, in combination with the upper half of the Data Space address, can provide up to 16 Mbytes of additional address space in the EDS and 8 Mbytes (DSRPAG only) of PSV address space. The paged data memory space is shown in Example 4-3.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG. Writes to PS are not supported, so DSWPAG is dedicated to DS, including EDS only. The Data Space and EDS can be read from, and written to, using DSRPAG and DSWPAG, respectively.

REGISTER 8-11: DMAPWC: DMA PERIPHERAL WRITE COLLISION STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	PWCOL3	PWCOL2	PWCOL1	PWCOL0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'bit 3 **PWCOL3:** DMA Channel 3 Peripheral Write Collision Flag bit

1 = Write collision is detected

0 = No write collision is detected

bit 2 **PWCOL2:** DMA Channel 2 Peripheral Write Collision Flag bit

1 = Write collision is detected

0 = No write collision is detected

bit 1 **PWCOL1:** DMA Channel 1 Peripheral Write Collision Flag bit

1 = Write collision is detected

0 = No write collision is detected

bit 0 **PWCOL0:** DMA Channel 0 Peripheral Write Collision Flag bit

1 = Write collision is detected

0 = No write collision is detected

10.2.1 SLEEP MODE

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into Standby when Sleep mode is entered by clearing the VREGS (RCON<8>) and VREGSF (RCON<11>) bits (default configuration).

If the application requires a faster wake-up time, and can accept higher current requirements, the VREGS (RCON<8>) and VREGSF (RCON<11>) bits can be set to keep the internal regulator and the Flash regulator active during Sleep mode.

10.2.2 IDLE MODE

The following occurs in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.4 “Peripheral Module Disable”**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction or the first instruction in the Interrupt Service Routine (ISR).

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral; for example, the TSIDL bit in the Timer1 Control register (T1CON<13>).

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>**: Trigger/Synchronization Source Selection bits

11111 = OCxRS compare event is used for synchronization
 11110 = INT2 pin synchronizes or triggers OCx
 11101 = INT1 pin synchronizes or triggers OCx
 11100 = CTMU module synchronizes or triggers OCx
 11011 = ADC1 module synchronizes or triggers OCx
 11010 = CMP3 module synchronizes or triggers OCx
 11001 = CMP2 module synchronizes or triggers OCx
 11000 = CMP1 module synchronizes or triggers OCx
 10111 = Reserved
 10110 = Reserved
 10101 = Reserved
 10100 = Reserved
 10011 = IC4 input capture event synchronizes or triggers OCx
 10010 = IC3 input capture event synchronizes or triggers OCx
 10001 = IC2 input capture event synchronizes or triggers OCx
 10000 = IC1 input capture event synchronizes or triggers OCx
 01111 = Timer5 synchronizes or triggers OCx
 01110 = Timer4 synchronizes or triggers OCx
 01101 = Timer3 synchronizes or triggers OCx
 01100 = Timer2 synchronizes or triggers OCx **(default)**
 01011 = Timer1 synchronizes or triggers OCx
 01010 = PTGOx synchronizes or triggers OCx⁽³⁾
 01001 = Reserved
 01000 = Reserved
 00111 = Reserved
 00110 = Reserved
 00101 = Reserved
 00100 = OC4 module synchronizes or triggers OCx^(1,2)
 00011 = OC3 module synchronizes or triggers OCx^(1,2)
 00010 = OC2 module synchronizes or triggers OCx^(1,2)
 00001 = OC1 module synchronizes or triggers OCx^(1,2)
 00000 = No Sync or Trigger source for OCx

Note 1: Do not use the OCx module as its own Synchronization or Trigger source.

2: When the OCy module is turned OFF, it sends a trigger out signal. If the OCx module uses the OCy module as a Trigger source, the OCy module must be unselected as a Trigger source prior to disabling it.

3: Each Output Compare x module (OCx) has one PTG Trigger/Synchronization source. See **Section 24.0 “Peripheral Trigger Generator (PTG) Module”** for more information.

PTGO0 = OC1

PTGO1 = OC2

PTGO2 = OC3

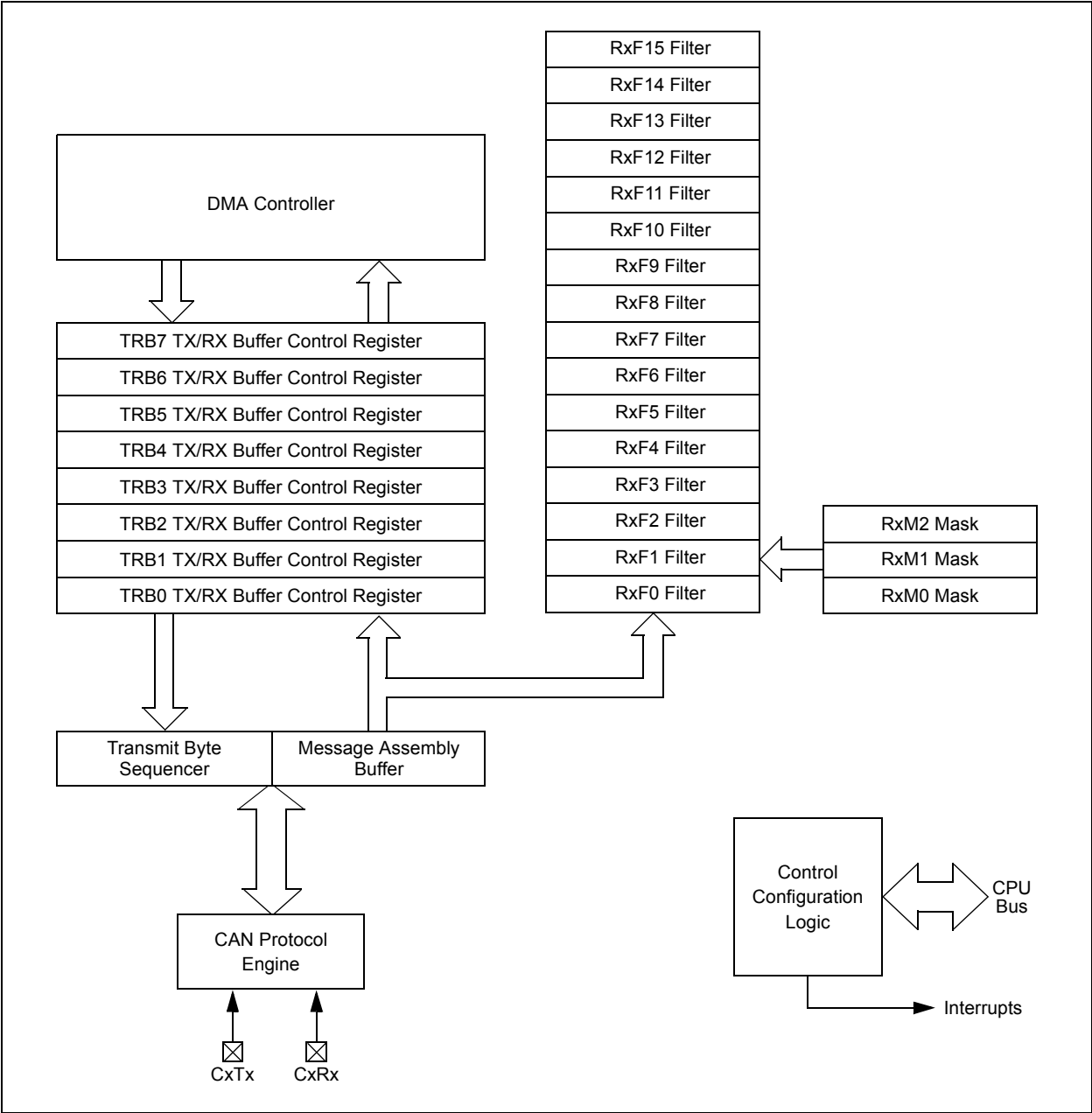
PTGO3 = OC4

REGISTER 16-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER⁽¹⁾

- bit 7-3 **FLTSRC<4:0>**: Fault Control Signal Source Select for PWM Generator # bits
- 11111 = Fault 32 (**default**)
 - 11110 = Reserved
 - .
 - .
 - .
 - 01100 = Reserved
 - 01011 = Comparator 4
 - 01010 = Op Amp/Comparator 3
 - 01001 = Op Amp/Comparator 2
 - 01000 = Op Amp/Comparator 1
 - 00111 = Reserved
 - 00110 = Reserved
 - 00101 = Reserved
 - 00100 = Reserved
 - 00011 = Fault 4
 - 00010 = Fault 3
 - 00001 = Fault 2
 - 00000 = Fault 1
- bit 2 **FLTPOL**: Fault Polarity for PWM Generator # bit⁽²⁾
- 1 = The selected Fault source is active-low
 - 0 = The selected Fault source is active-high
- bit 1-0 **FLTMOD<1:0>**: Fault Mode for PWM Generator # bits
- 11 = Fault input is disabled
 - 10 = Reserved
 - 01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (cycle)
 - 00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (latched condition)

- Note 1:** If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.
- 2:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

FIGURE 21-1: ECAN™ MODULE BLOCK DIAGRAM



REGISTER 21-7: CxINTE: ECANx INTERRUPT ENABLE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8	Unimplemented: Read as '0'
bit 7	IVRIE: Invalid Message Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 6	WAKIE: Bus Wake-up Activity Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 5	ERRIE: Error Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 4	Unimplemented: Read as '0'
bit 3	FIFOIE: FIFO Almost Full Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 2	RBOVIE: RX Buffer Overflow Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 1	RBIE: RX Buffer Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled
bit 0	TBIE: TX Buffer Interrupt Enable bit 1 = Interrupt request is enabled 0 = Interrupt request is not enabled

REGISTER 21-17: CxRXFnEID: ECANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **EID<15:0>**: Extended Identifier bits
1 = Message address bit, EIDx, must be '1' to match filter
0 = Message address bit, EIDx, must be '0' to match filter

REGISTER 21-18: CxFMSKSEL1: ECANx FILTER 7-0 MASK SELECTION REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7MSK<1:0>		F6MSK<1:0>		F5MSK<1:0>		F4MSK<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3MSK<1:0>		F2MSK<1:0>		F1MSK<1:0>		F0MSK<1:0>	
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **F7MSK<1:0>**: Mask Source for Filter 7 bits
11 = Reserved
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F6MSK<1:0>**: Mask Source for Filter 6 bits (same values as bits<15:14>)

bit 11-10 **F5MSK<1:0>**: Mask Source for Filter 5 bits (same values as bits<15:14>)

bit 9-8 **F4MSK<1:0>**: Mask Source for Filter 4 bits (same values as bits<15:14>)

bit 7-6 **F3MSK<1:0>**: Mask Source for Filter 3 bits (same values as bits<15:14>)

bit 5-4 **F2MSK<1:0>**: Mask Source for Filter 2 bits (same values as bits<15:14>)

bit 3-2 **F1MSK<1:0>**: Mask Source for Filter 1 bits (same values as bits<15:14>)

bit 1-0 **F0MSK<1:0>**: Mask Source for Filter 0 bits (same values as bits<15:14>)

NOTES:

24.2 PTG Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464
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24.2.1 KEY RESOURCES

- **“Peripheral Trigger Generator”** (DS70669) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions $\in \{W4 * W4, W5 * W5, W6 * W6, W7 * W7\}$
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions $\in \{W4 * W5, W4 * W6, W4 * W7, W5 * W6, W5 * W7, W6 * W7\}$
Wn	One of 16 working registers $\in \{W0...W15\}$
Wnd	One of 16 destination working registers $\in \{W0...W15\}$
Wns	One of 16 source working registers $\in \{W0...W15\}$
WREG	W0 (working register used in file register instructions)
Ws	Source W register $\in \{Ws, [Ws], [Ws++] , [Ws--], [++Ws], [--Ws] \}$
Wso	Source W register $\in \{Wns, [Wns], [Wns++] , [Wns--], [++Wns], [--Wns], [Wns+Wb] \}$
Wx	X Data Space Prefetch Address register for DSP instructions $\in \{[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], \text{none}\}$
Wxd	X Data Space Prefetch Destination register for DSP instructions $\in \{W4...W7\}$
Wy	Y Data Space Prefetch Address register for DSP instructions $\in \{[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], \text{none}\}$
Wyd	Y Data Space Prefetch Destination register for DSP instructions $\in \{W4...W7\}$

29.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

29.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

29.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

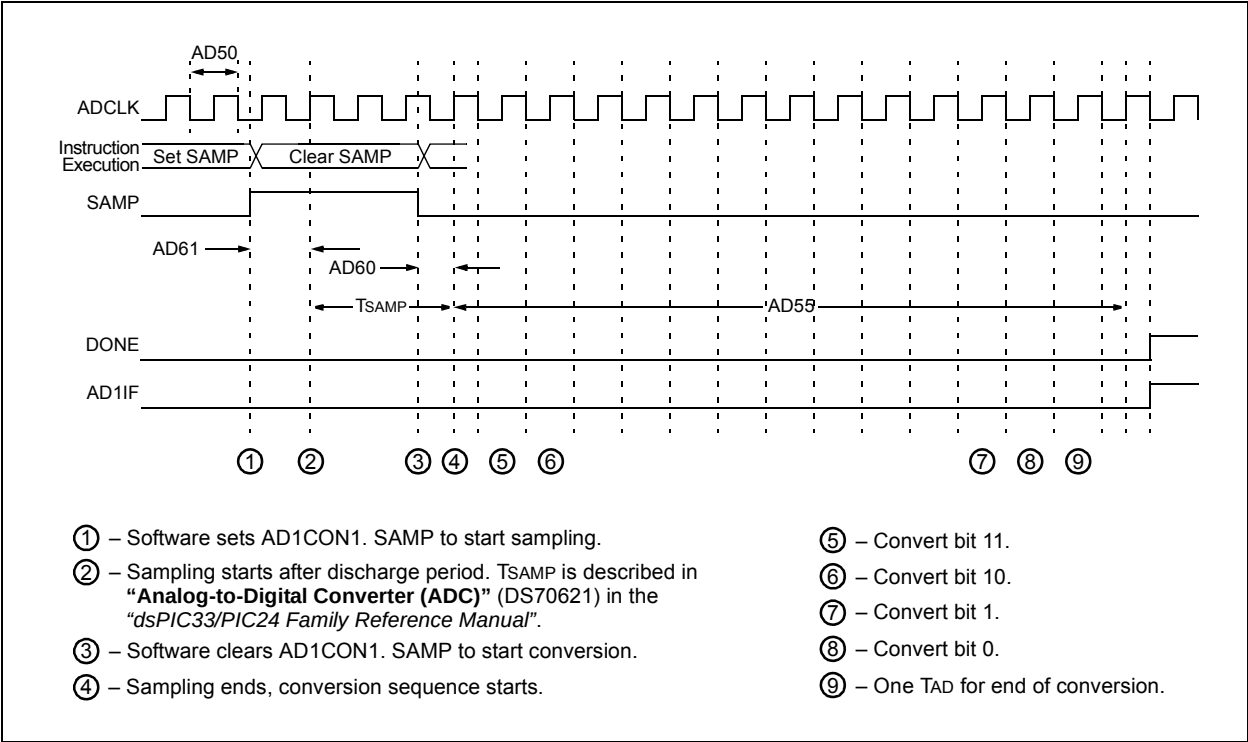
- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

29.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

FIGURE 30-36: ADC CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS
(ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)



31.0 HIGH-TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between -40°C to +150°C are identical to those shown in **Section 30.0 “Electrical Characteristics”** for operation between -40°C to +125°C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter DC10 in **Section 30.0 “Electrical Characteristics”** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X high-temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias ⁽²⁾	-40°C to +150°C
Storage temperature	-65°C to +160°C
Voltage on VDD with respect to VSS	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to VSS ⁽³⁾	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD < 3.0V ⁽³⁾	-0.3V to 3.6V
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 3.0V ⁽³⁾	-0.3V to 5.5V
Maximum current out of VSS pin	60 mA
Maximum current into VDD pin ⁽⁴⁾	60 mA
Maximum junction temperature	+155°C
Maximum current sourced/sunk by any 4x I/O pin	10 mA
Maximum current sourced/sunk by any 8x I/O pin	15 mA
Maximum current sunk by all ports combined	70 mA
Maximum current sourced by all ports combined ⁽⁴⁾	70 mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.

2: AEC-Q100 reliability testing for devices intended to operate at +150°C is 1,000 hours. Any design in which the total operating time from +125°C to +150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

3: Refer to the “Pin Diagrams” section for 5V tolerant pins.

4: Maximum allowable current is a function of device maximum power dissipation (see Table 31-2).

PMD (PIC24EPXXXMC20X Devices).....	94	CMxMSKCON (Comparator x Mask Gating Control).....	368
PORTA (PIC24EPXXXGP/MC202, dsPIC33EPXXXGP/MC202/502 Devices)	104	CMxMSKSR (Comparator x Mask Source Select Control).....	366
PORTA (PIC24EPXXXGP/MC203, dsPIC33EPXXXGP/MC203/503 Devices)	103	CORCON (Core Control).....	42, 133
PORTA (PIC24EPXXXGP/MC204, dsPIC33EPXXXGP/MC204/504 Devices)	102	CRCCON1 (CRC Control 1).....	375
PORTA (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	99	CRCCON2 (CRC Control 2).....	376
PORTB (PIC24EPXXXGP/MC202, dsPIC33EPXXXGP/MC202/502 Devices)	104	CRCXORH (CRC XOR Polynomial High)	377
PORTB (PIC24EPXXXGP/MC203, dsPIC33EPXXXGP/MC203/503 Devices)	103	CRCXORL (CRC XOR Polynomial Low).....	377
PORTB (PIC24EPXXXGP/MC204, dsPIC33EPXXXGP/MC204/504 Devices)	102	CTMUCON1 (CTMU Control 1).....	317
PORTB (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	99	CTMUCON2 (CTMU Control 2).....	318
PORTC (PIC24EPXXXGP/MC203, dsPIC33EPXXXGP/MC203/503 Devices)	103	CTMUICON (CTMU Current Control).....	319
PORTC (PIC24EPXXXGP/MC204, dsPIC33EPXXXGP/MC204/504 Devices)	102	CVRCON (Comparator Voltage Reference Control).....	371
PORTC (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	99	CxBUFPNT1 (ECANx Filter 0-3 Buffer Pointer 1)	300
PORTD (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	100	CxBUFPNT2 (ECANx Filter 4-7 Buffer Pointer 2)	301
PORTE (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	100	CxBUFPNT3 (ECANx Filter 8-11 Buffer Pointer 3)	301
PORTF (PIC24EPXXXGP/MC206, dsPIC33EPXXXGP/MC206/506 Devices)	100	CxBUFPNT4 (ECANx Filter 12-15 Buffer Pointer 4)	302
PORTG (PIC24EPXXXGP/MC206 and dsPIC33EPXXXGP/MC206/506 Devices)	101	CxCFG1 (ECANx Baud Rate Configuration 1).....	298
PTG.....	78	CxCFG2 (ECANx Baud Rate Configuration 2).....	299
PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices).....	79	CxCTRL1 (ECANx Control 1).....	290
PWM Generator 1 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices).....	79	CxCTRL2 (ECANx Control 2).....	291
PWM Generator 2 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices).....	80	CxEC (ECANx Transmit/Receive Error Count)	298
PWM Generator 3 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices).....	80	CxFCTRL (ECANx FIFO Control).....	293
QE11 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices).....	81	CxFEN1 (ECANx Acceptance Filter Enable 1).....	300
Reference Clock	93	CxFIFO (ECANx FIFO Status)	294
SPI1 and SPI2	83	CxFMSKSEL1 (ECANx Filter 7-0 Mask Selection 1).....	304
System Control	93	CxFMSKSEL2 (ECANx Filter 15-8 Mask Selection 2).....	305
Time1 through Time5.....	75	CxINTE (ECANx Interrupt Enable)	297
UART1 and UART2	82	CxINTF (ECANx Interrupt Flag).....	295
Registers		CxRXFnEID (ECANx Acceptance Filter n Extended Identifier)	304
AD1CHS0 (ADC1 Input Channel 0 Select)	333	CxRXFnSID (ECANx Acceptance Filter n Standard Identifier)	303
AD1CHS123 (ADC1 Input Channel 1, 2, 3 Select)	331	CxRXFUL1 (ECANx Receive Buffer Full 1).....	307
AD1CON1 (ADC1 Control 1)	325	CxRXFUL2 (ECANx Receive Buffer Full 2).....	307
AD1CON2 (ADC1 Control 2)	327	CxRXMnEID (ECANx Acceptance Filter Mask n Extended Identifier)	306
AD1CON3 (ADC1 Control 3)	329	CxRXMnSID (ECANx Acceptance Filter Mask n Standard Identifier)	306
AD1CON4 (ADC1 Control 4)	330	CxRXOVF1 (ECANx Receive Buffer Overflow 1).....	308
AD1CSSH (ADC1 Input Scan Select High)	335	CxRXOVF2 (ECANx Receive Buffer Overflow 2).....	308
AD1CSSL (ADC1 Input Scan Select Low).....	336	CxTRMnCON (ECANx TX/RX Buffer mn Control)	309
ALTDTRx (PWMx Alternate Dead-Time)	238	CxVEC (ECANx Interrupt Code).....	292
AUXCONx (PWMx Auxiliary Control).....	247	DEVID (Device ID).....	383
CHOP (PWMx Chop Clock Generator).....	234	DEVREV (Device Revision).....	383
CLKDIV (Clock Divisor).....	158	DMALCA (DMA Last Channel Active Status)	150
CM4CON (Comparator 4 Control)	364	DMAPPS (DMA Ping-Pong Status)	151
CMSTAT (Op Amp/Comparator Status)	360	DMAPOW (DMA Peripheral Write Collision Status).....	148
CMxCON (Comparator x Control, x = 1,2,3).....	362	DMARQC (DMA Request Collision Status).....	149
CMxFLTR (Comparator x Filter Control).....	370	DMAxCNT (DMA Channel x Transfer Count).....	146
		DMAxCON (DMA Channel x Control).....	142
		DMAxPAD (DMA Channel x Peripheral Address).....	146
		DMAxREQ (DMA Channel x IRQ Select).....	143