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Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gp506-h-pt

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4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in wordaddressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-6).

Program memory addresses are always word-aligned on the lower word and addresses are incremented, or decremented by two, during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices reserve the addresses between 0x000000 and 0x000200 for hardcoded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address, 0x000000, of Flash memory, with the actual address for the start of code at address, 0x000002, of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in **Section 7.1** "Interrupt Vector Table".



FIGURE 4-6: PROGRAM MEMORY ORGANIZATION



FIGURE 4-10: DATA MEMORY MAP FOR dsPIC33EP256MC20X/50X AND dsPIC33EP256GP50X DEVICES

TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC35	0886	_		JTAGIP<2:()>	—		ICDIP<2:0	>	_	—	—	—	—	_	—	—	4400
IPC36	0888			PTG0IP<2:0)>	—	PT	GWDTIP<	2:0>		P	TGSTEPIP<2	:0>	—	—		—	4440
IPC37	088A		_		_	—	F	PTG3IP<2:)>			PTG2IP<2:0	>	—	F	PTG1IP<2:0>		0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	_	_				—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4		—		_	_	_				—	DAE	DOOVR	—	—		—	0000
INTCON4	08C6		—		_	_	_				—	—	—	—	—		SGHT	0000
INTTREG	08C8	_	_	_	_		ILR<	3:0>		VECNUM<7:0>					0000			

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.3 DATA MEMORY ARBITRATION AND BUS MASTER PRIORITY

EDS accesses from bus masters in the system are arbitrated.

The arbiter for data memory (including EDS) arbitrates between the CPU, the DMA and the ICD module. In the event of coincidental access to a bus by the bus masters, the arbiter determines which bus master access has the highest priority. The other bus masters are suspended and processed after the access of the bus by the bus master with the highest priority.

By default, the CPU is Bus Master 0 (M0) with the highest priority and the ICD is Bus Master 4 (M4) with the lowest priority. The remaining bus master (DMA Controller) is allocated to M3 (M1 and M2 are reserved and cannot be used). The user application may raise or lower the priority of the DMA Controller to be above that of the CPU by setting the appropriate bits in the EDS Bus Master Priority Control (MSTRPR) register. All bus masters with raised priorities will maintain the same priority relationship relative to each other (i.e., M1 being highest and M3 being lowest, with M2 in between). Also, all the bus masters with priorities below

FIGURE 4-18: ARBITER ARCHITECTURE

that of the CPU maintain the same priority relationship relative to each other. The priority schemes for bus masters with different MSTRPR values are tabulated in Table 4-62.

This bus master priority control allows the user application to manipulate the real-time response of the system, either statically during initialization or dynamically in response to real-time events.

TABLE 4-62:	DATA MEMORY BUS
	ARBITER PRIORITY

Briority	MSTRPR<15:0> Bit Setting ⁽¹⁾					
Phoney	0x0000	0x0020				
M0 (highest)	CPU	DMA				
M1	Reserved	CPU				
M2	Reserved	Reserved				
M3	DMA	Reserved				
M4 (lowest)	ICD	ICD				

Note 1: All other values of MSTRPR<15:0> are reserved.



REGISTER 11-15: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

	5444.0	D 44/ 0	D 444 0		D 44/ 0	D 444 0		
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—				SYNCI1R<6:0)>			
bit 15							bit 8	
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
—	—	—		—	—	—	—	
bit 7				-	•		bit 0	
Legend:								
R = Readabl	le bit	W = Writable b	oit	U = Unimplemented bit, read as '0'				
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unknown		
bit 15	Unimplemer	nted: Read as '0)'					
bit 14-8	SYNCI1R<6: (see Table 11	• 0>: Assign PWI I-2 for input pin :	VI Synchroniz selection nur	zation Input 1 to nbers)	o the Correspon	ding RPn Pin b	its	
	1111001 = 	nput tied to RPI	121					
	•							
	•							
	0000001 = I	nout tied to CME	21					
	0000000 = 1	nput tied to Vss						
bit 7-0	Unimplemer	nted: Read as '0)'					

REGISTER 11-16: RPINR38: PERIPHERAL PIN SELECT INPUT REGISTER 38 (dsPIC33EPXXXMC20X AND PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
_				DTCMP1R<6:	0>				
bit 15							bit 8		
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
_	—	_		—	—	_	—		
bit 7		·		÷			bit 0		
Legend:									
R = Readabl	e bit	W = Writable	Writable bit U = Unimplemented bit, read as '0'						
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown			
bit 15	Unimplemer	ted: Read as '	0'						
bit 14-8	DTCMP1R<6 (see Table 11	::0>: Assign PV -2 for input pin	VM Dead-Tim selection nun	e Compensation nbers)	on Input 1 to the	e Correspondine	g RPn Pin bits		
	1111001 = 	nput tied to RPI	121						
	•								
	•								
	0000001 =	nput tied to CM	P1						
	0000000 = li	nput tied to Vss	}						
bit 7-0	Unimplemer	ted: Read as '	0'						

12.2 Timer1 Control Register

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON ⁽¹⁾	—	TSIDL	—	_	—	—	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	TCKPS1	TCKPS0	_	TSYNC ⁽¹⁾	TCS ⁽¹⁾	—
bit 7							bit 0
Legend:							
R = Readab	ole bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own
		(1)					
bit 15	TON: Timer1	On bit ⁽¹⁾					
	1 = Starts 16-	bit Limer1 bit Timer1					
bit 1/	Unimplement	ted: Pead as '	ı'				
bit 13		1 Stop in Idle N	/ode hit				
DIC 15	1 = Discontinu	i stop in lae k	eration when a	device enters l	dle mode		
	0 = Continues	module opera	tion in Idle mo	ode			
bit 12-7	Unimplement	ted: Read as ')'				
bit 6	TGATE: Time	r1 Gated Time	Accumulation	Enable bit			
	When TCS =	<u>1:</u> prod					
	When TCS =	0. 0.					
	1 = Gated tim	<u>e</u> accumulatior	n is enabled				
	0 = Gated tim	e accumulatior	n is disabled				
bit 5-4	TCKPS<1:0>	: Timer1 Input	Clock Prescal	e Select bits			
	11 = 1:256						
	10 = 1:64 01 = 1:8						
	01 = 1.0 00 = 1.1						
bit 3	Unimplement	ted: Read as ')'				
bit 2	TSYNC: Time	er1 External Clo	ock Input Sync	chronization Se	elect bit ⁽¹⁾		
	When TCS =	1:					
	1 = Synchroni	izes external cl	ock input				
	0 = Does not	synchronize ex	ternal clock in	nput			
	This bit is jand	<u>ored</u> .					
bit 1	TCS: Timer1 (Clock Source S	Select bit ⁽¹⁾				
	1 = External c	lock is from pir	n, T1CK (on th	ne rising edge)			
	0 = Internal cl	ock (FP)		5 5-7			
bit 0	Unimplement	ted: Read as ')'				
Note 1: \	When Timer1 is en attempts by user so	abled in Exterr oftware to write	al Synchrono to the TMR1	us Counter mo register are ig	ode (TCS = 1, T nored.	SYNC = 1, TO	N = 1), any

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

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REGISTER 17-3: QEI1STAT: QEI1 STATUS REGISTER (CONTINUED)

bit 2	HOMIEN: Home Input Event Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled
bit 1	IDXIRQ: Status Flag for Index Event Status bit 1 = Index event has occurred 0 = No Index event has occurred
bit 0	IDXIEN: Index Input Event Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled

Note 1: This status bit is only applicable to PIMOD<2:0> modes, '011' and '100'.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 17-7: VEL1CNT: VELOCITY COUNTER 1 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	VELCNT<15:8>									
bit 15 bit 8										
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
			VELC	NT<7:0>						
bit 7							bit 0			
Legend:										
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'										
-n = Value at POR (1' = Bit is set 0' = Bit is cleared x = Bit is unknown							nown			

bit 15-0 VELCNT<15:0>: Velocity Counter bits

REGISTER 17-8: INDX1CNTH: INDEX COUNTER 1 HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXCN	T<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXCN	T<23:16>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 INDXCNT<31:16>: High Word Used to Form 32-Bit Index Counter Register (INDX1CNT) bits

REGISTER 17-9: INDX1CNTL: INDEX COUNTER 1 LOW WORD REGISTER

'1' = Bit is set

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXC	NT<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXC	NT<7:0>			
bit 7							bit 0
Legend:							
R = Readable b	it	W = Writable bit	:	U = Unimpler	mented bit, read	l as '0'	

'0' = Bit is cleared

bit 15-0 INDXCNT<15:0>: Low Word Used to Form 32-Bit Index Counter Register (INDX1CNT) bits

-n = Value at POR

x = Bit is unknown

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 17-17: INT1TMRH: INTERVAL 1 TIMER HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTTM	R<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTTM	R<23:16>			
bit 7							bit 0
Legend:							
R = Readable b	bit	W = Writable bi	it	U = Unimplem	nented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown

bit 15-0 INTTMR<31:16>: High Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

REGISTER 17-18: INT1TMRL: INTERVAL 1 TIMER LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTTM	1R<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTT	/IR<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable b	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 INTTMR<15:0>: Low Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	_	—	—	BCL	GCSTAT	ADD10
bit 15					•		bit 8
R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF
bit 7							bit 0
Legend:		C = Clearab	le bit	HS = Hardwa	re Settable bit	HSC = Hardware S	ettable/Clearable bit
R = Readabl	e bit	W = Writable	e bit	U = Unimplemented bit, read as '0'			
-n = Value at	POR	'1' = Bit is se	et	'0' = Bit is cleared x = Bit is unknown			

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

bit 15	ACKSTAT: Acknowledge Status bit (when operating as I^2C^{TM} master, applicable to master transmit operation)
	1 = NACK received from slave 0 = ACK received from slave
	Hardware is set or clear at the end of slave Acknowledge.
bit 14	TRSTAT: Transmit Status bit (when operating as I^2C master, applicable to master transmit operation) 1 = Master transmit is in progress (8 bits + ACK)
	0 = Master transmit is not in progress Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
bit 13-11	Unimplemented: Read as '0'
bit 10	BCL: Master Bus Collision Detect bit
	1 = A bus collision has been detected during a master operation0 = No bus collision detected
	Hardware is set at detection of a bus collision.
bit 9	GCSTAT: General Call Status bit
	1 = General call address was received
	0 = General call address was not received
1.11.0	Hardware is set when address matches general call address. Hardware is clear at Stop detection.
DIT 8	ADD10: 10-Bit Address Status bit
	I = 10-bit address was matched 0 = 10-bit address was not matched
	Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
bit 7	IWCOL: I2Cx Write Collision Detect bit
	1 = An attempt to write to the I2CxTRN register failed because the I^2 C module is busy 0 = No collision
	Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
bit 6	I2COV: I2Cx Receive Overflow Flag bit
	 1 = A byte was received while the I2CxRCV register was still holding the previous byte 0 = No overflow
	Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
bit 5	D_A: Data/Address bit (when operating as I ² C slave)
	1 = Indicates that the last byte received was data
	 Indicates that the last byte received was a device address Hardware is clear at a device address match. Hardware is set by reception of a slave byte.
bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware is set or clear when a Start, Repeated Start or Stop is detected.

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
_	_	FBP5	FBP4	FBP3	FBP2	FBP1	FBP0
bit 15							bit 8
U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
_	_	FNRB5	FNRB4	FNRB3	FNRB2	FNRB1	FNRB0
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
bit 15-14	Unimplemen	ted: Read as '	0'				
bit 13-8	FBP<5:0>: F	IFO Buffer Poir	nter bits				
	011111 = RE	331 buffer					
	•	50 bullet					
	•						
	•						
	000001 = TR	B1 buffer					
	000000 = TR	RB0 buffer					
bit 7-6	Unimplemen	ted: Read as '	0'				
bit 5-0	FNRB<5:0>:	FIFO Next Rea	ad Buffer Poin	ter bits			
	011111 = RE	331 buffer					
	011110 = RE	330 buffer					
	•						
	•						
	•						
	000001 = TR	(B1 buffer					
	000000 = TR						

REGISTER 21-5: CxFIFO: ECANx FIFO STATUS REGISTER

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U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 15							bit 8
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE
bit 7					·		bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-8	Unimplemen	ted: Read as ')'				
bit 7	IVRIE: Invalid	I Message Inter	rupt Enable b	bit			
	1 = Interrupt r	equest is enab	led				
		request is not e	nabled				
DIT 6	WAKIE: Bus	vvake-up Activi	ty interrupt Er	Table bit			
	$\perp = \text{Interrupt r}$ 0 = Interrupt r	request is enab	nabled				
bit 5	ERRIE: Frror	Interrupt Enab	le bit				
	1 = Interrupt r	request is enab	led				
	0 = Interrupt r	equest is not e	nabled				
bit 4	Unimplemen	ted: Read as ')'				
bit 3	FIFOIE: FIFO	Almost Full Int	errupt Enable	e bit			
	1 = Interrupt r	request is enab	led				
	0 = Interrupt r	request is not e	nabled				
bit 2	RBOVIE: RX	Buffer Overflov	v Interrupt En	able bit			
	1 = Interrupt request is enabled						
hit 1	\cup = interrupt request is not enabled PRIE: DX Buffer Interrupt Enable bit						
bit 1	TDIE: RA DUIIEI INTEITUPI ETIADIE DIL 1 = Interrunt request is enabled						
	0 = Interrupt r	request is not e	nabled				
bit 0	TBIE: TX Buff	fer Interrupt En	able bit				
	1 = Interrupt r	request is enab	led				
	0 = Interrupt r	request is not e	nabled				

REGISTER 21-7: CXINTE: ECANX INTERRUPT ENABLE REGISTER

23.2 ADC Helpful Tips

- 1. The SMPIx control bits in the AD1CON2 register:
 - a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
 - b) When the CSCNA bit in the AD1CON2 registers is set to '1', this determines when the ADC analog scan channel list, defined in the AD1CSSL/AD1CSSH registers, starts over from the beginning.
 - c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
 - d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA.
- 2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMPIx bits and the condition described in 1c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
- 3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer (i.e., ADC1BUF0) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA Controller, before the next ADC conversion is complete to avoid overwriting the previous value.
- 4. The DONE bit (AD1CON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (AD1CON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.

5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for ANO, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUXA selections use ANO-AN2. Carefully study the ADC block diagram to determine the configuration that will best suit your application. Configuration examples are available in the "Analog-to-Digital Converter (ADC)" (DS70621) section in the "dsPIC33/ PIC24 Family Reference Manual".

23.3 ADC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

23.3.1 KEY RESOURCES

- "Analog-to-Digital Converter (ADC)" (DS70621) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 24-8: PTGC1LIM: PTG COUNTER 1 LIMIT REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC1L	IM<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC1L	_IM<7:0>			
bit 7							bit 0
Logond							

Legenu.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGC1LIM<15:0>:** PTG Counter 1 Limit Register bits May be used to specify the loop count for the PTGJMPC1 Step command or as a limit register for the General Purpose Counter 1.

REGISTER 24-9: PTGHOLD: PTG HOLD REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGHOL	_D<15:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			PTGHO	LD<7:0>				
bit 7 k								

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGHOLD<15:0>:** PTG General Purpose Hold Register bits Holds user-supplied data to be copied to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGCOPY command.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

Field	Description						
Wm,Wn	Dividend, Divisor working register pair (direct addressing)						
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}						
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}						
Wn	One of 16 working registers ∈ {W0W15}						
Wnd	One of 16 destination working registers ∈ {W0W15}						
Wns	One of 16 source working registers ∈ {W0W15}						
WREG	W0 (working register used in file register instructions)						
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws] }						
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb] }						
Wx	X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}						
Wxd	X Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}						
Wy	Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}						
Wyd	Y Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}						

TABLE 28-1:	SYMBOLS USED IN OPCODE DESCRIPTIONS ((CONTINUED)

DC CHARACTERISTICS		Standard Operating Condition (unless otherwise stated) Operating temperature -40°C -40°C				is: 3.0V to 3.6V \leq TA \leq +85°C for Industrial \leq TA \leq +125°C for Extended	
Param No.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
		Program Flash Memory					
D130	Eр	Cell Endurance	10,000		_	E/W	-40°C to +125°C
D131	Vpr	VDD for Read	3.0		3.6	V	
D132b	VPEW	VDD for Self-Timed Write	3.0		3.6	V	
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C
D135	IDDP	Supply Current during Programming ⁽²⁾	—	10	—	mA	
D136	IPEAK	Instantaneous Peak Current During Start-up	_	_	150	mA	
D137a	Тре	Page Erase Time	17.7	—	22.9	ms	TPE = 146893 FRC cycles, Ta = +85°C (See Note 3)
D137b	Тре	Page Erase Time	17.5	—	23.1	ms	TPE = 146893 FRC cycles, TA = +125°C (See Note 3)
D138a	Tww	Word Write Cycle Time	41.7	—	53.8	μs	Tww = 346 FRC cycles, TA = +85°C (See Note 3)
D138b	Tww	Word Write Cycle Time	41.2	—	54.4	μs	Tww = 346 FRC cycles, Ta = +125°C (See Note 3)

TABLE 30-14: DC CHARACTERISTICS: PROGRAM MEMORY

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: Parameter characterized but not tested in manufacturing.

3: Other conditions: FRC = 7.37 MHz, TUN<5:0> = 011111 (for Minimum), TUN<5:0> = 100000 (for Maximum). This parameter depends on the FRC accuracy (see Table 30-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). For complete details on calculating the Minimum and Maximum time, see Section 5.3 "Programming Operations".



FIGURE 30-19: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

AC CHARACTERISTICS		$ \begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)}^{(1)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array} $							
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions		
	ADC Accuracy (12-Bit Mode)								
AD20a	Nr	Resolution	12 Data Bits		bits				
AD21a	INL	Integral Nonlinearity	-2.5		2.5	LSb	-40°C ≤ TA ≤ +85°C (Note 2)		
			-5.5		5.5	LSb	+85°C < TA \leq +125°C (Note 2)		
AD22a	DNL	Differential Nonlinearity	-1		1	LSb	-40°C \leq TA \leq +85°C (Note 2)		
			-1		1	LSb	+85°C < TA \leq +125°C (Note 2)		
AD23a	Gerr	Gain Error ⁽³⁾	-10		10	LSb	-40°C \leq TA \leq +85°C (Note 2)		
			-10		10	LSb	+85°C < TA \leq +125°C (Note 2)		
AD24a	EOFF	Offset Error	-5		5	LSb	$-40^{\circ}C \le TA \le +85^{\circ}C$ (Note 2)		
			-5		5	LSb	+85°C < TA \leq +125°C (Note 2)		
AD25a	—	Monotonicity	—			—	Guaranteed		
	Dynamic Performance (12-Bit Mode)								
AD30a	THD	Total Harmonic Distortion ⁽³⁾	—	75		dB			
AD31a	SINAD	Signal to Noise and Distortion ⁽³⁾		68	-	dB			
AD32a	SFDR	Spurious Free Dynamic Range ⁽³⁾	_	80	_	dB			
AD33a	Fnyq	Input Signal Bandwidth ⁽³⁾	_	250	—	kHz			
AD34a	ENOB	Effective Number of Bits ⁽³⁾	11.09	11.3	_	bits			

TABLE 30-58: ADC MODULE SPECIFICATIONS (12-BIT MODE)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

3: Parameters are characterized but not tested in manufacturing.

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	E	0.40 BSC		
Optional Center Pad Width	W2			4.45
Optional Center Pad Length	T2			4.45
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A