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Applications of "Embedded - Microcontrollers"

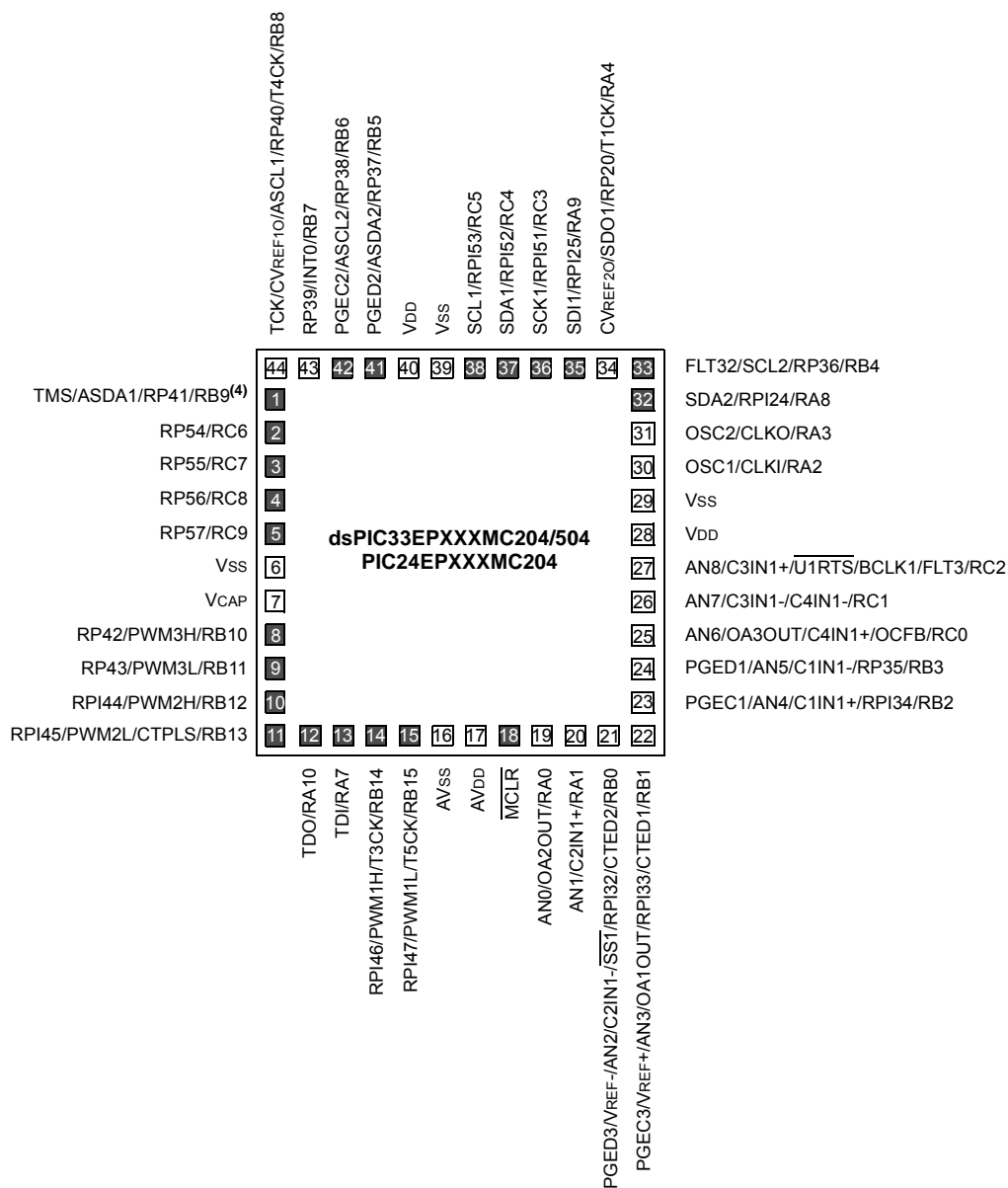| Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gp506-i-mr

Pin Diagrams (Continued)

44-Pin VTLA[1,2,3]

■ = Pins are up to 5V tolerant

Top pins (44–33):
- 44 TCK/CV$_{REF1O}$/ASCL1/RP40/T4CK/RB8
- 43 RP39/INT0/RB7
- 42 PGEC2/ASCL2/RP38/RB6
- 41 PGED2/ASDA2/RP37/RB5
- 40 V$_{DD}$
- 39 V$_{SS}$
- 38 SCL1/RPI53/RC5
- 37 SDA1/RPI52/RC4
- 36 SCK1/RPI51/RC3
- 35 SDI1/RPI25/RA9
- 34 CV$_{REF2O}$/SDO1/RP20/T1CK/RA4

Left pins (1–11):
- 1 TMS/ASDA1/RP41/RB9[4]
- 2 RP54/RC6
- 3 RP55/RC7
- 4 RP56/RC8
- 5 RP57/RC9
- 6 V$_{SS}$
- 7 V$_{CAP}$
- 8 RP42/PWM3H/RB10
- 9 RP43/PWM3L/RB11
- 10 RPI44/PWM2H/RB12
- 11 RPI45/PWM2L/CTPLS/RB13

Center:
dsPIC33EPXXXMC204/504
PIC24EPXXXMC204

Right pins (33–22):
- 33 FLT32/SCL2/RP36/RB4
- 32 SDA2/RPI24/RA8
- 31 OSC2/CLKO/RA3
- 30 OSC1/CLKI/RA2
- 29 V$_{SS}$
- 28 V$_{DD}$
- 27 AN8/C3IN1+/U1RTS/BCLK1/FLT3/RC2
- 26 AN7/C3IN1-/C4IN1-/RC1
- 25 AN6/OA3OUT/C4IN1+/OCFB/RC0
- 24 PGED1/AN5/C1IN1-/RP35/RB3
- 23 PGEC1/AN4/C1IN1+/RPI34/RB2

Bottom pins (12–22):
- 12 TDO/RA10
- 13 TDI/RA7
- 14 RPI46/PWM1H/T3CK/RB14
- 15 RPI47/PWM1L/T5CK/RB15
- 16 AV$_{SS}$
- 17 AV$_{DD}$
- 18 MCLR
- 19 AN0/OA2OUT/RA0
- 20 AN1/C2IN1+/RA1
- 21 PGED3/V$_{REF}$-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0
- 22 PGEC3/V$_{REF}$+/AN3/OA1OUT/RPI33/CTED1/RB1

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to V$_{SS}$ externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

TABLE 4-19: SPI1 AND SPI2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	SPIBEC<2:0>			SRMPT	SPIROV	SRXMPT	SISEL<2:0>			SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE<2:0>			PPRE<1:0>		0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI1BUF	0248	SPI1 Transmit and Receive Buffer Register																0000
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	SPIBEC<2:0>			SRMPT	SPIROV	SRXMPT	SISEL<2:0>			SPITBF	SPIRBF	0000
SPI2CON1	0262	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE<2:0>			PPRE<1:0>		0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI2BUF	0268	SPI2 Transmit and Receive Buffer Register																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-34: NVM REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0728	WR	WREN	WRERR	NVMSIDL	—	—	—	—	—	—	—	—	NVMOP<3:0>				0000
NVMADRL	072A	NVMADR<15:0>																0000
NVMADRH	072C	—	—	—	—	—	—	—	NVMADR<23:16>									0000
NVMKEY	072E	—	—	—	—	—	—	—	NVMKEY<7:0>									0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-35: SYSTEM CONTROL REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	—	—	VREGSF	—	CM	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	Note 1
OSCCON	0742	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	IOLOCK	LOCK	—	CF	—	—	OSWEN	Note 2
CLKDIV	0744	ROI	DOZE<2:0>			DOZEN	FRCDIV<2:0>			PLLPOST<1:0>		—	PLLPRE<4:0>					0030
PLLFBD	0746	—	—	—	—	—	—	—	PLLDIV<8:0>									0030
OSCTUN	0748	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: RCON register Reset values are dependent on the type of Reset.
2: OSCCON register Reset values are dependent on the Configuration Fuses.

TABLE 4-36: REFERENCE CLOCK REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
REFOCON	074E	ROON	—	ROSSLP	ROSEL	RODIV<3:0>				—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.2 EXTENDED X DATA SPACE

The lower portion of the base address space range, between 0x0000 and 0x7FFF, is always accessible regardless of the contents of the Data Space Page registers. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x007FFF with the base address bit, EA<15> = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF, of base Data Space, in combination with DSRPAG = 0x000 or DSWPAG = 0x000. Consequently, DSRPAG and DSWPAG are initialized to 0x001 at Reset.

> **Note 1:** DSxPAG should not be used to access Page 0. An EDS access with DSxPAG set to 0x000 will generate an address error trap.
>
> **2:** Clearing the DSxPAG in software has no effect.

The remaining pages, including both EDS and PSV pages, are only accessible using the DSRPAG or DSWPAG registers in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where base address bit, EA<15> = 1.

For example, when DSRPAG = 0x001 or DSWPAG = 0x001, accesses to the upper 32 Kbytes, 0x8000 to 0xFFFF, of the Data Space will map to the EDS address range of 0x008000 to 0x00FFFF. When DSRPAG = 0x002 or DSWPAG = 0x002, accesses to the upper 32 Kbytes of the Data Space will map to the EDS address range of 0x010000 to 0x017FFF and so on, as shown in the EDS memory map in Figure 4-17.

For more information on the PSV page access using Data Space Page registers, refer to the **"Program Space Visibility from Data Space"** section in **"Program Memory"** (DS70613) of the *"dsPIC33/PIC24 Family Reference Manual"*.

FIGURE 4-17:   EDS MEMORY MAP
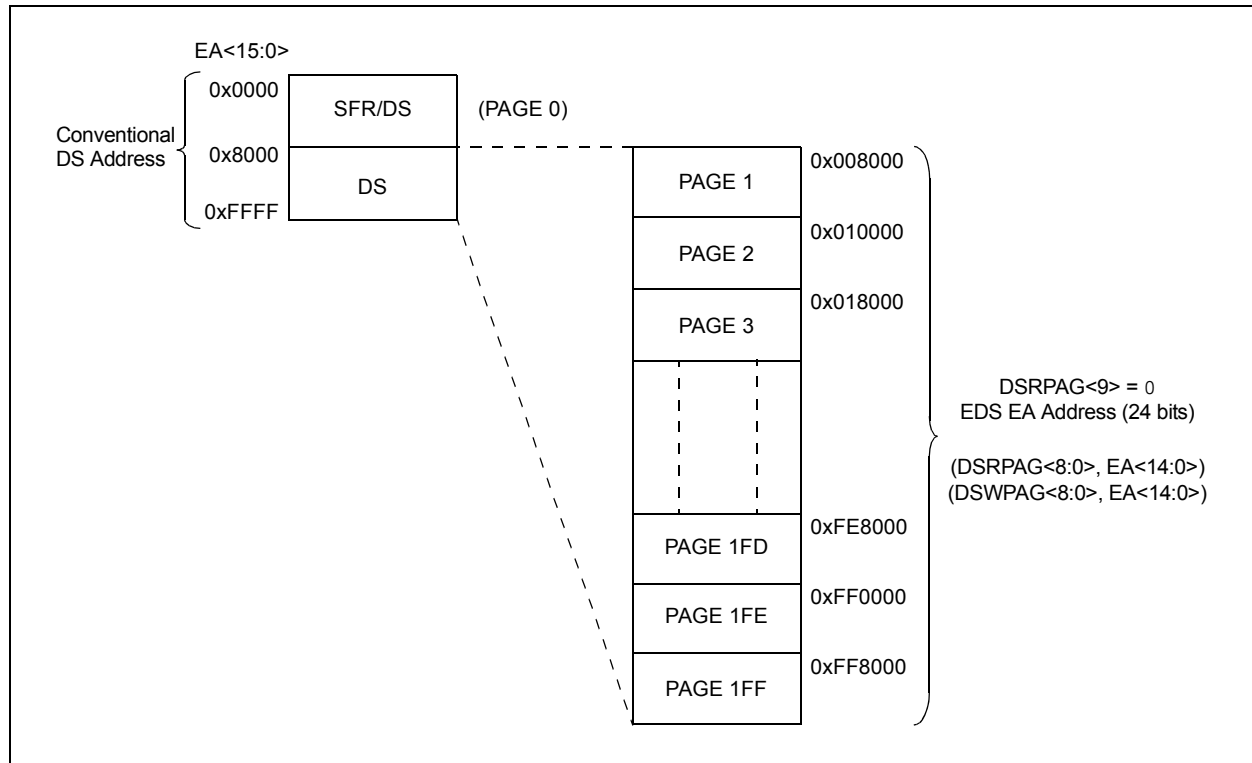
4.4.3 DATA MEMORY ARBITRATION AND BUS MASTER PRIORITY

EDS accesses from bus masters in the system are arbitrated.

The arbiter for data memory (including EDS) arbitrates between the CPU, the DMA and the ICD module. In the event of coincidental access to a bus by the bus masters, the arbiter determines which bus master access has the highest priority. The other bus masters are suspended and processed after the access of the bus by the bus master with the highest priority.

By default, the CPU is Bus Master 0 (M0) with the highest priority and the ICD is Bus Master 4 (M4) with the lowest priority. The remaining bus master (DMA Controller) is allocated to M3 (M1 and M2 are reserved and cannot be used). The user application may raise or lower the priority of the DMA Controller to be above that of the CPU by setting the appropriate bits in the EDS Bus Master Priority Control (MSTRPR) register. All bus masters with raised priorities will maintain the same priority relationship relative to each other (i.e., M1 being highest and M3 being lowest, with M2 in between). Also, all the bus masters with priorities below

that of the CPU maintain the same priority relationship relative to each other. The priority schemes for bus masters with different MSTRPR values are tabulated in Table 4-62.

This bus master priority control allows the user application to manipulate the real-time response of the system, either statically during initialization or dynamically in response to real-time events.

TABLE 4-62: DATA MEMORY BUS ARBITER PRIORITY

Priority	MSTRPR<15:0> Bit Setting[1]	
	0x0000	0x0020
M0 (highest)	CPU	DMA
M1	Reserved	CPU
M2	Reserved	Reserved
M3	DMA	Reserved
M4 (lowest)	ICD	ICD

Note 1: All other values of MSTRPR<15:0> are reserved.

FIGURE 4-18: ARBITER ARCHITECTURE
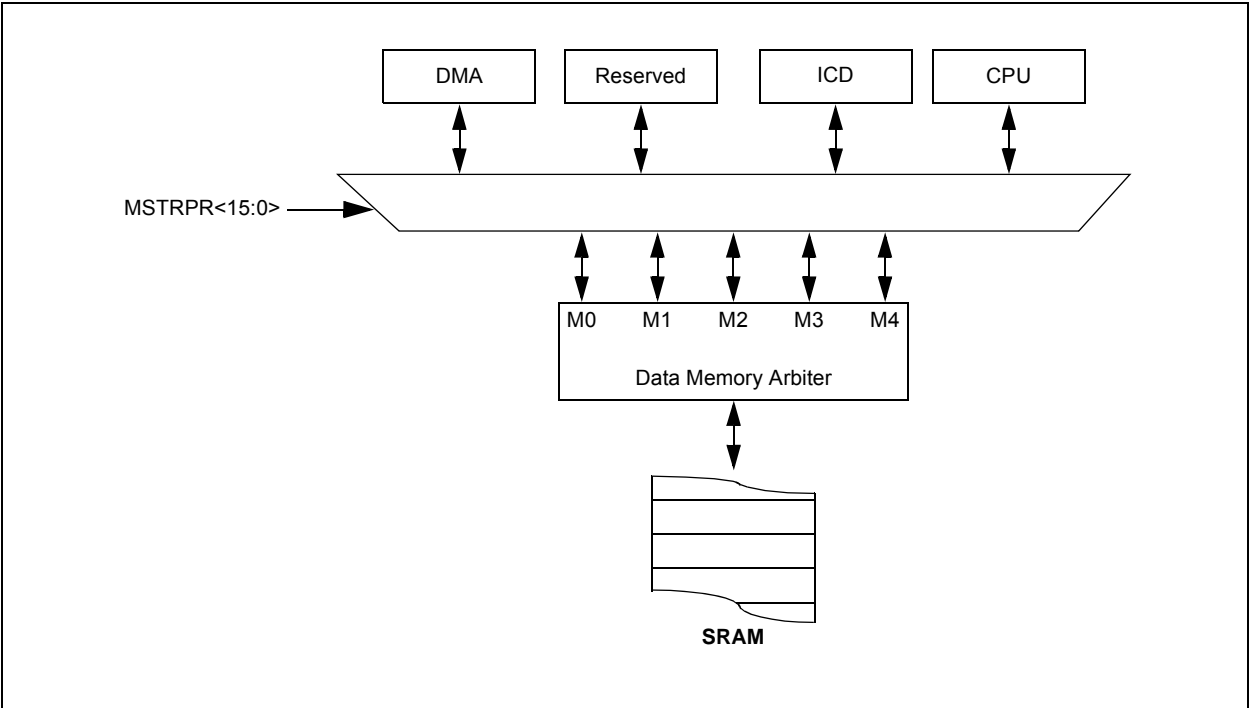
REGISTER 7-1: **SR: CPU STATUS REGISTER**[1]

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA	SB	OAB	SAB	DA	DC
bit 15							bit 8

R/W-0[3]	R/W-0[3]	R/W-0[3]	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL<2:0>[2]			RA	N	OV	Z	C
bit 7							bit 0

Legend:		C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5   **IPL<2:0>:** CPU Interrupt Priority Level Status bits[2,3]

111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

Note 1: For complete register details, see Register 3-1.

2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/S-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
FORCE[1]	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0
bit 7							bit 0

Legend:			
	S = Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15　　**FORCE:** Force DMA Transfer bit[1]

　　　　　1 = Forces a single DMA transfer (Manual mode)
　　　　　0 = Automatic DMA transfer initiation by DMA request

bit 14-8　**Unimplemented:** Read as '0'

bit 7-0　　**IRQSEL<7:0>:** DMA Peripheral IRQ Number Select bits

　　　　　01000110 = ECAN1 – TX Data Request[2]
　　　　　00100110 = IC4 – Input Capture 4
　　　　　00100101 = IC3 – Input Capture 3
　　　　　00100010 = ECAN1 – RX Data Ready[2]
　　　　　00100001 = SPI2 Transfer Done
　　　　　00011111 = UART2TX – UART2 Transmitter
　　　　　00011110 = UART2RX – UART2 Receiver
　　　　　00011100 = TMR5 – Timer5
　　　　　00011011 = TMR4 – Timer4
　　　　　00011010 = OC4 – Output Compare 4
　　　　　00011001 = OC3 – Output Compare 3
　　　　　00001101 = ADC1 – ADC1 Convert done
　　　　　00001100 = UART1TX – UART1 Transmitter
　　　　　00001011 = UART1RX – UART1 Receiver
　　　　　00001010 = SPI1 – Transfer Done
　　　　　00001000 = TMR3 – Timer3
　　　　　00000111 = TMR2 – Timer2
　　　　　00000110 = OC2 – Output Compare 2
　　　　　00000101 = IC2 – Input Capture 2
　　　　　00000010 = OC1 – Output Compare 1
　　　　　00000001 = IC1 – Input Capture 1
　　　　　00000000 = INT0 – External Interrupt 0

Note 1: The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).

　　2: This selection is available in dsPIC33EPXXXGP/MC50X devices only.

9.1   CPU Clocking System

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X family of devices provides six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase Locked Loop (PLL)
- FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator

Instruction execution speed or device operating frequency, F_{CY}, is given by Equation 9-1.

EQUATION 9-1:   DEVICE OPERATING FREQUENCY

$$F_{CY} = F_{osc}/2$$

Figure 9-2 is a block diagram of the PLL module.

Equation 9-2 provides the relationship between input frequency (F_{IN}) and output frequency (F_{PLLO}). In clock modes S1 and S3, when the PLL output is selected, $F_{OSC} = F_{PLLO}$.

Equation 9-3 provides the relationship between input frequency (F_{IN}) and VCO frequency (F_{VCO}).

FIGURE 9-2:   PLL BLOCK DIAGRAM
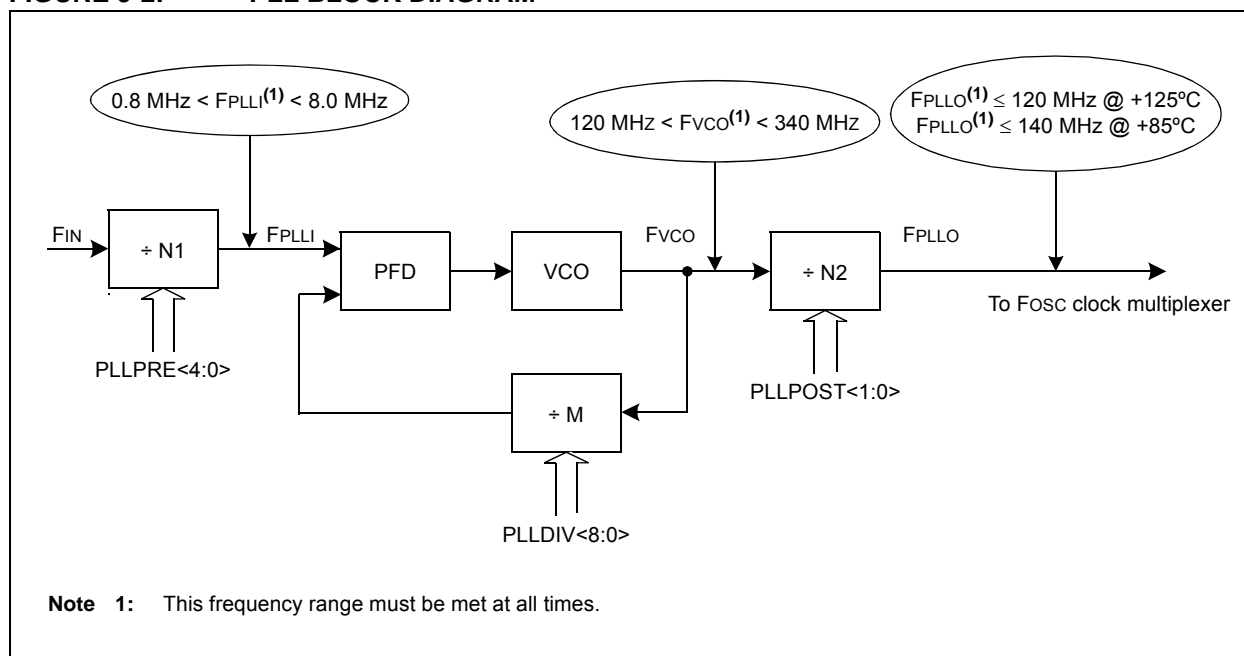
EQUATION 9-2: F_{PLLO} CALCULATION

$$F_{PLLO} = F_{IN} \times \left(\frac{M}{N1 \times N2}\right) = F_{IN} \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2) \times 2(PLLPOST + 1)}\right)$$

Where:

$N1 = PLLPRE + 2$

$N2 = 2 \times (PLLPOST + 1)$

$M = PLLDIV + 2$

EQUATION 9-3: F_{VCO} CALCULATION

$$F_{VCO} = F_{IN} \times \left(\frac{M}{N1}\right) = F_{IN} \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2)}\right)$$

REGISTER 9-2:   CLKDIV: CLOCK DIVISOR REGISTER (CONTINUED)

bit 4-0   **PLLPRE<4:0>:** PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)

11111 = Input divided by 33

•

•

•

00001 = Input divided by 3

00000 = Input divided by 2 (default)

Note 1:   The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.

2:   This bit is cleared when the ROI bit is set and an interrupt occurs.

3:   The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

REGISTER 11-24:   RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP57R<5:0>			
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP56R<5:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14   **Unimplemented:** Read as '0'

bit 13-8   **RP57R<5:0>:** Peripheral Output Function is Assigned to RP57 Output Pin bits
(see Table 11-3 for peripheral function numbers)

bit 7-6   **Unimplemented:** Read as '0'

bit 5-0   **RP56R<5:0>:** Peripheral Output Function is Assigned to RP56 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 11-25:   RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP97R<5:0>			
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14   **Unimplemented:** Read as '0'

bit 13-8   **RP97R<5:0>:** Peripheral Output Function is Assigned to RP97 Output Pin bits
(see Table 11-3 for peripheral function numbers)

bit 7-0   **Unimplemented:** Read as '0'

NOTES:

REGISTER 16-3: **PTPER: PWMx PRIMARY MASTER TIME BASE PERIOD REGISTER**

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PTPER<15:8>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
PTPER<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **PTPER<15:0>:** Primary Master Time Base (PMTMR) Period Value bits

REGISTER 16-4: **SEVTCMP: PWMx PRIMARY SPECIAL EVENT COMPARE REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **SEVTCMP<15:0>:** Special Event Compare Count Value bits

REGISTER 16-16: LEBCONx: PWMx LEADING-EDGE BLANKING CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	BCH[1]	BCL[1]	BPHH	BPHL	BPLH	BPLL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PHR:** PWMxH Rising Edge Trigger Enable bit

1 = Rising edge of PWMxH will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores rising edge of PWMxH

bit 14 **PHF:** PWMxH Falling Edge Trigger Enable bit

1 = Falling edge of PWMxH will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores falling edge of PWMxH

bit 13 **PLR:** PWMxL Rising Edge Trigger Enable bit

1 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores rising edge of PWMxL

bit 12 **PLF:** PWMxL Falling Edge Trigger Enable bit

1 = Falling edge of PWMxL will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores falling edge of PWMxL

bit 11 **FLTLEBEN:** Fault Input Leading-Edge Blanking Enable bit

1 = Leading-Edge Blanking is applied to selected Fault input
0 = Leading-Edge Blanking is not applied to selected Fault input

bit 10 **CLLEBEN:** Current-Limit Leading-Edge Blanking Enable bit

1 = Leading-Edge Blanking is applied to selected current-limit input
0 = Leading-Edge Blanking is not applied to selected current-limit input

bit 9-6 **Unimplemented:** Read as '0'

bit 5 **BCH:** Blanking in Selected Blanking Signal High Enable bit[1]

1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is high
0 = No blanking when selected blanking signal is high

bit 4 **BCL:** Blanking in Selected Blanking Signal Low Enable bit[1]

1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low
0 = No blanking when selected blanking signal is low

bit 3 **BPHH:** Blanking in PWMxH High Enable bit

1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is high
0 = No blanking when PWMxH output is high

bit 2 **BPHL:** Blanking in PWMxH Low Enable bit

1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low
0 = No blanking when PWMxH output is low

bit 1 **BPLH:** Blanking in PWMxL High Enable bit

1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high
0 = No blanking when PWMxL output is high

bit 0 **BPLL:** Blanking in PWMxL Low Enable bit

1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is low
0 = No blanking when PWMxL output is low

Note 1: The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

FIGURE 18-1: **SPIx MODULE BLOCK DIAGRAM**

Note 1: In Standard mode, the FIFO is only one level deep.

19.1 I²C Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

> **Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

19.1.1 KEY RESOURCES

- **"Inter-Integrated Circuit (I²C)"** (DS70330) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

23.2   ADC Helpful Tips

1. The SMPIx control bits in the AD1CON2 register:

    a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.

    b) When the CSCNA bit in the AD1CON2 registers is set to '1', this determines when the ADC analog scan channel list, defined in the AD1CSSL/AD1CSSH registers, starts over from the beginning.

    c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.

    d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA.

2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMPIx bits and the condition described in 1c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.

3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer (i.e., ADC1BUF0) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA Controller, before the next ADC conversion is complete to avoid overwriting the previous value.

4. The DONE bit (AD1CON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (AD1CON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.

5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for AN0, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUXA selections use AN0-AN2. Carefully study the ADC block diagram to determine the configuration that will best suit your application. Configuration examples are available in the **"Analog-to-Digital Converter (ADC)"** (DS70621) section in the *"dsPIC33/ PIC24 Family Reference Manual"*.

23.3   ADC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

> **Note:**   In the event you are not able to access the product page using the link above, enter this URL in your browser:
> http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

23.3.1   KEY RESOURCES

*   **"Analog-to-Digital Converter (ADC)"** (DS70621) in the *"dsPIC33/PIC24 Family Reference Manual"*
*   Code Samples
*   Application Notes
*   Software Libraries
*   Webinars
*   All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
*   Development Tools

NOTES:

29.0   DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

• Integrated Development Environment
   - MPLAB® X IDE Software
• Compilers/Assemblers/Linkers
   - MPLAB XC Compiler
   - MPASM™ Assembler
   - MPLINK™ Object Linker/
   MPLIB™ Object Librarian
   - MPLAB Assembler/Linker/Librarian for Various Device Families
• Simulators
   - MPLAB X SIM Software Simulator
• Emulators
   - MPLAB REAL ICE™ In-Circuit Emulator
• In-Circuit Debuggers/Programmers
   - MPLAB ICD 3
   - PICkit™ 3
• Device Programmers
   - MPLAB PM3 Device Programmer
• Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
• Third-party development tools

29.1   MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

• Color syntax highlighting
• Smart code completion makes suggestions and provides hints as you type
• Automatic code formatting based on user-defined rules
• Live parsing

User-Friendly, Customizable Interface:

• Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
• Call graph window

Project-Based Workspaces:

• Multiple projects
• Multiple tools
• Multiple configurations
• Simultaneous debugging sessions

File History and Bug Tracking:

• Local file history feature
• Built-in support for Bugzilla issue tracker

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 30.0 "Electrical Characteristics"	Removed Voltage on V_{CAP} with respect to V_{SS} and added Note 5 in Absolute Maximum Ratings[1].
	Removed Parameter DC18 (V_{CORE}) and Note 3 from the DC Temperature and Voltage Specifications (see Table 30-4).
	Updated Note 1 in the DC Characteristics: Operating Current (I_{DD}) (see Table 30-6).
	Updated Note 1 in the DC Characteristics: Idle Current (I_{IDLE}) (see Table 30-7).
	Changed the Typical values for Parameters DC60a-DC60d and updated Note 1 in the DC Characteristics: Power-down Current (I_{PD}) (see Table 30-8).
	Updated Note 1 in the DC Characteristics: Doze Current (I_{DOZE}) (see Table 30-9).
	Updated Note 2 in the Electrical Characteristics: BOR (see Table 30-12).
	Updated Parameters CM20 and CM31, and added Parameters CM44 and CM45 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14).
	Added the Op amp/Comparator Reference Voltage Settling Time Specifications (see Table 30-15).
	Added Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16).
	Updated Internal FRC Accuracy Parameter F20a (see Table 30-21).
	Updated the Typical value and Units for Parameter CTMUI1, and added Parameters CTMUI4, CTMUFV1, and CTMUFV2 to the CTMU Current Source Specifications (see Table 30-55).
Section 31.0 "Packaging Information"	Updated packages by replacing references of VLAP with TLA.
"Product Identification System"	Changed VLAP to TLA.

TABLE A-2:   MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"	Updated the High-Speed PWM Module Register Interconnection Diagram (see Figure 16-2). Added the TRGCONx and TRIGx registers (see Register 16-12 and Register 16-14, respectively).
Section 21.0 "Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)"	Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1).
Section 22.0 "Charge Time Measurement Unit (CTMU)"	Updated the IRNG<1:0> bit value definitions and added Note 2 in the CTMU Current Control Register (see Register 22-3).
Section 25.0 "Op amp/ Comparator Module"	Updated the Op amp/Comparator I/O Operating Modes Diagram (see Figure 25-1). Updated the User-programmable Blanking Function Block Diagram (see Figure 25-3). Updated the Digital Filter Interconnect Block Diagram (see Figure 25-4). Added **Section 25.1 "Op amp Application Considerations"**. Added Note 2 to the Comparator Control Register (see Register 25-2). Updated the bit definitions in the Comparator Mask Gating Control Register (see Register 25-5).
Section 27.0 "Special Features"	Updated the FICD Configuration Register, updated Note 1, and added Note 3 in the Configuration Byte Register Map (see Table 27-1). Added **Section 27.2 "User ID Words"**.
Section 30.0 "Electrical Characteristics"	Updated the following Absolute Maximum Ratings: • Maximum current out of V_{SS} pin • Maximum current into V_{DD} pin Added Note 1 to the Operating MIPS vs. Voltage (see Table 30-1). Updated all Idle Current (I_{IDLE}) Typical and Maximum DC Characteristics values (see Table 30-7). Updated all Doze Current (I_{DOZE}) Typical and Maximum DC Characteristics values (see Table 30-9). Added Note 2, removed Parameter CM24, updated the Typical values Parameters CM10, CM20, CM21, CM32, CM41, CM44, and CM45, and updated the Minimum values for CM40 and CM41, and the Maximum value for CM40 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14). Updated Note 2 and the Typical value for Parameter VR310 in the Op amp/ Comparator Reference Voltage Settling Time Specifications (see Table 30-15). Added Note 1, removed Parameter VRD312, and added Parameter VRD314 to the Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16). Updated the Minimum, Typical, and Maximum values for Internal LPRC Accuracy (see Table 30-22). Updated the Minimum, Typical, and Maximum values for Parameter SY37 in the Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer Timing Requirements (see Table 30-24). The Maximum Data Rate values were updated for the SPI2 Maximum Data/Clock Rate Summary (see Table 30-35)