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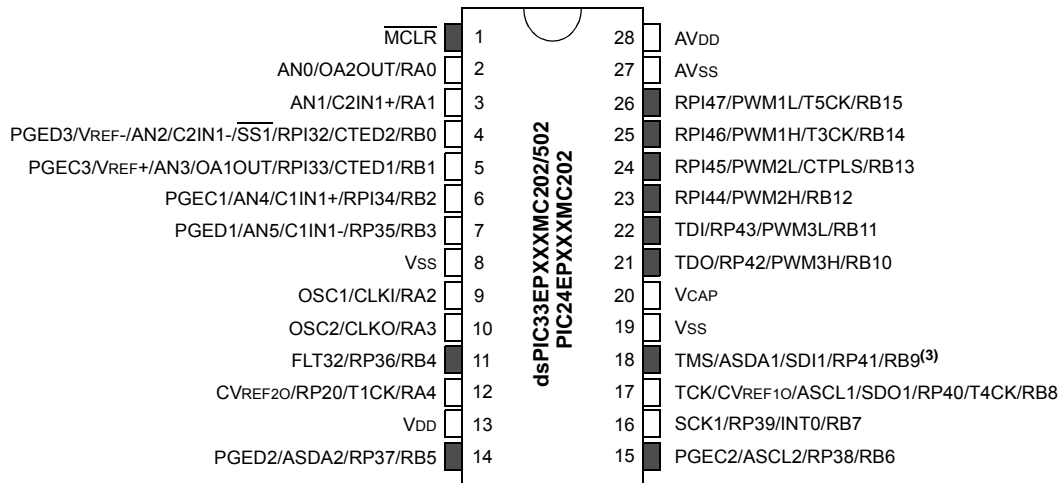
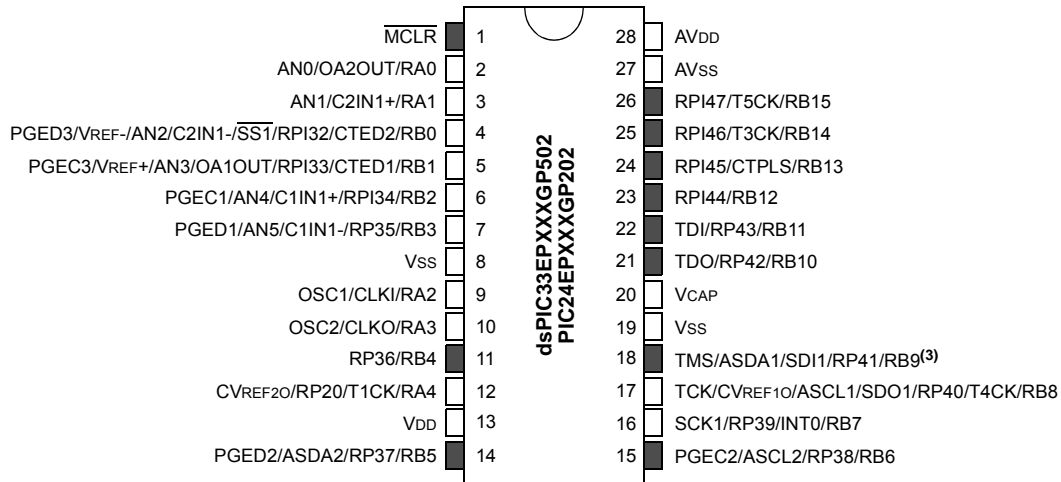
#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc202-e-sp">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc202-e-sp</a>

## Pin Diagrams

### 28-Pin SPDIP/SOIC/SSOP<sup>(1,2)</sup>

■ = Pins are up to 5V tolerant



- Note 1:** The RPN/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## 2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS AND MICROCONTROLLERS

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com))

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

### 2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins  
(see **Section 2.2 “Decoupling Capacitors”**)
- All AVDD and AVSS pins (regardless if ADC module is not used)  
(see **Section 2.2 “Decoupling Capacitors”**)
- VCAP  
(see **Section 2.3 “CPU Logic Filter Capacitor Connection (VCAP)”**)
- MCLR pin  
(see **Section 2.4 “Master Clear (MCLR) Pin”**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes  
(see **Section 2.5 “ICSP Pins”**)
- OSC1 and OSC2 pins when external oscillator source is used  
(see **Section 2.6 “External Oscillator Pins”**)

Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for the ADC module is implemented

**Note:** The AVDD and AVSS pins must be connected, independent of the ADC voltage reference source.

### 2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1  $\mu$ F (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01  $\mu$ F to 0.001  $\mu$ F. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1  $\mu$ F in parallel with 0.001  $\mu$ F.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

**TABLE 4-23: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY (CONTINUED)**

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1RXF11EID	046E	EID<15:8>								EID<7:0>								xxxx
C1RXF12SID	0470	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF12EID	0472	EID<15:8>								EID<7:0>								xxxx
C1RXF13SID	0474	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF13EID	0476	EID<15:8>								EID<7:0>								xxxx
C1RXF14SID	0478	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF14EID	047A	EID<15:8>								EID<7:0>								xxxx
C1RXF15SID	047C	SID<10:3>								SID<2:0>		—	EXIDE	—	EID<17:16>			xxxx
C1RXF15EID	047E	EID<15:8>								EID<7:0>								xxxx

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## 4.6 Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either Data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y Data Spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

### 4.6.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified, and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

**Note:** Y space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

### 4.6.2 W ADDRESS REGISTER SELECTION

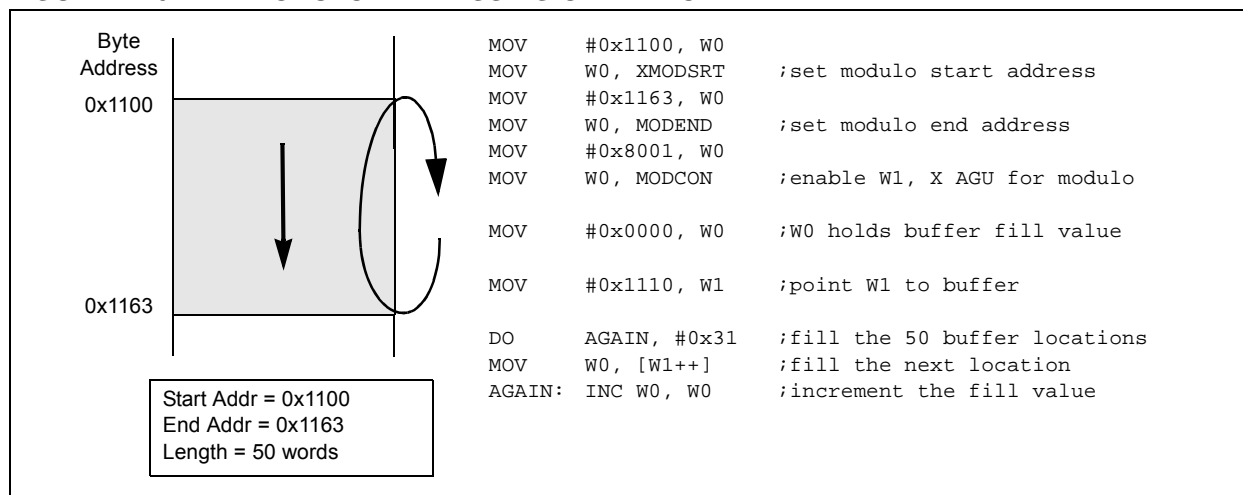
The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = 1111, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = 1111, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X Data Space when XWM is set to any value other than '1111' and the XMODEN bit is set (MODCON<15>).

The Y Address Space Pointer W register (YWM), to which Modulo Addressing is to be applied, is stored in MODCON<7:4>. Modulo Addressing is enabled for Y Data Space when YWM is set to any value other than '1111' and the YMODEN bit is set at MODCON<14>.

**FIGURE 4-20: MODULO ADDRESSING OPERATION EXAMPLE**



**REGISTER 6-1: RCON: RESET CONTROL REGISTER<sup>(1)</sup>**

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	—	—	VREGSF	—	CM	VREGS
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN <sup>(2)</sup>	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15      **TRAPR:** Trap Reset Flag bit  
 1 = A Trap Conflict Reset has occurred  
 0 = A Trap Conflict Reset has not occurred
- bit 14      **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit  
 1 = An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset  
 0 = An illegal opcode or Uninitialized W register Reset has not occurred
- bit 13-12      **Unimplemented:** Read as '0'
- bit 11      **VREGSF:** Flash Voltage Regulator Standby During Sleep bit  
 1 = Flash voltage regulator is active during Sleep  
 0 = Flash voltage regulator goes into Standby mode during Sleep
- bit 10      **Unimplemented:** Read as '0'
- bit 9      **CM:** Configuration Mismatch Flag bit  
 1 = A Configuration Mismatch Reset has occurred.  
 0 = A Configuration Mismatch Reset has not occurred
- bit 8      **VREGS:** Voltage Regulator Standby During Sleep bit  
 1 = Voltage regulator is active during Sleep  
 0 = Voltage regulator goes into Standby mode during Sleep
- bit 7      **EXTR:** External Reset ( $\overline{\text{MCLR}}$ ) Pin bit  
 1 = A Master Clear (pin) Reset has occurred  
 0 = A Master Clear (pin) Reset has not occurred
- bit 6      **SWR:** Software RESET (Instruction) Flag bit  
 1 = A RESET instruction has been executed  
 0 = A RESET instruction has not been executed
- bit 5      **SWDTEN:** Software Enable/Disable of WDT bit<sup>(2)</sup>  
 1 = WDT is enabled  
 0 = WDT is disabled
- bit 4      **WDTO:** Watchdog Timer Time-out Flag bit  
 1 = WDT time-out has occurred  
 0 = WDT time-out has not occurred

- Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
- 2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

**REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER (CONTINUED)**

bit 4-0      **PLLPRE<4:0>**: PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)  
11111 = Input divided by 33  
•  
•  
•  
00001 = Input divided by 3  
00000 = Input divided by 2 (default)

- Note 1:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
- 2:** This bit is cleared when the ROI bit is set and an interrupt occurs.
- 3:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

### 11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx and TRISx registers for data control, port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs other than VDD by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum VIH specification for that particular pin.

See the “Pin Diagrams” section for the available 5V tolerant pins and Table 30-11 for the maximum VIH specification for each pin.

## 11.2 Configuring Analog and Digital Port Pins

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of analog in the Pinout I/O Descriptions (see Table 1-1).

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or comparator module.

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

### 11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP, as shown in Example 11-1.

## 11.3 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the Change Notification (CN) functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups and pull-downs act as a current source or sink source connected to the pin and eliminate the need for external resistors when push button, or keypad devices are connected. The pull-ups and pull-downs are enabled separately, using the CNPUs and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

**Note:** Pull-ups and pull-downs on Change Notification pins should always be disabled when the port pin is configured as a digital output.

### EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

```
MOV    0xFF00, W0    ; Configure PORTB<15:8>
                        ; as inputs
MOV    W0, TRISB      ; and PORTB<7:0>
                        ; as outputs
NOP                                ; Delay 1 cycle
BTSS   PORTB, #13     ; Next Instruction
```



## 12.0 TIMER1

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “Timers” (DS70362) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated in Asynchronous Counter mode from an external clock source
- The external clock input (T1CK) can optionally be synchronized to the internal device clock and the clock synchronization is performed after the prescaler

A block diagram of Timer1 is shown in Figure 12-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (Fcy). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

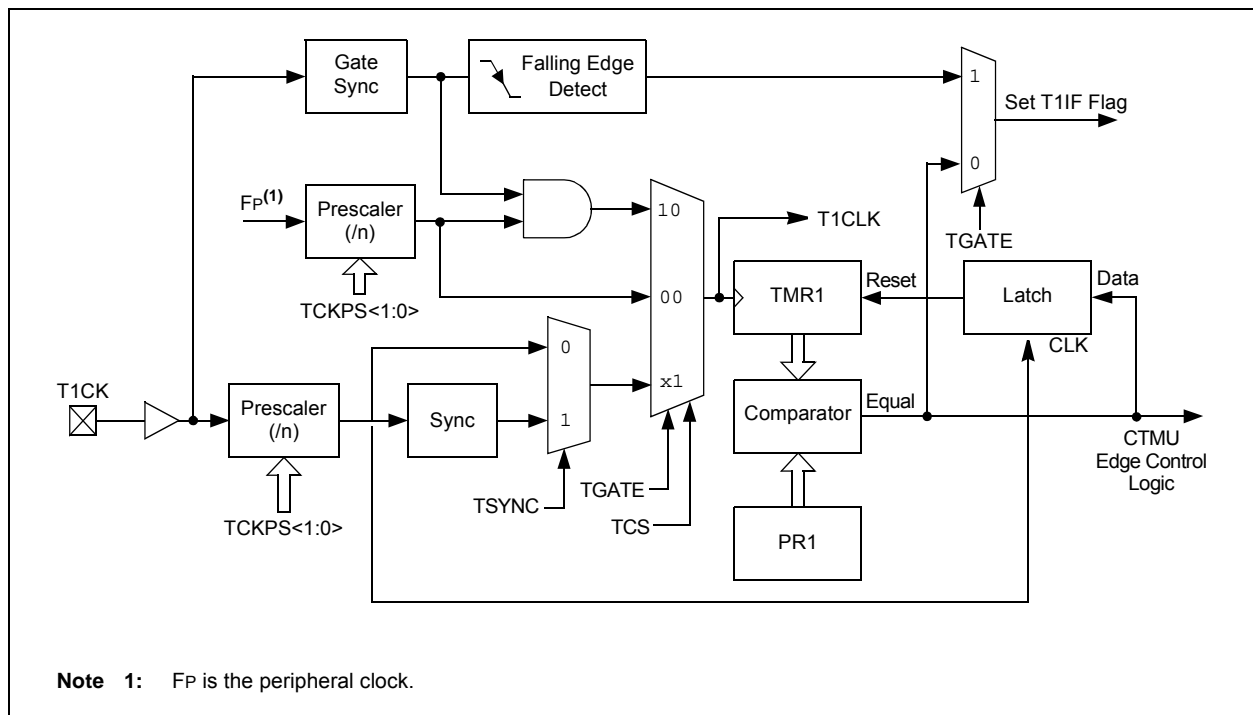
- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit setting for different operating modes are given in the Table 12-1.

**TABLE 12-1: TIMER MODE SETTINGS**

Mode	TCS	TGATE	TSYNC
Timer	0	0	x
Gated Timer	0	1	x
Synchronous Counter	1	x	1
Asynchronous Counter	1	x	0

**FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM**



**REGISTER 16-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER<sup>(1)</sup>**

- bit 7-3      **FLTSRC<4:0>**: Fault Control Signal Source Select for PWM Generator # bits
- 11111 = Fault 32 (**default**)
  - 11110 = Reserved
  - .
  - .
  - .
  - 01100 = Reserved
  - 01011 = Comparator 4
  - 01010 = Op Amp/Comparator 3
  - 01001 = Op Amp/Comparator 2
  - 01000 = Op Amp/Comparator 1
  - 00111 = Reserved
  - 00110 = Reserved
  - 00101 = Reserved
  - 00100 = Reserved
  - 00011 = Fault 4
  - 00010 = Fault 3
  - 00001 = Fault 2
  - 00000 = Fault 1
- bit 2      **FLTPOL**: Fault Polarity for PWM Generator # bit<sup>(2)</sup>
- 1 = The selected Fault source is active-low
  - 0 = The selected Fault source is active-high
- bit 1-0      **FLTMOD<1:0>**: Fault Mode for PWM Generator # bits
- 11 = Fault input is disabled
  - 10 = Reserved
  - 01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (cycle)
  - 00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (latched condition)

- Note 1:** If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.
- 2:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

## 20.1 UART Helpful Tips

1. In multi-node, direct-connect UART networks, UART receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
  - a) If URXINV = 0, use a pull-up resistor on the RX pin.
  - b) If URXINV = 1, use a pull-down resistor on the RX pin.
2. The first character received on a wake-up from Sleep mode caused by activity on the UxRX pin of the UARTx module will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid; this is to be expected.

## 20.2 UART Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

### 20.2.1 KEY RESOURCES

- “UART” (DS70582) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

**REGISTER 21-4: CxFCTRL: ECANx FIFO CONTROL REGISTER**

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
DMABS2	DMABS1	DMABS0	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FSA4	FSA3	FSA2	FSA1	FSA0
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **DMABS<2:0>:** DMA Buffer Size bits

111 = Reserved

110 = 32 buffers in RAM

101 = 24 buffers in RAM

100 = 16 buffers in RAM

011 = 12 buffers in RAM

010 = 8 buffers in RAM

001 = 6 buffers in RAM

000 = 4 buffers in RAM

bit 12-5 **Unimplemented:** Read as '0'

bit 4-0 **FSA<4:0>:** FIFO Area Starts with Buffer bits

11111 = Read Buffer RB31

11110 = Read Buffer RB30

•

•

•

00001 = TX/RX Buffer TRB1

00000 = TX/RX Buffer TRB0

## 24.3 PTG Control Registers

### REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGEN	—	PTGSIDL	PTGTOGL	—	PTGSWT <sup>(2)</sup>	PTGSSEN <sup>(3)</sup>	PTGIVIS
bit 15							bit 8

R/W-0	HS-0	U-0	U-0	U-0	U-0	R/W-0	
PTGSTRT	PTGWDTO	—	—	—	—	PTGITM1 <sup>(1)</sup>	PTGITM0 <sup>(1)</sup>
bit 7							bit 0

<b>Legend:</b>	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15      **PTGEN:** Module Enable bit  
1 = PTG module is enabled  
0 = PTG module is disabled
- bit 14      **Unimplemented:** Read as '0'
- bit 13      **PTGSIDL:** PTG Stop in Idle Mode bit  
1 = Discontinues module operation when device enters Idle mode  
0 = Continues module operation in Idle mode
- bit 12      **PTGTOGL:** PTG TRIG Output Toggle Mode bit  
1 = Toggle state of the PTGOx for each execution of the PTGTRIG command  
0 = Each execution of the PTGTRIG command will generate a single PTGOx pulse determined by the value in the PTGPWDx bits
- bit 11      **Unimplemented:** Read as '0'
- bit 10      **PTGSWT:** PTG Software Trigger bit<sup>(2)</sup>  
1 = Triggers the PTG module  
0 = No action (clearing this bit will have no effect)
- bit 9      **PTGSSEN:** PTG Enable Single-Step bit<sup>(3)</sup>  
1 = Enables Single-Step mode  
0 = Disables Single-Step mode
- bit 8      **PTGIVIS:** PTG Counter/Timer Visibility Control bit  
1 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the current values of their corresponding counter/timer registers (PTGSD, PTGCx, PTGTx)  
0 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the value previously written to those limit registers
- bit 7      **PTGSTRT:** PTG Start Sequencer bit  
1 = Starts to sequentially execute commands (Continuous mode)  
0 = Stops executing commands
- bit 6      **PTGWDTO:** PTG Watchdog Timer Time-out Status bit  
1 = PTG Watchdog Timer has timed out  
0 = PTG Watchdog Timer has not timed out.
- bit 5-2      **Unimplemented:** Read as '0'

- Note 1:** These bits apply to the PTGWHI and PTGWLO commands only.
- Note 2:** This bit is only used with the PTGCTRL step command software trigger option.
- Note 3:** Use of the PTG Single-Step mode is reserved for debugging tools only.

### 25.1.2 OP AMP CONFIGURATION B

Figure 25-7 shows a typical inverting amplifier circuit with the output of the op amp (OAxOUT) externally routed to a separate analog input pin (ANy) on the device. This op amp configuration is slightly different in terms of the op amp output and the ADC input connection, therefore, RINT1 is not included in the transfer function. However, this configuration requires the designer to externally route the op amp output (OAxOUT) to another analog input pin (ANy). See Table 30-53 in **Section 30.0 “Electrical Characteristics”** for the typical value of RINT1. Table 30-60 and Table 30-61 in **Section 30.0 “Electrical Characteristics”** describe the minimum sample time (TSAMP) requirements for the ADC module in this configuration.

Figure 25-7 also defines the equation to be used to calculate the expected voltage at point VOAxOUT. This is the typical inverting amplifier equation.

## 25.2 Op Amp/Comparator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

### 25.2.1 KEY RESOURCES

- “Op Amp/Comparator” (DS70357) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools

**FIGURE 25-7: OP AMP CONFIGURATION B**

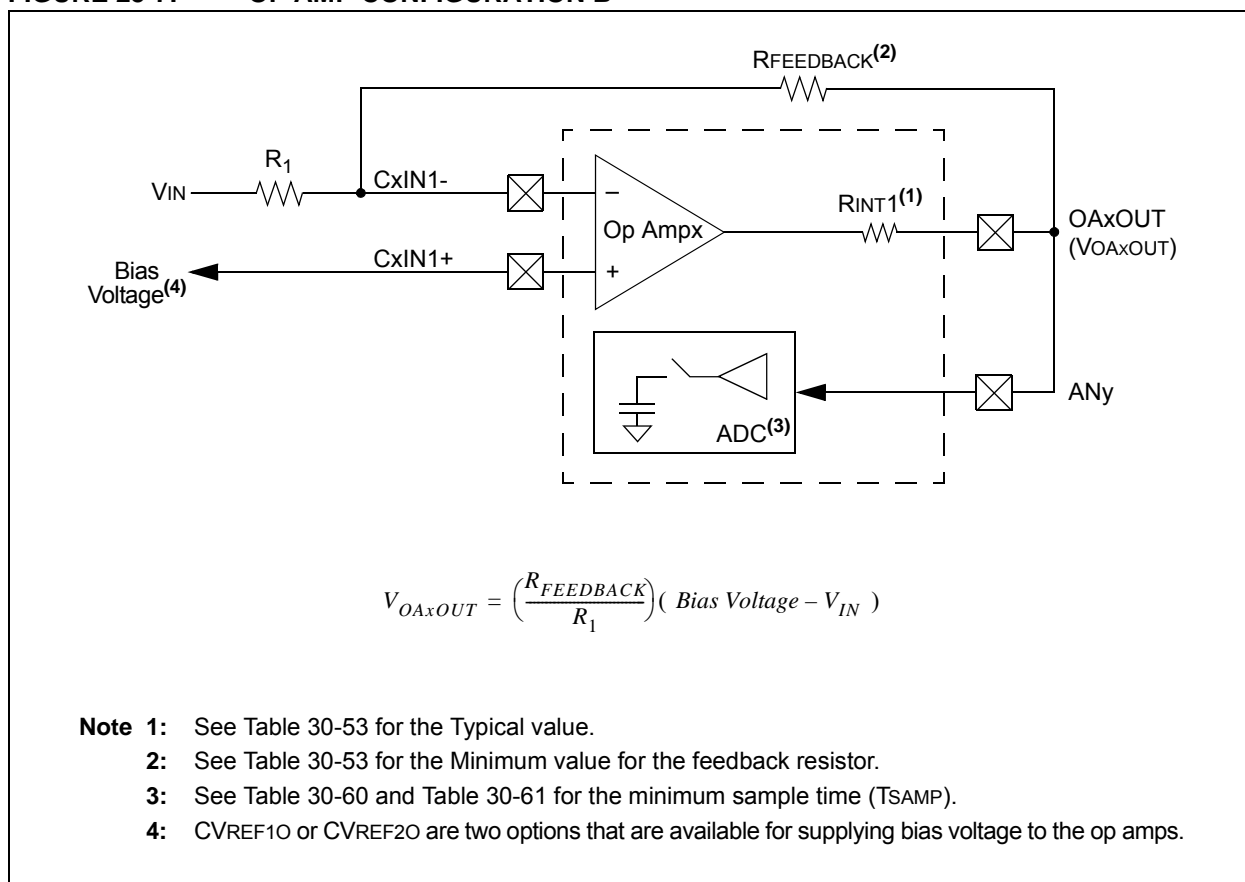


TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles <sup>(2)</sup>	Status Flags Affected
25	DAW	DAW Wn	Wn = decimal adjust Wn	1	1	C
26	DEC	DEC f	$f = f - 1$	1	1	C,DC,N,OV,Z
		DEC f, WREG	WREG = $f - 1$	1	1	C,DC,N,OV,Z
		DEC Ws, Wd	$Wd = Ws - 1$	1	1	C,DC,N,OV,Z
27	DEC2	DEC2 f	$f = f - 2$	1	1	C,DC,N,OV,Z
		DEC2 f, WREG	WREG = $f - 2$	1	1	C,DC,N,OV,Z
		DEC2 Ws, Wd	$Wd = Ws - 2$	1	1	C,DC,N,OV,Z
28	DISI	DISI #lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S Wm, Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD Wm, Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U Wm, Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD Wm, Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF Wm, Wn <sup>(1)</sup>	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO #lit15, Expr <sup>(1)</sup>	Do code to PC + Expr, lit15 + 1 times	2	2	None
		DO Wn, Expr <sup>(1)</sup>	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED Wm*Wm, Acc, Wx, Wy, Wxd <sup>(1)</sup>	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB,SA,SB,SAB
33	EDAC	EDAC Wm*Wm, Acc, Wx, Wy, Wxd <sup>(1)</sup>	Euclidean Distance	1	1	OA,OB,OAB,SA,SB,SAB
34	EXCH	EXCH Wns, Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL Ws, Wnd	Find Bit Change from Left (MSb) Side	1	1	C
36	FF1L	FF1L Ws, Wnd	Find First One from Left (MSb) Side	1	1	C
37	FF1R	FF1R Ws, Wnd	Find First One from Right (LSb) Side	1	1	C
38	GOTO	GOTO Expr	Go to address	2	4	None
		GOTO Wn	Go to indirect	1	4	None
		GOTO.L Wn	Go to indirect (long address)	1	4	None
39	INC	INC f	$f = f + 1$	1	1	C,DC,N,OV,Z
		INC f, WREG	WREG = $f + 1$	1	1	C,DC,N,OV,Z
		INC Ws, Wd	$Wd = Ws + 1$	1	1	C,DC,N,OV,Z
40	INC2	INC2 f	$f = f + 2$	1	1	C,DC,N,OV,Z
		INC2 f, WREG	WREG = $f + 2$	1	1	C,DC,N,OV,Z
		INC2 Ws, Wd	$Wd = Ws + 2$	1	1	C,DC,N,OV,Z
41	IOR	IOR f	$f = f . \text{IOR} . \text{WREG}$	1	1	N,Z
		IOR f, WREG	WREG = $f . \text{IOR} . \text{WREG}$	1	1	N,Z
		IOR #lit10, Wn	$Wd = \text{lit10} . \text{IOR} . Wd$	1	1	N,Z
		IOR Wb, Ws, Wd	$Wd = Wb . \text{IOR} . Ws$	1	1	N,Z
		IOR Wb, #lit5, Wd	$Wd = Wb . \text{IOR} . \text{lit5}$	1	1	N,Z
42	LAC	LAC Wso, #Slit4, Acc	Load Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
43	LNK	LNK #lit14	Link Frame Pointer	1	1	SFA
44	LSR	LSR f	$f = \text{Logical Right Shift } f$	1	1	C,N,OV,Z
		LSR f, WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR Ws, Wd	$Wd = \text{Logical Right Shift } Ws$	1	1	C,N,OV,Z
		LSR Wb, Wns, Wnd	$Wnd = \text{Logical Right Shift } Wb \text{ by } Wns$	1	1	N,Z
		LSR Wb, #lit5, Wnd	$Wnd = \text{Logical Right Shift } Wb \text{ by lit5}$	1	1	N,Z
45	MAC	MAC Wm*Wn, Acc, Wx, Wxd, Wy, Wyd, AWB <sup>(1)</sup>	Multiply and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
		MAC Wm*Wm, Acc, Wx, Wxd, Wy, Wyd <sup>(1)</sup>	Square and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB

**Note 1:** These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
<b>Operating Voltage</b>							
DC10	VDD	<b>Supply Voltage</b>	3.0	—	3.6	V	
DC16	VPOR	<b>VDD Start Voltage</b> to Ensure Internal Power-on Reset Signal	—	—	VSS	V	
DC17	SVDD	<b>VDD Rise Rate</b> to Ensure Internal Power-on Reset Signal	0.03	—	—	V/ms	0V-1V in 100 ms

**Note 1:** Device is functional at  $V_{BORMIN} < V_{DD} < V_{DDMIN}$ . Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

TABLE 30-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated): Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended							
Param No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Comments
	CEFC	External Filter Capacitor Value <sup>(1)</sup>	4.7	10	—	$\mu\text{F}$	Capacitor must have a low series resistance ( $< 1\ \Omega$ )

**Note 1:** Typical VCAP voltage = 1.8 volts when  $V_{DD} \geq V_{DDMIN}$ .



**TABLE 30-46: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)  
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—	—	Lesser of Fp or 11	MHz	(Note 3)
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1} \downarrow$ to SCK1 $\uparrow$ or SCK1 $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1} \uparrow$ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	Tsch2ssH, TscL2ssH	$\overline{SS1} \uparrow$ after SCK1 Edge	1.5 Tcy + 40	—	—	ns	(Note 4)
SP60	TssL2doV	SDO1 Data Output Valid after $\overline{SS1}$ Edge	—	—	50	ns	

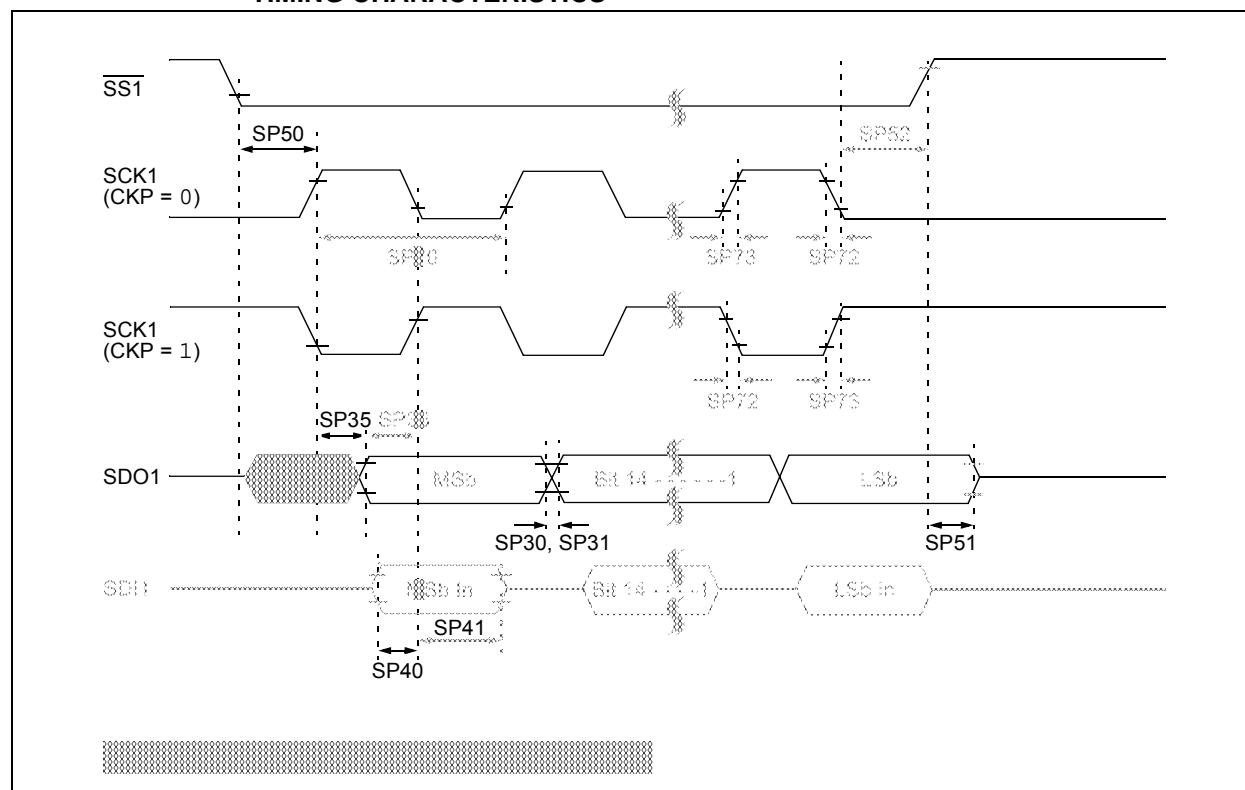
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

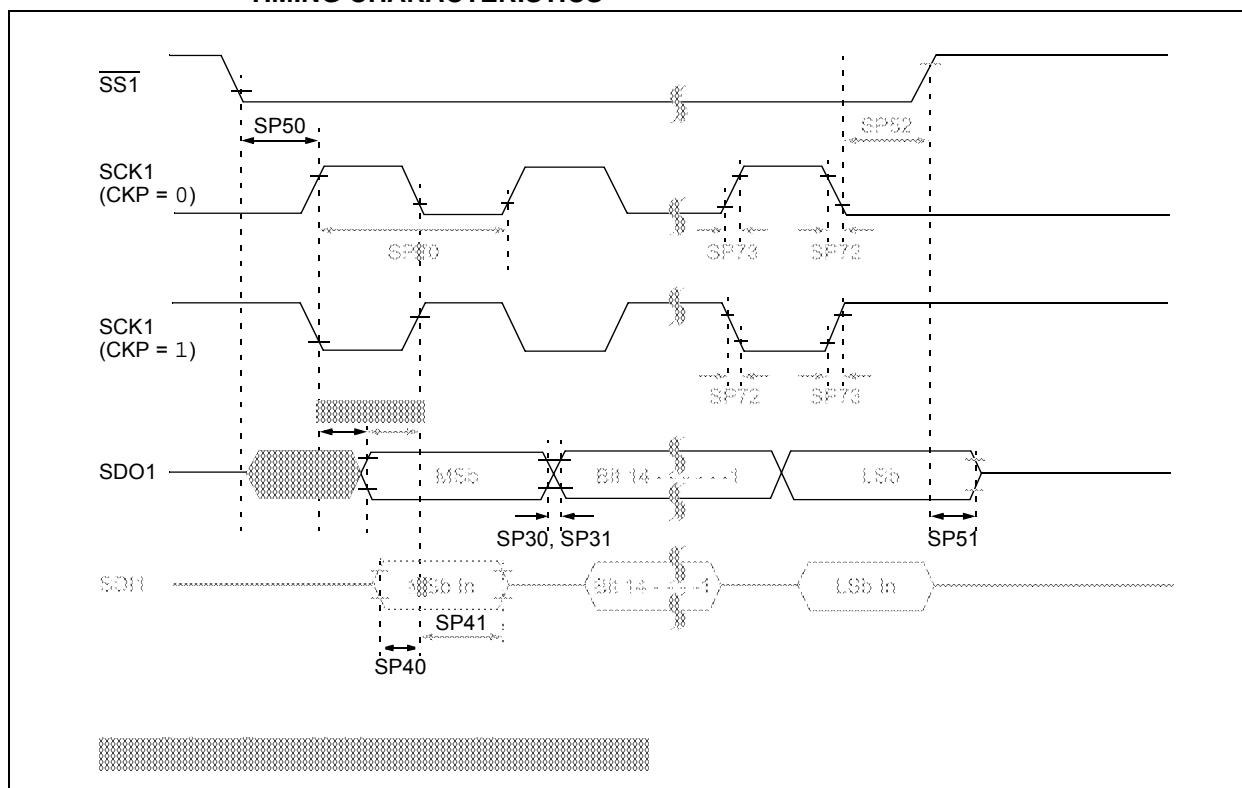
**3:** The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.

**FIGURE 30-28: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)**  
**TIMING CHARACTERISTICS**

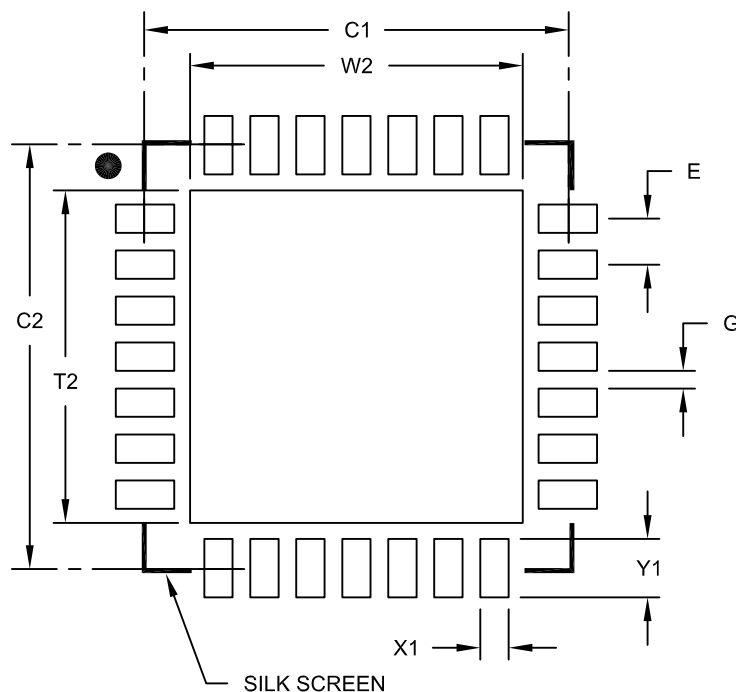


**FIGURE 30-29: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)  
TIMING CHARACTERISTICS**



**28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S]  
with 0.40 mm Contact Length**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



**RECOMMENDED LAND PATTERN**

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (X28)	Y1			0.85
Distance Between Pads	G	0.25		

**Notes:**

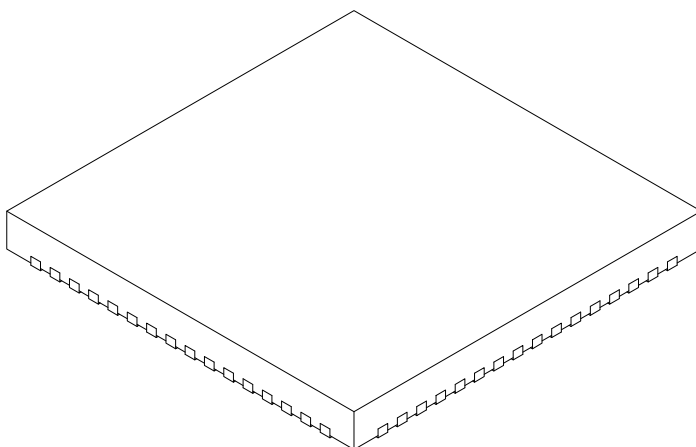
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A

**64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	64		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	9.00 BSC		
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D	9.00 BSC		
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2