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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc204-e-tl

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TABLE 4-19: SPI1 AND SPI2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	:	SPIBEC<2:0)>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI1CON1	0242	_	_	_	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	—	_	_	_	FRMDLY	SPIBEN	0000
SPI1BUF	0248							SPI1 Tra	ansmit and F	Receive Buf	fer Registe	r						0000
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	:	SPIBEC<2:0)>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI2CON1	0262	_	—		DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	—	_	_	_	FRMDLY	SPIBEN	0000
SPI2BUF	0268	8 SPI2 Transmit and Receive Buffer Register 00											0000					

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-53: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00		—	—			TRISA10	TRISA9	TRISA8	TRISA7			TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	079F
PORTA	0E02		—	_			RA10	RA9	RA8	RA7			RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04		—	—	-	-	LATA10	LATA9	LATA8	LATA7	_	-	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	_	_	_	_	_	ODCA10	ODCA9	ODCA8	ODCA7	_	_	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08		—	—			CNIEA10	CNIEA9	CNIEA8	CNIEA7			CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	_	_	_	_	_	CNPUA10	CNPUA9	CNPUA8	CNPUA7	_	_	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	_	_	_	_	_	CNPDA10	CNPDA9	CNPDA8	CNPDA7	_	_	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	_	_	_	_	_	_	_	_	_	_	_	ANSA4	_	_	ANSA1	ANSA0	0013

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-54: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	-	—	—	—	—	—	—	ANSB8	-	—	-	_	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-55: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	—	—	—	—	—	-	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	03FF
PORTC	0E22	—	_	—	—	—		RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	0E24	—	—	—	—	—		LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
ODCC	0E26	_	_	_	_	_	_	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000
CNENC	0E28	—	—	—	—	—	-	CNIEC9	CNIEC8	CNIEC7	CNIEC6	CNIEC5	CNIEC4	CNIEC3	CNIEC2	CNIEC1	CNIEC0	0000
CNPUC	0E2A	_	_	_	_	_	_	CNPUC9	CNPUC8	CNPUC7	CNPUC6	CNPUC5	CNPUC4	CNPUC3	CNPUC2	CNPUC1	CNPUC0	0000
CNPDC	0E2C	_	_	_	_	_	_	CNPDC9	CNPDC8	CNPDC7	CNPDC6	CNPDC5	CNPDC4	CNPDC3	CNPDC2	CNPDC1	CNPDC0	0000
ANSELC	0E2E	_	_	_	_	_	_	_		_		_	_	_	ANSC2	ANSC1	ANSC0	0007

Legend: x = unknown value on Reset, --- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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4.4.2 EXTENDED X DATA SPACE

The lower portion of the base address space range, between 0x0000 and 0x7FFF, is always accessible regardless of the contents of the Data Space Page registers. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x007FFF with the base address bit, EA<15> = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF, of base Data Space, in combination with DSRPAG = 0x000 or DSWPAG = 0x000. Consequently, DSRPAG and DSWPAG are initialized to 0x001 at Reset.

- Note 1: DSxPAG should not be used to access Page 0. An EDS access with DSxPAG set to 0x000 will generate an address error trap.
 - 2: Clearing the DSxPAG in software has no effect.

The remaining pages, including both EDS and PSV pages, are only accessible using the DSRPAG or DSWPAG registers in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where base address bit, EA<15> = 1.

For example, when DSRPAG = 0x001 or DSWPAG = 0x001, accesses to the upper 32 Kbytes, 0x8000 to 0xFFFF, of the Data Space will map to the EDS address range of 0x008000 to 0x00FFFF. When DSRPAG = 0x002 or DSWPAG = 0x002, accesses to the upper 32 Kbytes of the Data Space will map to the EDS address range of 0x010000 to 0x017FFF and so on, as shown in the EDS memory map in Figure 4-17.

For more information on the PSV page access using Data Space Page registers, refer to the "**Program Space Visibility from Data Space**" section in "**Program Memory**" (DS70613) of the "*dsPIC33/ PIC24 Family Reference Manual*".



FIGURE 4-17: EDS MEMORY MAP

4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- · Register Indirect
- · Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal
- Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

4.6.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

It is important to realize that the address boundaries check for addresses less than, or greater than, the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

Note: The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (such as [W7 + W2]) is used, Modulo Addressing correction is performed but the contents of the register remain unchanged.

4.7 Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

4.7.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled when all these conditions are met:

- BWMx bits (W register selection) in the MODCON register are any value other than '1111' (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is $M = 2^{N}$ bytes, the last 'N' bits of the data buffer start address must be zeros.

XBREV<14:0> is the Bit-Reversed Addressing modifier, or 'pivot point', which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

Note:	All bit-reversed EA calculations assume
	word-sized data (LSb of every EA is always
	clear). The XBREVx value is scaled
	accordingly to generate compatible (byte)
	addresses.

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It does not function for any other addressing mode or for byte-sized data and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XBREVx) and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

Note: Modulo Addressing and Bit-Reversed Addressing can be enabled simultaneously using the same W register, but Bit-Reversed Addressing operation will always take precedence for data writes when enabled.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer. In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receives a request to transfer data, a simple fixed priority scheme based on channel number, dictates which channel completes the transfer and which channel, or channels, are left pending. Each DMA channel moves a block of data, after which, it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA Controller provides these functional capabilities:

- Four DMA channels
- Register Indirect with Post-Increment Addressing mode
- Register Indirect without Post-Increment Addressing mode

- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU interrupt after half or full block transfer complete
- Byte or word transfers
- · Fixed priority channel arbitration
- Manual (software) or automatic (peripheral DMA requests) transfer initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two SRAM start addresses after each block transfer is complete)
- DMA request for each channel can be selected from any supported interrupt source
- Debug support features

The peripherals that can utilize DMA are listed in Table 8-1.

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
INT0 – External Interrupt 0	00000000	—	—
IC1 – Input Capture 1	0000001	0x0144 (IC1BUF)	—
IC2 – Input Capture 2	00000101	0x014C (IC2BUF)	_
IC3 – Input Capture 3	00100101	0x0154 (IC3BUF)	—
IC4 – Input Capture 4	00100110	0x015C (IC4BUF)	—
OC1 – Output Compare 1	00000010	_	0x0906 (OC1R) 0x0904 (OC1RS)
OC2 – Output Compare 2	00000110	_	0x0910 (OC2R) 0x090E (OC2RS)
OC3 – Output Compare 3	00011001	_	0x091A (OC3R) 0x0918 (OC3RS)
OC4 – Output Compare 4	00011010	_	0x0924 (OC4R) 0x0922 (OC4RS)
TMR2 – Timer2	00000111	—	—
TMR3 – Timer3	00001000	—	—
TMR4 – Timer4	00011011	_	—
TMR5 – Timer5	00011100	—	—
SPI1 Transfer Done	00001010	0x0248 (SPI1BUF)	0x0248 (SPI1BUF)
SPI2 Transfer Done	00100001	0x0268 (SPI2BUF)	0x0268 (SPI2BUF)
UART1RX – UART1 Receiver	00001011	0x0226 (U1RXREG)	—
UART1TX – UART1 Transmitter	00001100	—	0x0224 (U1TXREG)
UART2RX – UART2 Receiver	00011110	0x0236 (U2RXREG)	—
UART2TX – UART2 Transmitter	00011111	—	0x0234 (U2TXREG)
ECAN1 – RX Data Ready	00100010	0x0440 (C1RXD)	
ECAN1 – TX Data Request	01000110	—	0x0442 (C1TXD)
ADC1 – ADC1 Convert Done	00001101	0x0300 (ADC1BUF0)	_

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_		_	_		_	
bit 15			•				bit 8
U-0	U-0	U-0	U-0	R-1	R-1	R-1	R-1
—	—		_		LSTCI	H<3:0>	
bit 7		bit 0					
Legend:							
R = Readab	le bit	W = Writable	bit				
-n = Value a	It POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-4	Unimplemen	ted: Read as '	0'				
bit 3-0	LSTCH<3:0>	: Last DMAC C	hannel Active	e Status bits			
	1111 = No DI 1110 = Reser	MA transfer ha rved	s occurred sir	nce system Re	set		
	•						
	•						
	•						
	0100 = Reser 0011 = Last c 0010 = Last c 0001 = Last c	rved Jata transfer wa Jata transfer wa Jata transfer wa	as handled by as handled by as handled by	/ Channel 3 / Channel 2 / Channel 1			

REGISTER 8-13: DMALCA: DMA LAST CHANNEL ACTIVE STATUS REGISTER

0000 = Last data transfer was handled by Channel 0 0000 = Last data transfer was handled by Channel 0



FIGURE 13-3: TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)

3: Timery is a Type C timer (y = 3 and 5).

Timerx/y Resources 13.1

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
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	http://www.microchip.com/
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KEY RESOURCES 13.1.1

- "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- · Software Libraries
- · Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

BUFFER 21-5: ECAN™ MESSAGE BUFFER WORD 4

R = Readable bi	t ND	W = Writable b	it	U = Unimplen	nented bit, read ared	l as '0' x = Bit is unkr	
Legend:							
bit 7							bit 0
			Ву	rte 2			
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
bit 15							bit 8
			Ву	rte 3			
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x

bit 15-8 Byte 3<15:8>: ECAN Message Byte 3 bits

bit 7-0 Byte 2<7:0>: ECAN Message Byte 2 bits

BUFFER 21-6: ECAN™ MESSAGE BUFFER WORD 5

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Ву	/te 5			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Ву	/te 4			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimplen	nented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
-							

bit 15-8 Byte 5<15:8>: ECAN Message Byte 5 bits

bit 7-0 Byte 4<7:0>: ECAN Message Byte 4 bits

23.2 ADC Helpful Tips

- 1. The SMPIx control bits in the AD1CON2 register:
 - a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
 - b) When the CSCNA bit in the AD1CON2 registers is set to '1', this determines when the ADC analog scan channel list, defined in the AD1CSSL/AD1CSSH registers, starts over from the beginning.
 - c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
 - d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA.
- 2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMPIx bits and the condition described in 1c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
- 3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer (i.e., ADC1BUF0) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA Controller, before the next ADC conversion is complete to avoid overwriting the previous value.
- 4. The DONE bit (AD1CON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (AD1CON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.

5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for ANO, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUXA selections use AN0-AN2. Carefully study the ADC block diagram to determine the configuration that will best suit your application. Configuration examples are available in the "Analog-to-Digital Converter (ADC)" (DS70621) section in the "dsPIC33/ PIC24 Family Reference Manual".

23.3 ADC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

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	product page using the link above, enter
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23.3.1 KEY RESOURCES

- "Analog-to-Digital Converter (ADC)" (DS70621) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER^(1,2) (CONTINUED)

OC1CS: Clock Source for OC1 bit
 1 = Generates clock pulse when the broadcast command is executed 0 = Does not generate clock pulse when the broadcast command is executed
OC4TSS: Trigger/Synchronization Source for OC4 bit
 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
OC3TSS: Trigger/Synchronization Source for OC3 bit
 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
OC2TSS: Trigger/Synchronization Source for OC2 bit
 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
OC1TSS: Trigger/Synchronization Source for OC1 bit
 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed

- **Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).
 - 2: This register is only used with the PTGCTRL OPTION = 1111 Step command.

PTG Output Number	PTG Output Description
PTGO0	Trigger/Synchronization Source for OC1
PTGO1	Trigger/Synchronization Source for OC2
PTGO2	Trigger/Synchronization Source for OC3
PTGO3	Trigger/Synchronization Source for OC4
PTGO4	Clock Source for OC1
PTGO5	Clock Source for OC2
PTGO6	Clock Source for OC3
PTGO7	Clock Source for OC4
PTGO8	Trigger/Synchronization Source for IC1
PTGO9	Trigger/Synchronization Source for IC2
PTGO10	Trigger/Synchronization Source for IC3
PTGO11	Trigger/Synchronization Source for IC4
PTGO12	Sample Trigger for ADC
PTGO13	Sample Trigger for ADC
PTGO14	Sample Trigger for ADC
PTGO15	Sample Trigger for ADC
PTGO16	PWM Time Base Synchronous Source for PWM ⁽¹⁾
PTGO17	PWM Time Base Synchronous Source for PWM ⁽¹⁾
PTGO18	Mask Input Select for Op Amp/Comparator
PTGO19	Mask Input Select for Op Amp/Comparator
PTGO20	Reserved
PTGO21	Reserved
PTGO22	Reserved
PTGO23	Reserved
PTGO24	Reserved
PTGO25	Reserved
PTGO26	Reserved
PTGO27	Reserved
PTGO28	Reserved
PTGO29	Reserved
PTGO30	PTG Output to PPS Input Selection
PTGO31	PTG Output to PPS Input Selection

TABLE 24-2: PTG OUTPUT DESCRIPTIONS

Note 1: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0
_	CVR2OE ⁽¹⁾	—	—	—	VREFSEL	—	—
bit 15							bit 8
R/W-0) R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVRE	N CVR1OE ⁽¹⁾	CVRR	CVRSS ⁽²⁾	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0
Legend:							
R = Read	able bit	W = Writable	bit	U = Unimple	mented bit, read	i as '0'	
-n = Value	e at POR	'1' = Bit is set	t	'0' = Bit is cle	eared	x = Bit is unkr	Iown
bit 15	Unimplemen	ted: Read as '	0'		(1)		
bit 14	CVR2OE: Co	mparator Volta	ige Reference	2 Output Ena	ble bit ⁽¹⁾		
	1 = (AVDD - A 0 = (AVDD - A	AVSS)/2 is conr AVSS)/2 is disce	nected to the C	VREF20 pin the CVREF20	pin		
bit 13-11	Unimplemen	ted: Read as '	0'				
bit 10	VREFSEL: C	omparator Voli	tage Reference	e Select bit			
	1 = CVREFIN :	= VREF+	-				
	0 = CVREFIN i	s generated by	y the resistor n	etwork			
bit 9-8	Unimplemen	ted: Read as '	0'				
bit 7	CVREN: Con	nparator Voltag	je Reference E	nable bit			
	1 = Compara	tor voltage refe	erence circuit is	s powered on	wn		
bit 6	CVR1OF: Co	mparator Volta	age Reference	1 Output Ena	ble bit(1)		
bit o	1 = Voltage le	evel is output o	n the CVRFF10				
	0 = Voltage le	evel is disconne	ected from the	n CVREF10 pi	'n		
bit 5	CVRR: Comp	arator Voltage	Reference Ra	inge Selectior	n bit		
	1 = CVRSRC/2	24 step-size					
	0 = CVRSRC/3	32 step-size					
bit 4	CVRSS: Com	parator Voltag	e Reference S	ource Selecti	on bit ⁽²⁾		
	1 = Compara 0 = Compara	tor voltage refe tor voltage refe	erence source,	CVRSRC = (V CVRSRC = A)	(REF+) – (AVSS) /DD – AVSS		
bit 3-0	CVR<3:0> Co	omparator Volt	age Reference	Value Select	ion $0 \leq CVR < 3$:	0> ≤ 15 bits	
	When CVRR	= 1:					
	CVREFIN = (C	VR<3:0>/24) •	(CVRSRC)				
	When CVRR	= 0:					
	CVREFIN = (C	VRSRC/4) + (C	VR<3:0>/32) •	(CVRSRC)			
Note 1:	CVRxOE overrides	s the TRISx an	d the ANSELx	bit settinas.			

REGISTER 25-7: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

- 2: In order to operate with CVRSS = 1, at least one of the comparator modules must be enabled.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 26-3: CRCXORH: CRC XOR POLYNOMIAL HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			X<3	31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			X<2	3:16>			
bit 7							bit 0
Legend:							
R = Readable b	bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 X<31:16>: XOR of Polynomial Term Xⁿ Enable bits

REGISTER 26-4: CRCXORL: CRC XOR POLYNOMIAL LOW REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
X<15:8>										
bit 15 bit 8										
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0				
		X<7:1>				—				
						bit 0				
t	W = Writable	bit	U = Unimplen	nented bit, rea	id as '0'					
R	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown				
· · · · · · · · · · · · · · · · · · ·	R/W-0	R/W-0 R/W-0 t W = Writable 0R '1' = Bit is set	R/W-0 R/W-0 R/W-0 X<7:1> W = Writable bit 0R '1' = Bit is set	R/W-0 R/W-0 R/W-0 R/W-0 X<15:8> X<7:1> U U U U U U U U U U U U U U U U U U U U U U U U U U U U U U U U U U	R/W-0 R/W-0 R/W-0 R/W-0 X<15:8> X<7:1> U	R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 X<15:8> R/W-0 R/W-0 R/W-0 X<7:1> t W = Writable bit U = Unimplemented bit, read as '0' VR '1' = Bit is set '0' = Bit is cleared x = Bit is unkr				

bit 15-1X<15:1>: XOR of Polynomial Term Xⁿ Enable bitsbit 0Unimplemented: Read as '0'

DC CHARACTERISTICS			Standard (unless Operatin	d Operating otherwise g temperat	g Conditio stated) ure -40° -40°	ons: 3.0\ C ≤ Ta ≤ C ≤ Ta ≤	/ to 3.6V +85°C for Industrial +125°C for Extended
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
	lı∟	Input Leakage Current ^(1,2)					
DI50		I/O Pins 5V Tolerant ⁽³⁾	-1	—	+1	μA	$Vss \le VPIN \le VDD$, Pin at high-impedance
DI51		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	$\label{eq:VSS} \begin{split} &Vss \leq V \text{PIN} \leq V \text{DD}, \\ &\text{Pin at high-impedance}, \\ &-40^\circ\text{C} \leq \text{TA} \leq +85^\circ\text{C} \end{split}$
DI51a		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	Analog pins shared with external reference pins, $-40^{\circ}C \le TA \le +85^{\circ}C$
DI51b		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	$\label{eq:VSS} \begin{array}{l} VSS \leq VPIN \leq VDD, \\ Pin \text{ at high-impedance}, \\ -40^\circC \leq TA \leq +125^\circC \end{array}$
DI51c		I/O Pins Not 5V Tolerant ⁽³⁾	-1	_	+1	μA	Analog pins shared with external reference pins, $-40^{\circ}C \le TA \le +125^{\circ}C$
DI55		MCLR	-5	_	+5	μA	$Vss \leq V \text{PIN} \leq V \text{DD}$
DI56		OSC1	-5	_	+5	μA	$\label{eq:VSS} \begin{array}{l} VSS \leq VPIN \leq VDD, \\ XT \text{ and } HS \text{ modes} \end{array}$

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 2: Negative current is defined as current sourced by the pin.
- 3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 4: VIL source < (Vss 0.3). Characterized but not tested.
- **5:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.
- 6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

TABLE 30-18: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS				d Operat otherwis ng temper	ing Cond e stated) ature -4 -4	itions: 3 0°C ≤ TA 0°C ≤ TA	.0V to 3.6V A \leq +85°C for Industrial A \leq +125°C for Extended	
Param No.	Symbol	Characteristic	Min. Typ. ⁽¹⁾ Max. Units Conditions					
OS50	Fplli	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	_	8.0	MHz	ECPLL, XTPLL modes	
OS51	Fvco	On-Chip VCO System Frequency	120	_	340	MHz		
OS52	TLOCK	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	ms		
OS53	DCLK	CLKO Stability (Jitter) ⁽²⁾	-3	0.5	3	%		

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases, or communication clocks used by the application, use the following formula:

$$Effective Jitter = \frac{DCLK}{\sqrt{\frac{FOSC}{Time Base or Communication Clock}}}$$

For example, if Fosc = 120 MHz and the SPIx bit rate = 10 MHz, the effective jitter is as follows:

Effective Jitter =
$$\frac{DCLK}{\sqrt{\frac{120}{10}}} = \frac{DCLK}{\sqrt{12}} = \frac{DCLK}{3.464}$$

TABLE 30-19: INTERNAL FRC ACCURACY

АС СНА	RACTERISTICS	Standard Operatin	d Operatin g tempera	g Conditi ture -40° -40°	ons: 3.0V °C ≤ Ta ≤ · °C ≤ Ta ≤ ·	to 3.6V (unless otherw ⊦85°C for Industrial ⊦125°C for Extended	vise stated)
Param No. Characteristic Min. Typ. Max. Units Conditions							ons
Internal	FRC Accuracy @ FRC Fre	equency =	7.37 MHz	<u>(</u> 1)			
F20a	FRC	-1.5	0.5	+1.5	%	$-40^{\circ}C \le TA \le -10^{\circ}C$	VDD = 3.0-3.6V
		-1	0.5	+1	%	$-10^{\circ}C \leq TA \leq +85^{\circ}C$	VDD = 3.0-3.6V
F20b	FRC	-2	1	+2	%	$+85^{\circ}C \le TA \le +125^{\circ}C$	VDD = 3.0-3.6V

Note 1: Frequency is calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

TABLE 30-20: INTERNAL LPRC ACCURACY

AC CH	ARACTERISTICS	Standard Operating	Operating temperation	g Conditic ure -40° -40°	ons: 3.0V C ≤ TA ≤ + C ≤ TA ≤ +	to 3.6V (unless otherw 85°C for Industrial 125°C for Extended	ise stated)		
Param No.	Characteristic	Min.	Тур.	Max.	Units	Conditio	Conditions		
LPRC (@ 32.768 kHz ⁽¹⁾								
F21a	LPRC	-30		+30	%	$-40^\circ C \le T A \le -10^\circ C$	VDD = 3.0-3.6V		
		-20		+20	%	$-10^{\circ}C \le TA \le +85^{\circ}C$	VDD = 3.0-3.6V		
F21b	LPRC	-30		+30	%	$+85^{\circ}C \leq TA \leq +125^{\circ}C$	VDD = 3.0-3.6V		

Note 1: The change of LPRC frequency as VDD changes.

TABLE 30-37:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)TIMING REQUIREMENTS

АС СНА	ARACTERIS	Standard Op (unless othe Operating ter	erating erwise st mperatur	Conditio ated) re -40° -40°	ons: 3.0' C ≤ Ta ≤ C ≤ Ta ≤	V to 3.6V +85°C for Industrial +125°C for Extended	
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	-	—	Lesser of FP or 15	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	_	—	—	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	_	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	_	_	ns	(Note 4)
SP60	TssL2doV	SDO2 Data Output Valid after SS2 Edge	-	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

DC CHARACTERISTICS			Standard Op (unless other Operating ter	erating rwise st nperatu	Conditions: 3.0 $(ated)^{(1)}$ $e -40^{\circ}C \le TA$ $-40^{\circ}C \le TA$	0V to 3.0 ≤ +85°C ≤ +125°	5 V for Industrial C for Extended
Param No.	Symbol	Characteristic	Min.	Тур. ⁽²⁾	Max.	Units	Conditions
Op Am	p DC Chara	cteristics					
CM40	VCMR	Common-Mode Input Voltage Range	AVss	_	AVDD	V	
CM41	CMRR	Common-Mode Rejection Ratio ⁽³⁾	—	40		db	Vсм = AVdd/2
CM42	VOFFSET	Op Amp Offset Voltage ⁽³⁾	—	±5	—	mV	
CM43	Vgain	Open-Loop Voltage Gain ⁽³⁾	—	90	—	db	
CM44	los	Input Offset Current	—	_	_		See pad leakage currents in Table 30-11
CM45	Ів	Input Bias Current	—	—	_	_	See pad leakage currents in Table 30-11
CM46	Ιουτ	Output Current	—	_	420	μA	With minimum value of RFEEDBACK (CM48)
CM48	RFEEDBACK	Feedback Resistance Value	8	-	_	kΩ	
CM49a	VOADC	Output Voltage Measured at OAx Using ADC ^(3,4)	AVss + 0.077 AVss + 0.037 AVss + 0.018		AVDD – 0.077 AVDD – 0.037 AVDD – 0.018	V V V	Ιουτ = 420 μΑ Ιουτ = 200 μΑ Ιουτ = 100 μΑ
CM49b	Vout	Output Voltage Measured at OAxOUT Pin ^(3,4,5)	AVss + 0.210 AVss + 0.100 AVss + 0.050		AVDD - 0.210 AVDD - 0.100 AVDD - 0.050	V V V	Ιουτ = 420 μΑ Ιουτ = 200 μΑ Ιουτ = 100 μΑ
CM51	RINT1 ⁽⁶⁾	Internal Resistance 1 (Configuration A and B) ^(3,4,5)	198	264	317	Ω	Min = -40°C Typ = +25°C Max = +125°C

TABLE 30-53: OP AMP/COMPARATOR SPECIFICATIONS (CONTINUED)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

- 2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
- **3:** Parameter is characterized but not tested in manufacturing.
- 4: See Figure 25-6 for configuration information.
- 5: See Figure 25-7 for configuration information.
- 6: Resistances can vary by ±10% between op amps.

	30-37.									
AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽¹⁾ Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended							
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions			
Device Supply										
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or 3.0	—	Lesser of: VDD + 0.3 or 3.6	V				
AD02	AVss	Module Vss Supply	Vss – 0.3	_	Vss + 0.3	V				
	Reference Inputs									
AD05	Vrefh	Reference Voltage High	AVss + 2.5	—	AVdd	V	VREFH = VREF+ VREFL = VREF- (Note 1)			
AD05a			3.0	—	3.6	V	VREFH = AVDD VREFL = AVSS = 0			
AD06	VREFL	Reference Voltage Low	AVss	_	AVDD – 2.5	V	(Note 1) VREFH = AVDD VREFL = AVSS = 0			
AD06a	-		0	—	0	V				
AD07	Vref	Absolute Reference Voltage	2.5	—	3.6	V	VREF = VREFH - VREFL			
AD08	IREF	Current Drain	_	_	10 600	μΑ μΑ	ADC off ADC on			
AD09	IAD	AD Operating Current ⁽²⁾ — 5		—	mA	ADC operating in 10-bit mode (Note 1)				
			—	2	—	mA	ADC operating in 12-bit mode (Note 1)			
Analog Input										
AD12	Vinh	Input Voltage Range Vinн	VINL	_	Vrefh	V	This voltage reflects Sample-and- Hold Channels 0, 1, 2 and 3 (CH0-CH3), positive input			
AD13	VINL	Input Voltage Range VINL	VREFL		AVss + 1V	V	This voltage reflects Sample-and- Hold Channels 0, 1, 2 and 3 (CH0-CH3), negative input			
AD17	Rin	Recommended Impedance of Analog Voltage Source	_		200	Ω	Impedance to achieve maximum performance of ADC			

TABLE 30-57: ADC MODULE SPECIFICATIONS

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: Parameter is characterized but not tested in manufacturing.

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS				
Dimensior	ı Limits	MIN	NOM	MAX	
Contact Pitch	E		0.50 BSC		
Contact Pad Spacing	C1		11.40		
Contact Pad Spacing	C2		11.40		
Contact Pad Width (X64)	X1			0.30	
Contact Pad Length (X64)	Y1			1.50	
Distance Between Pads	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B