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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc204-i-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### Pin Diagrams (Continued)



### **Pin Diagrams (Continued)**









### EXAMPLE 4-2: EXTENDED DATA SPACE (EDS) WRITE ADDRESS GENERATION

The paged memory scheme provides access to multiple 32-Kbyte windows in the EDS and PSV memory. The Data Space Page registers, DSxPAG, in combination with the upper half of the Data Space address, can provide up to 16 Mbytes of additional address space in the EDS and 8 Mbytes (DSRPAG only) of PSV address space. The paged data memory space is shown in Example 4-3.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG. Writes to PS are not supported, so DSWPAG is dedicated to DS, including EDS only. The Data Space and EDS can be read from, and written to, using DSRPAG and DSWPAG, respectively.

### 4.4.4 SOFTWARE STACK

The W15 register serves as a dedicated Software Stack Pointer (SSP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating of the Stack Pointer (for example, creating stack frames).

Note:	То	protec	t	agains	st	misal	lign	ed	st	ack
	acc	esses,	W	15<0>	is	fixed	to	'0'	by	the
	hard	dware.								

W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within Data Space.

The Software Stack Pointer always points to the first available free word and fills the software stack working from lower toward higher addresses. Figure 4-19 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> are pushed onto the first available stack word, then PC<22:16> are pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-19. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

- **Note 1:** To maintain system Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging, and is therefore restricted to an address range of 0x0000 to 0xFFFF. The same applies to the W14 when used as a Stack Frame Pointer (SFA = 1).
  - 2: As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a C development environment

FIGURE 4-19: CALL STACK FRAME



### 5.2 RTSP Operation

RTSP allows the user application to erase a single page of memory and to program two instruction words at a time. See the General Purpose and Motor Control Family tables (Table 1 and Table 2, respectively) for the page sizes of each device.

For more information on erasing and programming Flash memory, refer to "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual".

### 5.3 **Programming Operations**

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

For erase and program times, refer to Parameters D137a and D137b (Page Erase Time), and D138a and D138b (Word Write Cycle Time) in Table 30-14 in **Section 30.0 "Electrical Characteristics"**.

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

### 5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of program Flash memory at a time on every other word address boundary (0x000002, 0x000006, 0x00000A, etc.). To do this, it is necessary to erase the page that contains the desired address of the location the user wants to change.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPS.

Refer to **Flash Programming**" (DS70609) in the "*dsPIC33/PIC24 Family Reference Manual*" for details and codes examples on programming using RTSP.

### 5.4 Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

### 5.4.1 KEY RESOURCES

- "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

### 5.5 Control Registers

Four SFRs are used to erase and write the program Flash memory: NVMCON, NVMKEY, NVMADRH and NVMADRL.

The NVMCON register (Register 5-1) enables and initiates Flash memory erase and write operations.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRH and NVMADRL. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word for programming operations or the selected page for erase operations.

The NVMADRH register is used to hold the upper 8 bits of the EA, while the NVMADRL register is used to hold the lower 16 bits of the EA.

# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 7-5	INTCON3 INTERRUPT CONTROL REGISTER 3	

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	—	DAE	DOOVR	—	—	—	—
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value at I	POR	'1' = Bit is set	:	'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-6	Unimplemen	ted: Read as	'0'				
bit 5	bit 5 DAE: DMA Address Error Soft Trap Status bit						
1 = DMA address error soft trap has occurred							
0 = DMA address error soft trap has not occurred							
bit 4	DOOVR: DO	Stack Overflow	/ Soft Trap Stat	tus bit			
	1 = DO stack overflow soft trap has occurred						

	0 = DO stack overflow soft trap has not occurred
~ ~	

### REGISTER 7-6: INTCON4: INTERRUPT CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	_
bit 15			•		•		bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SGHT
bit 7			•		•		bit 0
Legend:							

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 0

SGHT: Software Generated Hard Trap Status bit

1 = Software generated hard trap has occurred

0 = Software generated hard trap has not occurred

### 11.4.4.2 Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6-bit fields, with each set associated with one RPn pin (see Register 11-18 through Register 11-27). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-3 and Figure 11-3).

A null output is associated with the output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

### FIGURE 11-3: MULTIPLEXING REMAPPABLE OUTPUT FOR RPn



### 11.4.4.3 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings across any or all of the RPn pins is possible. This includes both many-toone and one-to-many mappings of peripheral inputs and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

### TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPxR<5:0>	Output Name
Default PORT	000000	RPn tied to Default Pin
U1TX	000001	RPn tied to UART1 Transmit
U2TX	000011	RPn tied to UART2 Transmit
SDO2	001000	RPn tied to SPI2 Data Output
SCK2	001001	RPn tied to SPI2 Clock Output
SS2	001010	RPn tied to SPI2 Slave Select
C1TX <sup>(2)</sup>	001110	RPn tied to CAN1 Transmit
OC1	010000	RPn tied to Output Compare 1 Output
OC2	010001	RPn tied to Output Compare 2 Output
OC3	010010	RPn tied to Output Compare 3 Output
OC4	010011	RPn tied to Output Compare 4 Output
C1OUT	011000	RPn tied to Comparator Output 1
C2OUT	011001	RPn tied to Comparator Output 2
C3OUT	011010	RPn tied to Comparator Output 3
SYNCO1 <sup>(1)</sup>	101101	RPn tied to PWM Primary Time Base Sync Output
QEI1CCMP <sup>(1)</sup>	101111	RPn tied to QEI 1 Counter Comparator Output
REFCLKO	110001	RPn tied to Reference Clock Output
C4OUT	110010	RPn tied to Comparator Output 4

Note 1: This function is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This function is available in dsPIC33EPXXXGP/MC50X devices only.



#### **FIGURE 13-3:** TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)

3: Timery is a Type C timer (y = 3 and 5).

#### **Timerx/y Resources** 13.1

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/
	wwwproducts/Devices.aspx?d
	DocName=en555464

#### **KEY RESOURCES** 13.1.1

- "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- · Software Libraries
- · Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

# REGISTER 16-13: IOCONX: PWMx I/O CONTROL REGISTER<sup>(2)</sup> (CONTINUED)

- bit 1 SWAP: SWAP PWMxH and PWMxL Pins bit
   1 = PWMxH output signal is connected to PWMxL pins; PWMxL output signal is connected to PWMxH pins
   0 = PWMxH and PWMxL pins are mapped to their respective pins
   bit 0 OSYNC: Output Override Synchronization bit
   1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWMx period boundary
  - 0 = Output overrides via the OVDDAT<1:0> bits occur on the next CPU clock boundary
- Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).
  - 2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

NOTES:

### REGISTER 17-1: QEI1CON: QEI1 CONTROL REGISTER (CONTINUED)

bit 6-4	<b>INTDIV&lt;2:0&gt;:</b> Timer Input Clock Prescale Select bits (interval timer, main timer (position counter), velocity counter and index counter internal clock divider select) <sup>(3)</sup>								
	<pre>111 = 1:128 prescale value 110 = 1:64 prescale value 101 = 1:32 prescale value 100 = 1:16 prescale value 011 = 1:8 prescale value 010 = 1:4 prescale value 001 = 1:2 prescale value 000 = 1:1 prescale value</pre>								
bit 3	<b>CNTPOL:</b> Position and Index Counter/Timer Direction Select bit								
	<ul> <li>0 = Counter direction is positive unless modified by external up/down signal</li> </ul>								
bit 2	GATEN: External Count Gate Enable bit								
	<ul> <li>1 = External gate signal controls position counter operation</li> <li>0 = External gate signal does not affect position counter/timer operation</li> </ul>								
bit 1-0	CCM<1:0>: Counter Control Mode Selection bits								
	<ul> <li>11 = Internal Timer mode with optional external count is selected</li> <li>10 = External clock count with optional external count is selected</li> <li>01 = External clock count with external up/down direction is selected</li> <li>00 = Quadrature Encoder Interface (x4 mode) Count mode is selected</li> </ul>								
Note 1:	When CCM<1:0> = 10 or 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.								

- 2: When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.
- 3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

# 19.0 INTER-INTEGRATED CIRCUIT<sup>™</sup> (I<sup>2</sup>C<sup>™</sup>)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Inter-Integrated Circuit™ (I<sup>2</sup>C™)" (DS70330) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.
  - 3: There are minimum bit rates of approximately FCY/512. As a result, high processor speeds may not support 100 Kbit/second operation. See timing specifications, IM10 and IM11, and the "Baud Rate Generator" in the "dsPIC33/PIC24 Family Reference Manual".

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X family of devices contains two Inter-Integrated Circuit (I<sup>2</sup>C) modules: I2C1 and I2C2.

The  $l^2C$  module provides complete hardware support for both Slave and Multi-Master modes of the  $l^2C$  serial communication standard, with a 16-bit interface.

The  $I^2C$  module has a 2-pin interface:

- · The SCLx pin is clock
- The SDAx pin is data

The I<sup>2</sup>C module offers the following key features:

- I<sup>2</sup>C interface supporting both Master and Slave modes of operation
- I<sup>2</sup>C Slave mode supports 7 and 10-bit addressing
- I<sup>2</sup>C Master mode supports 7 and 10-bit addressing
- I<sup>2</sup>C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for I<sup>2</sup>C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I<sup>2</sup>C supports multi-master operation, detects bus collision and arbitrates accordingly
- Intelligent Platform Management Interface (IPMI)
   support
- System Management Bus (SMBus) support

### 29.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

### 29.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

### 29.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a highspeed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

## 29.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a fullspeed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming<sup>™</sup> (ICSP<sup>™</sup>).

### 29.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

DC CH4	ARACTER	$\begin{tabular}{ l l l l l l l l l l l l l l l l l l l$							
Param No.	Symbol	Characteristic	Min. Typ. Max. Units Conditions						
Operating Voltage									
DC10	Vdd	Supply Voltage	3.0	_	3.6	V			
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	_	_	Vss	V			
DC17	Svdd	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.03	—	—	V/ms	0V-1V in 100 ms		

### TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

### TABLE 30-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated):Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended									
Param No.	Param No.SymbolCharacteristicsMin.Typ.Max.UnitsComments								
	Cefc	External Filter Capacitor Value <sup>(1)</sup>	4.7	10	_	μF	Capacitor must have a low series resistance (< 1 Ohm)		

**Note 1:** Typical VCAP voltage = 1.8 volts when VDD  $\geq$  VDDMIN.

# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X



TADLE 30-23. THVIER I EATERINAL CLOCK THVIING REQUIREIVIEN 13	TABLE 30-23:	TIMER1 EXTERNAL	<b>CLOCK TIMING</b>	<b>REQUIREMENTS</b> <sup>(1)</sup>
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AC CHARACTERISTICS				$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Charao	cteristic <sup>(2)</sup>	Min.	Тур.	Max.	Units	Conditions	
TA10	A10 TTXH T1C Tim		Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	—	ns	Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256)	
			Asynchronous	35	—	—	ns		
TA11	ΤτxL	T1CK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256)	
			Asynchronous	10	—	—	ns		
TA15	ΤτχΡ	T1CK Input Synchronous Period mode		Greater of: 40 or (2 Tcy + 40)/N	_		ns	N = prescale value (1, 8, 64, 256)	
OS60	Ft1	T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>))		DC		50	kHz		
TA20	TCKEXTMRL	Delay from External T1CK Clock Edge to Timer Increment		0.75 Tcy + 40		1.75 Tcy + 40	ns		

Note 1: Timer1 is a Type A.

2: These parameters are characterized, but are not tested in manufacturing.



### FIGURE 30-27: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

# TABLE 30-48:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)TIMING REQUIREMENTS

АС СНА	ARACTERIS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Тур. <sup>(2)</sup>	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency		_	11	MHz	(Note 3)
SP72	TscF	SCK1 Input Fall Time	_		_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time			_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	_	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	Ι	—	ns	
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	TscH2ssH, TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 Tcy + 40	—	_	ns	(Note 4)

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

	30-37.									
АС СН	ARACTE	RISTICS	$ \begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)}^{(1)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array} $							
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Conditions				
Device Supply										
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or 3.0	—	Lesser of: VDD + 0.3 or 3.6	V				
AD02	AVss	Module Vss Supply	Vss – 0.3	_	Vss + 0.3	V				
		·	Refer	ence In	puts					
AD05	Vrefh	Reference Voltage High	AVss + 2.5	—	AVdd	V	VREFH = VREF+ VREFL = VREF- <b>(Note 1)</b>			
AD05a			3.0	—	3.6	V	VREFH = AVDD VREFL = AVSS = 0			
AD06	VREFL	Reference Voltage Low	AVss	_	AVDD – 2.5	V	(Note 1)			
AD06a	-		0	—	0	V	VREFH = AVDD VREFL = AVSS = 0			
AD07	Vref	Absolute Reference Voltage	2.5	—	3.6	V	VREF = VREFH - VREFL			
AD08	IREF	Current Drain	_	_	10 600	μΑ μΑ	ADC off ADC on			
AD09	IAD	Operating Current <sup>(2)</sup>	—	5	—	mA	ADC operating in 10-bit mode (Note 1)			
			—	2	—	mA	ADC operating in 12-bit mode (Note 1)			
			Ana	log Inp	out	•				
AD12	Vinh	Input Voltage Range Vinн	VINL	_	Vrefh	V	This voltage reflects Sample-and- Hold Channels 0, 1, 2 and 3 (CH0-CH3), positive input			
AD13	VINL	Input Voltage Range VINL	VREFL		AVss + 1V	V	This voltage reflects Sample-and- Hold Channels 0, 1, 2 and 3 (CH0-CH3), negative input			
AD17	Rin	Recommended Impedance of Analog Voltage Source	_		200	Ω	Impedance to achieve maximum performance of ADC			

### TABLE 30-57: ADC MODULE SPECIFICATIONS

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: Parameter is characterized but not tested in manufacturing.

### 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	MILLIMETERS						
Dimension	l Limits	MIN	NOM	MAX			
Number of Pins	N		28				
Pitch	е		1.27 BSC				
Overall Height	Α	-	-	2.65			
Molded Package Thickness	A2	2.05	-	-			
Standoff §	A1	0.10	-	0.30			
Overall Width	E		10.30 BSC				
Molded Package Width	E1	7.50 BSC					
Overall Length	D		17.90 BSC				
Chamfer (Optional)	h	0.25	-	0.75			
Foot Length	L	0.40	-	1.27			
Footprint	L1	1.40 REF					
Lead Angle	Θ	0°	-	-			
Foot Angle	φ	0°	-	8°			
Lead Thickness	С	0.18	-	0.33			
Lead Width	b	0.31	-	0.51			
Mold Draft Angle Top	-	15°					
Mold Draft Angle Bottom	If Angle Bottom $\beta$ 5° - 1						

### Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2