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Product Status	Active
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Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
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TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	-	—	_	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—		—	_	_	_		IC4IF	IC3IF	DMA3IF	_	—	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—		—	—	_	_		—	—	_	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	_	_	CTMUIF		_	_	_	_		—	_	—	CRCIF	U2EIF	U1EIF	_	0000
IFS8	0810	JTAGIF	ICDIF	—	_	—	—	—	—	_	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	_	—	—	—	—	_	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	_	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	_	—	—	—	—	_	IC4IE	IC3IE	DMA3IE	—	—	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	_	—	—	—	—		—	_	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	_	—	—	—	—	_	—	—	—	CRCIE	U2EIE	U1EIE	—	0000
IEC8	0830	JTAGIE	ICDIE	—	_	—	—	—	—		—	_	—	—	—	—	—	0000
IEC9	0832	—	—	—	_	—	—	—	_	_	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	—	0000
IPC0	0840	—		T1IP<2:0>		—	- OC1IP<2:0>)>	_	IC1IP<2:0>		—		INT0IP<2:0>		4444	
IPC1	0842	—		T2IP<2:0>		—		OC2IP<2:0)>	— IC2IP<2:0>		—	0	0MA0IP<2:0>		4444		
IPC2	0844	—	ι	J1RXIP<2:0	>	—	:	SPI1IP<2:0)>	_	SPI1EIP<2:0>		—		T3IP<2:0>		4444	
IPC3	0846	—	—	—	—	—	DMA1IP<2:0>		0>		AD1IP<2:0>		—	ι	J1TXIP<2:0>		0444	
IPC4	0848	—		CNIP<2:0>		—		CMIP<2:0	>	_	MI2C1IP<2:0>		>	—	5	SI2C1IP<2:0>		4444
IPC5	084A	—	—	—	_	—	—	—	—	_	—	—	—	—		INT1IP<2:0>		0004
IPC6	084C	—		T4IP<2:0>		—		OC4IP<2:0)>	_		OC3IP<2:0>	•	—	DMA2IP<2:0>		4444	
IPC7	084E	—	l	J2TXIP<2:0	>	—	ι	J2RXIP<2:	0>	_		INT2IP<2:0>	>	—	T5IP<2:0>		4444	
IPC8	0850	—	—	—	_	—	—	—	—	_		SPI2IP<2:0>	>	—	S	SPI2EIP<2:0>		0044
IPC9	0852	—	—	—	_	—		IC4IP<2:0	>	_		IC3IP<2:0>		—	0	0MA3IP<2:0>		0444
IPC12	0858	—	—	—	_	—	N	112C2IP<2:	0>	_		SI2C2IP<2:0	>	—	—	—	—	0440
IPC16	0860	—		CRCIP<2:0	>	—		U2EIP<2:0	>	_		U1EIP<2:0>		—	—	—	—	4440
IPC19	0866	—	—	—	_	—	—	—	—	_		CTMUIP<2:0	>	—	—	—	—	0040
IPC35	0886	—		JTAGIP<2:0	>	—		ICDIP<2:0	>	_	—	—	—	—	—	—	—	4400
IPC36	0888	—	F	PTG0IP<2:0	>	—	PT	GWDTIP<	2:0>	_	P	TGSTEPIP<2	2:0>	—	—	—	—	4440
IPC37	088A	—	—	—		—	F	PTG3IP<2:	0>			PTG2IP<2:0	>	—	F	PTG1IP<2:0>		0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	_	—	—	—	—	_	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	_	—	_	—	—	_	—	_	_	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	_	—	—	_	—	_	—	—	_	—	DAE	DOOVR	—	_	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	_	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	_	_	_	—		ILR<	3:0>					VECN	JM<7:0>				0000

- = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 3	SLEEP: Wake-up from Sleep Flag bit 1 = Device has been in Sleep mode 0 = Device has not been in Sleep mode
bit 2	IDLE: Wake-up from Idle Flag bit
	1 = Device was in Idle mode0 = Device was not in Idle mode
bit 1	BOR: Brown-out Reset Flag bit 1 = A Brown-out Reset has occurred 0 = A Brown-out Reset has not occurred
bit 0	POR: Power-on Reset Flag bit 1 = A Power-on Reset has occurred 0 = A Power-on Reset has not occurred

- **Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
 - 2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

7.0 INTERRUPT CONTROLLER

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP/MC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Interrupts" (DS70600) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X CPU.

The interrupt controller has the following features:

- Up to eight processor exceptions and software traps
- Eight user-selectable priority levels
- Interrupt Vector Table (IVT) with a unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X Interrupt Vector Table (IVT), shown in Figure 7-1, resides in program memory starting at location, 000004h. The IVT contains seven non-maskable trap vectors and up to 246 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit-wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

NOTES:

REGISTER 11-9: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				HOME1R<6:0	>		
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				INDX1R<6:0>	>		
bit 7							bit 0
Legend:							
R = Readab	ole bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	Unimpleme	ented: Read as '	0'				
bit 15 bit 14-8	HOME1R<6	5:0>: Assign QEI	0 1 HOME1 (H selection nun	OME1) to the C	Corresponding	RPn Pin bits	
	1111001 =	Input tied to RPI	121	,			
		Input tied to CM	D1				
	0000000 =	Input tied to Vss	;				
bit 7	Unimpleme	ented: Read as '	0'				
bit 6-0	IND1XR<6: (see Table 2	0>: Assign QEI1 I1-2 for input pin	INDEX1 (INE selection nun	0X1) to the Cor nbers)	responding R	Pn Pin bits	
	1111001 =	Input tied to RPI	121	,			
	•						
	0000001 =	Input tied to CM	P1				
	0000000 =	Input tied to Vss					

15.2 Output Compare Control Registers

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
		OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	_	ENFLTB
bit 15							bit 8
R/W-0	U-0	R/W-0, HSC	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0
ENFLTA		OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0
bit 7							bit 0
Legend:		HSC = Hardw	are Settable/Cl	earable bit			
R = Reada	ible bit	W = Writable I	bit	U = Unimplem	nented bit, read	as '0'	
-n = Value	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-14	Unimplemen	ted: Read as '0)'				
bit 13	OCSIDL: Out	tput Compare x	Stop in Idle Mo	de Control bit			
	1 = Output C	compare x Halts	in CPU Idle me	ode via CDU Idia m	odo		
bit 12 10			nues lo operale		oue		
DIL 12-10	111 = Perinh	eral clock (Ep)	pare x Clock S				
	110 = Reserv	/ed					
	101 = PTGO	x clock ⁽²⁾					
	100 = T1CLK	is the clock so	urce of the OC	k (only the sync	hronous clock	is supported)	
	011 = 15CLK	is the clock sou	urce of the OC	х ~			
	001 = T3CLK	is the clock so	urce of the OC	x X			
	000 = T2CLK	is the clock so	urce of the OC	ĸ			
bit 9	Unimplemen	ted: Read as '0)'				
bit 8	ENFLTB: Fau	ult B Input Enab	le bit				
	1 = Output C 0 = Output C	compare Fault B compare Fault B	input (OCFB) input (OCFB)	is enabled is disabled			
bit 7	ENFLTA: Fau	ult A Input Enabl	le bit				
	1 = Output C	ompare Fault A	input (OCFA)	is enabled			
	0 = Output C	ompare Fault A	input (OCFA)	is disabled			
bit 6	Unimplemen	ted: Read as '0)'				
bit 5	OCFLTB: PW	M Fault B Cond	dition Status bit				
	1 = PWM Fa 0 = No PWM	ult B condition of Fault B condition	on OCFB pin ha on on OCFB pi	as occurred n has occurred			
bit 4	OCFLTA: PW	/M Fault A Cond	dition Status bit				
	1 = PWM Fa	ult A condition of	on OCFA pin ha	as occurred			
	0 = No PWM	I Fault A condition	on on OCFA pi	n has occurred			
Note 1:	OCxR and OCxF	RS are double-b	ouffered in PWN	A mode only.			
2:	Each Output Cor	mpare x module	(OCx) has one	PTG clock sou	urce. See Secti	on 24.0 "Perip	oheral Trigger
	Generator (PTG PTGO4 = OC1) wodule" for r	nore informatio	n.			
	PTGO5 = OC2						
	PTGO6 = OC3						
	PTGO7 = OC4						

·							
R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PENH	PENL	POLH	POLL	PMOD1 ⁽¹⁾	PMOD0 ⁽¹⁾	OVRENH	OVRENL
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15	PENH: PWM	(H Output Pin (Ownership bit				
	1 = PWMx mc	dule controls I	PWMxH pin WMx⊟ pin				
hit 11							
DIL 14	1 = DM/Mx mc	adula controla l					
	1 = PWWX IIIC 0 = GPIO mod	dule controls P	WMxL pin				
hit 13		H Output Pin I	Polarity bit				
	1 = PWMxH r	in is active-low	/				
	0 = PWMxH p	oin is active-hig	h				
bit 12	POLL: PWMx	L Output Pin F	olarity bit				
	1 = PWMxL p	in is active-low	,				
	0 = PWMxL p	in is active-hig	h				
bit 11-10	PMOD<1:0>:	PWMx # I/O P	in Mode bits ⁽¹)			
	11 = Reserve	d; do not use					
	10 = PWMx I/	O pin pair is in	the Push-Pul	I Output mode			
	01 = PWWx I/ 00 = PWMx I/	O pin pair is in O pin pair is in	the Complem	nt Output mod entary Output	mode		
hit 9	OVRENH: Ov	erride Enable i	for PWMxH P	in bit	mouo		
bit o	1 = OVRDAT	<1> controls or	itput on PWM	xH nin			
	0 = PWMx ge	nerator control	s PWMxH pin				
bit 8	OVRENL: Ov	erride Enable f	or PWMxL Pi	n bit			
	1 = OVRDAT	<0> controls ou	Itput on PWM	xL pin			
	0 = PWMx ge	nerator control	s PWMxL pin				
bit 7-6	OVRDAT<1:0	>: Data for PW	/MxH, PWMxl	L Pins if Overr	ide is Enabled b	its	
	If OVERENH	= 1, PWMxH is	s driven to the	state specifie	d by OVRDAT<	1>.	
	If OVERENL :	= 1, PWMxL is	driven to the	state specified	l by OVRDAT<0	>.	
bit 5-4	FLTDAT<1:0>	Data for PW	MxH and PWI	MxL Pins if FL	TMOD is Enable	ed bits	
	If Fault is activ	ve, PWMxH is	driven to the s	state specified	by FLTDAT<1>		
hit 2 0		VE, FVVIVIXL IS (UY FLIDAISUS.	hita	
UIL 3-2	LUAI <1:0>			IXL PILIS IT ULN			
	If current-limit	is active. PWN	/IxL is driven t	to the state sp	ecified by CLDA	T<0>.	
Note 1: The	ese bits should i	not be changed	d after the PW	Mx module is	enabled (PTEN	= 1).	

REGISTER 16-13: IOCONx: PWMx I/O CONTROL REGISTER⁽²⁾

2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

REGISTER 17-3: QEI1STAT: QEI1 STATUS REGISTER (CONTINUED)

bit 2	HOMIEN: Home Input Event Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled
bit 1	IDXIRQ: Status Flag for Index Event Status bit 1 = Index event has occurred 0 = No Index event has occurred
bit 0	IDXIEN: Index Input Event Interrupt Enable bit 1 = Interrupt is enabled 0 = Interrupt is disabled

Note 1: This status bit is only applicable to PIMOD<2:0> modes, '011' and '100'.

18.1 SPI Helpful Tips

- 1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
 - a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on SSx.
 - b) If FRMPOL = 0, use a pull-up resistor on $\frac{1}{SSx}$.

Note:	This	insures	that	the	first	fra	ame
	transn	nission	after	initializ	ation	is	not
	shifted or corru		upted.				

- 2. In Non-Framed 3-Wire mode, (i.e., not using SSx from a master):
 - a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on SSx.
 - b) If CKP = 0, always place a pull-down resistor on SSx.
 - **Note:** This will insure that during power-up and initialization the master/slave will not lose Sync due to an errant SCKx transition that would cause the slave to accumulate data shift errors for both transmit and receive appearing as corrupted data.
- FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the SSx pin, which indicates the start of a data frame.
 - Note: Not all third-party devices support Frame mode timing. Refer to the SPIx specifications in Section 30.0 "Electrical Characteristics" for details.
- In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPIx data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

18.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

18.2.1 KEY RESOURCES

- "Serial Peripheral Interface (SPI)" (DS70569) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

R-0, HSC	R-0, HSC R-0, HSC U-0 U-		U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC	
ACKSTAT TRSTAT		—	—	BCL	GCSTAT	ADD10		
bit 15					•		bit 8	
R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	
bit 7							bit 0	
Legend: C = Clear		C = Clearab	C = Clearable bit		re Settable bit	HSC = Hardware Settable/Clearable bit		
R = Readable bit V		W = Writable	e bit	U = Unimplen	nented bit, read	as '0'		
-n = Value at POR		'1' = Bit is se	et	'0' = Bit is clea	ared	x = Bit is unknown		

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

bit 15	ACKSTAT: Acknowledge Status bit (when operating as I^2C^{TM} master, applicable to master transmit operation)
	1 = NACK received from slave 0 = ACK received from slave
	Hardware is set or clear at the end of slave Acknowledge.
bit 14	TRSTAT: Transmit Status bit (when operating as I^2C master, applicable to master transmit operation) 1 = Master transmit is in progress (8 bits + ACK)
	0 = Master transmit is not in progress Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
bit 13-11	Unimplemented: Read as '0'
bit 10	BCL: Master Bus Collision Detect bit
	1 = A bus collision has been detected during a master operation0 = No bus collision detected
	Hardware is set at detection of a bus collision.
bit 9	GCSTAT: General Call Status bit
	1 = General call address was received
	0 = General call address was not received
1.11.0	Hardware is set when address matches general call address. Hardware is clear at Stop detection.
DIT 8	ADD10: 10-Bit Address Status bit
	I = 10-bit address was matched 0 = 10-bit address was not matched
	Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
bit 7	IWCOL: I2Cx Write Collision Detect bit
	1 = An attempt to write to the I2CxTRN register failed because the I^2 C module is busy 0 = No collision
	Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
bit 6	I2COV: I2Cx Receive Overflow Flag bit
	 1 = A byte was received while the I2CxRCV register was still holding the previous byte 0 = No overflow
	Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
bit 5	D_A: Data/Address bit (when operating as I ² C slave)
	1 = Indicates that the last byte received was data
	 Indicates that the last byte received was a device address Hardware is clear at a device address match. Hardware is set by reception of a slave byte.
bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware is set or clear when a Start, Repeated Start or Stop is detected.

REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER (CONTINUED)

- bit 1 **RBIF:** RX Buffer Interrupt Flag bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 0 **TBIF:** TX Buffer Interrupt Flag bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred

U-0	R/W-x	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x			
	WAKFIL		—		SEG2PH2	SEG2PH1	SEG2PH0			
bit 15			•	•			bit 8			
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
SEG2PHTS	SAM	SEG1PH2	SEG1PH1	SEG1PH0	PRSEG2	PRSEG1	PRSEG0			
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'				
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown			
bit 15	Unimplemen	nted: Read as '	0'							
bit 14	WAKFIL: Sel	lect CAN Bus L	ine Filter for V	Vake-up bit						
	1 = Uses CAI	N bus line filter	for wake-up	a-un						
bit 13-11		ted. Pead as '		e-up						
bit 10-8	SEG2PH-2.0		u nent 2 hits							
511 10-0	111 = 1 enoth	is 8 x To								
	•									
	•									
	•									
	000 = Length	n is 1 x Tq								
bit 7	SEG2PHTS: Phase Segment 2 Time Select bit									
	1 = Freely programmable									
hit C		1 OF SEGIPHX	Dits or informa	ation Processin	g Time (IPT), w	nicnever is gre	eater			
DIL 6	J = Rus lino i	e of the CAN B	us Line bit a timos at tha	complo point						
	0 = Bus line i	s sampled once	e at the sampl	e point						
bit 5-3	SEG1PH<2:0)>: Phase Segr	nent 1 bits	•						
	111 = Length	n is 8 x Tq								
	•									
	•									
	•									
	000 = Length	n is 1 x Tq								
bit 2-0	PRSEG<2:0>	>: Propagation	Time Segmen	t bits						
	111 = Length	n is 8 x TQ								
	•									
	•									
	-									

REGISTER 21-10: CxCFG2: ECANx BAUD RATE CONFIGURATION REGISTER 2

REGISTER 21-26:	CxTRmnCON: ECANx TX/RX BUFFER mn CONTROL REGISTER	
	(m = 0,2,4,6; n = 1,3,5,7)	

R/W-0) R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXEN	n TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI1	TXnPRI0
bit 15							bit 8
R/W-0) R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENr	n TXABTm ⁽¹⁾	TXLARBm ⁽¹⁾	TXERRm ⁽¹⁾	TXREQm	RTRENm	TXmPRI1	TXmPRI0
bit 7							bit 0
Legend:							
R = Reada	able bit	W = Writable	bit		mented bit, read		
-n = Value	e at POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	IOWN
h:+ 45 0	Cae Definition	a far hita (7:0)	Controlo Duffe				
		1 IOF DILS < 7.0 >,					
DIC 7							
	0 = Buffer TR	Bn is a transm	buffer				
bit 6	TXABTm: Me	essage Aborteg	bit ⁽¹⁾				
	1 = Message	was aborted					
	0 = Message	completed tran	smission suce	cessfully			
bit 5	TXLARBm: N	Message Lost A	Arbitration bit ⁽¹)			
	1 = Message	lost arbitration	while being se	ent			
	0 = Message	did not lose ar	bitration while	being sent			
bit 4	TXERRm: Er	ror Detected D	uring Transmis	ssion bit ⁽¹⁾			
	1 = A bus erro 0 = A bus erro	or occurred wh or did not occu	ile the messag r while the me	je was being s ssage was bei	sent ing sent		
bit 3	TXREQm: M	essage Send R	equest bit				
	1 = Requests	s that a messag	ge be sent; the	bit automatic	ally clears wher	n the message i	s successfully
	sent	the bit to '0' wh	nile set reques	te a maesana	abort		
hit 2	D = Cleaning	ite Dir to 0 wi	ne set reques	is a messaye hit	abolt		
	1 = When a r	emote transmit	is received T	VREO will be	sot		
	0 = When a r	emote transmit	is received, T	XREQ will be	unaffected		
bit 1-0	TXmPRI<1:0	>: Message Tra	ansmission Pri	iority bits			
	11 = Highest	message priori	ity				
	10 = High inte	ermediate mes	sage priority				
	01 = Low interpreter 00 = Lowest	ermediate mess	age priority				
		nessaye prom	•y				
Note 1:	This bit is cleared	when TXREQ i	s set.				

Note: The buffers, SID, EID, DLC, Data Field, and Receive Status registers are located in DMA RAM.

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1		
bit 15				·	- -	·	bit 8		
U-x	U-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
_	—	—	RB0	DLC3	DLC2	DLC1	DLC0		
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	l as '0'			
-n = Value at	POR	'1' = Bit is set	t	'0' = Bit is cleared			x = Bit is unknown		
bit 15-10	EID<5:0>: E>	ktended Identifi	er bits						
bit 9	RTR: Remote	e Transmission	Request bit						
	When IDE =	<u>1:</u>							
	1 = Message	will request re	mote transmis	ssion					
		lessage							
	<u>When IDE = (</u> The RTR bit i	<u>0:</u> is ignored							
hit 9	BB1 : Boson								
DILO	Llear must so	t this hit to '0' r	oor CAN proto						
DIT 7-5	Unimplemen	ted: Read as	0						
bit 4	RB0: Reserve	ed Bit 0							
	User must se	t this bit to '0' p	per CAN proto	COI.					

BUFFER 21-3: ECAN™ MESSAGE BUFFER WORD 2

bit 3-0 DLC<3:0>: Data Length Code bits

BUFFER 21-4: ECAN[™] MESSAGE BUFFER WORD 3

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
			B	yte 1				
bit 15							bit 8	
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
			B	yte 0				
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable I	bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = B		'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		

bit 15-8 Byte 1<15:8>: ECAN Message Byte 1 bits

bit 7-0 Byte 0<7:0>: ECAN Message Byte 0 bits

23.2 ADC Helpful Tips

- 1. The SMPIx control bits in the AD1CON2 register:
 - a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
 - b) When the CSCNA bit in the AD1CON2 registers is set to '1', this determines when the ADC analog scan channel list, defined in the AD1CSSL/AD1CSSH registers, starts over from the beginning.
 - c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
 - d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA.
- 2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMPIx bits and the condition described in 1c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
- 3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer (i.e., ADC1BUF0) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA Controller, before the next ADC conversion is complete to avoid overwriting the previous value.
- 4. The DONE bit (AD1CON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (AD1CON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.

5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for ANO, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUXA selections use ANO-AN2. Carefully study the ADC block diagram to determine the configuration that will best suit your application. Configuration examples are available in the "Analog-to-Digital Converter (ADC)" (DS70621) section in the "dsPIC33/ PIC24 Family Reference Manual".

23.3 ADC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

23.3.1 KEY RESOURCES

- "Analog-to-Digital Converter (ADC)" (DS70621) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
CH0NB		_	CH0SB4 ⁽¹⁾	CH0SB3 ⁽¹⁾	CH0SB2 ⁽¹⁾	CH0SB1 ⁽¹⁾	CH0SB0 ⁽¹⁾		
bit 15		·	•				bit 8		
R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
CH0NA		_	CH0SA4 ⁽¹⁾	CH0SA3 ⁽¹⁾	CH0SA2 ⁽¹⁾	CH0SA1 ⁽¹⁾	CH0SA0 ⁽¹⁾		
bit 7					I		bit 0		
Legend:									
R = Read	able bit	W = Writable b	bit	U = Unimpler	nented bit. read	as '0'			
-n = Value	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	lown		
bit 15	CHONB. Cha	nnel () Negative	Innut Select fo	r Sample MLIX	'B hit				
Sit 10	1 = Channel (negative input	is AN1(1)						
	0 = Channel (0 negative input	is Vrefl						
bit 14-13	Unimplemen	ted: Read as '0'							
bit 12-8	CH0SB<4:0>	Channel 0 Pos	itive Input Sele	ect for Sample	MUXB bits ⁽¹⁾				
	11111 = Ope	en; use this seled	tion with CTM	U capacitive ar	nd time measure	ement			
	11110 = Cha	nnel 0 positive inp	out is connected	to the CTMU te	emperature mea	surement diode	(CTMU TEMP)		
	11101 = Res	erved							
	11100 = Res	erved							
	11011 = Res 11010 = Cha	innel 0 positive ir	nout is the outr	out of OA3/AN6	_ວ (2,3)				
	11001 = Cha	innel 0 positive ir	nput is the outp	out of OA2/AN)(2)				
	11000 = Cha	innel 0 positive ir	nput is the outp	out of OA1/AN3	₃ (2)				
	10111 = Res	erved							
	•								
	•								
	10000 = Res	erved							
	01111 = Cha	innel 0 positive ir	1put is AN15 ⁽³⁾						
	01110 = Cha	innel 0 positive ir	1put is AN14(3)						
	•		iput is AN 13.						
	•								
	•		(0)						
	00010 = Cha	innel 0 positive ir	nput is $AN2^{(3)}$						
	00001 = Cha	innel 0 positive ir	1 put is AN1(3)						
hit 7		nnel 0 Negative	Input Soloct fo		A hit				
	1 = Channel (negative input	is ANI1(1)						
	0 = Channel (0 negative input	is Vrefl						
bit 6-5	Unimplemen	ited: Read as '0'							
		17				in an alt of C			
Note 1:	ANU through AN	v are repurpose	a wnen compa ticular on amn	arator and op a	mp runctionality	is enabled. Se	e ⊢igure 23-1		
	and 3.		uculai op amp				1, 2		
2:	The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1);								

REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER

3: See the "**Pin Diagrams**" section for the available analog channels for each device.

otherwise, the ANx input is used.

DC CH	ARACTE	RISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$							
Param No.	Symbol	Characteristic	Min. Typ. Max. Units Conditions							
	VIL	Input Low Voltage								
DI10		Any I/O Pin and MCLR	Vss	—	0.2 VDD	V				
DI18		I/O Pins with SDAx, SCLx	Vss	_	0.3 VDD	V	SMBus disabled			
DI19		I/O Pins with SDAx, SCLx	Vss	—	0.8	V	SMBus enabled			
	Vih	Input High Voltage								
DI20		I/O Pins Not 5V Tolerant	0.8 VDD	—	Vdd	V	(Note 3)			
		I/O Pins 5V Tolerant and MCLR	0.8 VDD	—	5.5	V	(Note 3)			
		I/O Pins with SDAx, SCLx	0.8 VDD	—	5.5	V	SMBus disabled			
		I/O Pins with SDAx, SCLx	2.1	—	5.5	V	SMBus enabled			
	ICNPU	Change Notification Pull-up Current								
DI30			150	250	550	μA	VDD = 3.3V, VPIN = VSS			
	ICNPD	Change Notification Pull-Down Current ⁽⁴⁾								
DI31			20	50	100	μA	VDD = 3.3V, VPIN = VDD			

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 2: Negative current is defined as current sourced by the pin.
- 3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 4: VIL source < (VSS 0.3). Characterized but not tested.

5: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

- 6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.





FIGURE 30-10: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)



TABLE 30-29: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			Standa (unless Operati	rd Opera otherwis ng tempe	ting Con se stated rature	ditions: 3) -40°C ≤ T -40°C ≤ T	3.0V to 3.6V $A \le +85^{\circ}C$ for Industrial $A \le +125^{\circ}C$ for Extended
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Conditions			
MP10	TFPWM	PWMx Output Fall Time	—			ns	See Parameter DO32
MP11	TRPWM	PWMx Output Rise Time	_	_		ns	See Parameter DO31
MP20	TFD	Fault Input ↓ to PWMx I/O Change	_	_	15	ns	
MP30	Tfh	Fault Input Pulse Width	15	_		ns	

Note 1: These parameters are characterized but not tested in manufacturing.



FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS