



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc204t-i-tl

TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES (CONTINUED)

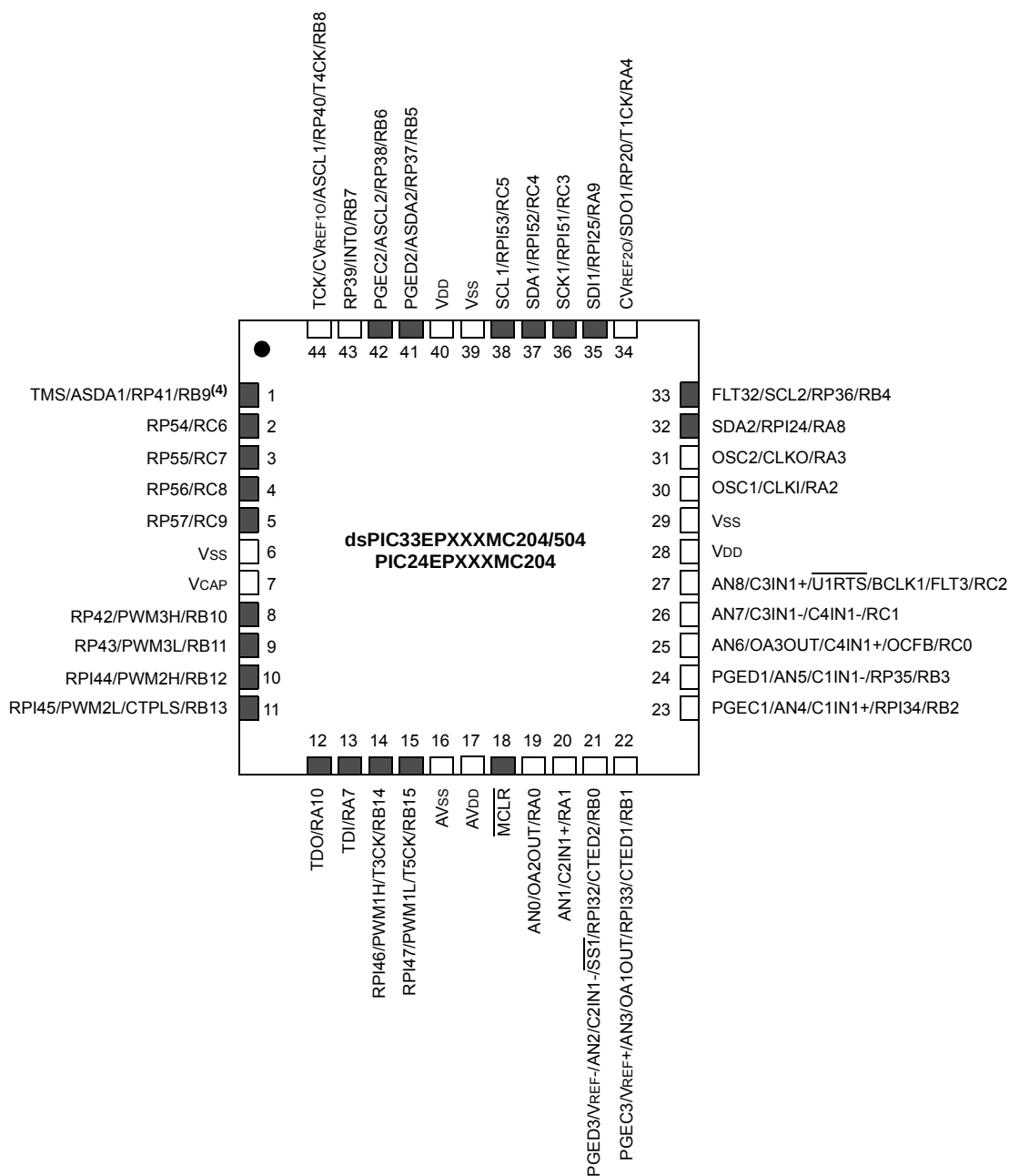
Device	Page Erase Size (Instructions)	Program Flash Memory (Kbytes)	RAM (Kbytes)	Remappable Peripherals										CRC Generator	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	I/O Pins	Pins	Packages
				16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM ⁽⁴⁾ (Channels)	Quadrature Encoder Interface	UART	SPI ⁽²⁾	ECAN™ Technology	External Interrupts ⁽³⁾	I ² C™								
dsPIC33EP32MC504	512	32	4	5	4	4	6	1	2	2	1	3	2	1	9	3/4	Yes	Yes	35	44/ 48	VTLA ⁽⁵⁾ , TQFP, QFN, UQFN
dsPIC33EP64MC504	1024	64	8																		
dsPIC33EP128MC504	1024	128	16																		
dsPIC33EP256MC504	1024	256	32																		
dsPIC33EP512MC504	1024	512	48	5	4	4	6	1	2	2	1	3	2	1	16	3/4	Yes	Yes	53	64	TQFP, QFN
dsPIC33EP64MC506	1024	64	8																		
dsPIC33EP128MC506	1024	128	16																		
dsPIC33EP256MC506	1024	256	32																		
dsPIC33EP512MC506	1024	512	48																		

- Note 1:** On 28-pin devices, Comparator 4 does not have external connections. Refer to **Section 25.0 “Op Amp/Comparator Module”** for details.
2: Only SPI2 is remappable.
3: INT0 is not remappable.
4: Only the PWM Faults are remappable.
5: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

Pin Diagrams (Continued)

44-Pin QFN^(1,2,3)

■ = Pins are up to 5V tolerant



- Note 1:** The RPN/RPI pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
- Note 4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

FIGURE 2-7: INTERLEAVED PFC

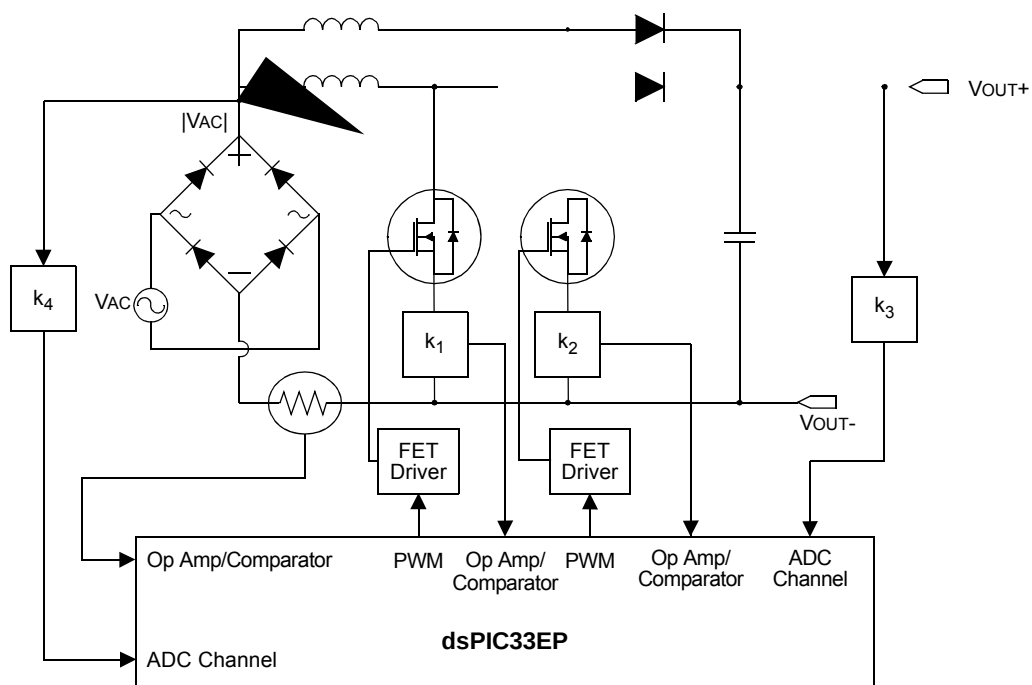


FIGURE 2-8: BEMF VOLTAGE MEASURED USING THE ADC MODULE

REGISTER 8-5: DMAxSTBH: DMA CHANNEL x START ADDRESS REGISTER B (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<23:16>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'bit 7-0 **STB<23:16>:** Secondary Start Address bits (source or destination)**REGISTER 8-6: DMAxSTBL: DMA CHANNEL x START ADDRESS REGISTER B (LOW)**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **STB<15:0>:** Secondary Start Address bits (source or destination)

REGISTER 8-7: DMAxPAD: DMA CHANNEL x PERIPHERAL ADDRESS REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PAD<15:0>**: Peripheral Address Register bits

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-8: DMAxCNT: DMA CHANNEL x TRANSFER COUNT REGISTER⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CNT<13:8> ⁽²⁾					
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNT<7:0> ⁽²⁾							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

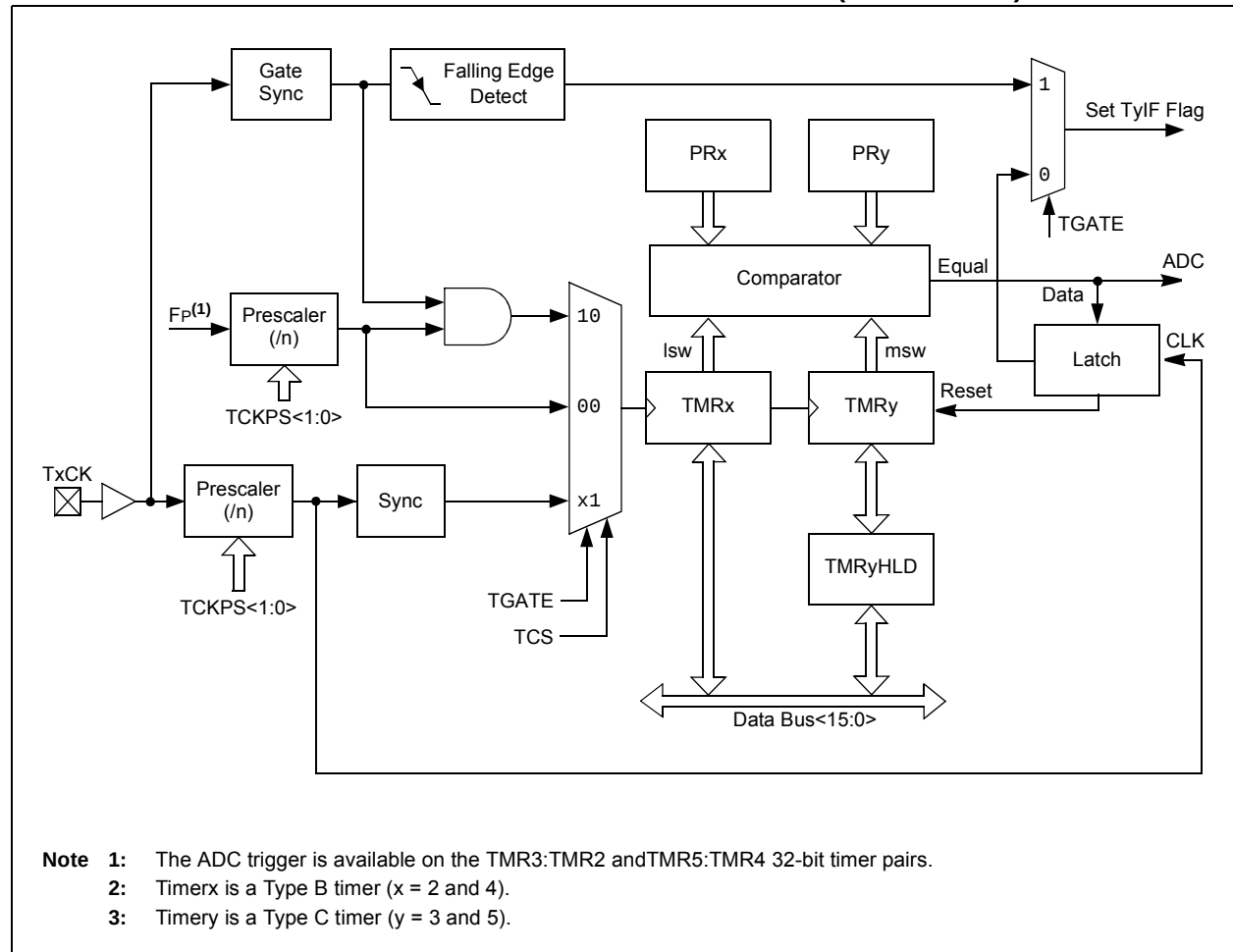
bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **CNT<13:0>**: DMA Transfer Count Register bits⁽²⁾

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

2: The number of DMA transfers = CNT<13:0> + 1.

FIGURE 13-3: TYPE B/TIME C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)



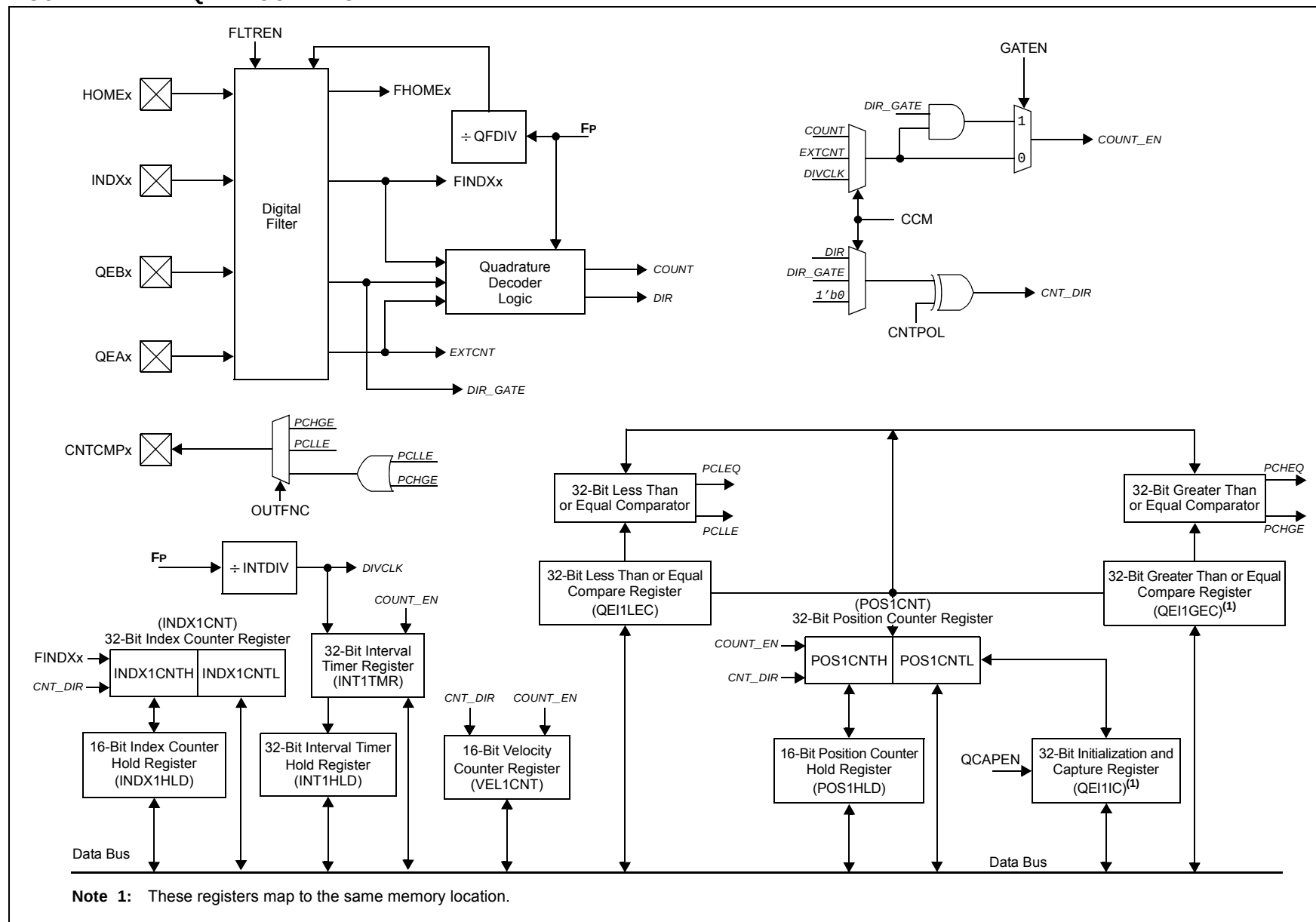
13.1 Timerx/y Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

13.1.1 KEY RESOURCES

- “Timers” (DS70362) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools

FIGURE 17-1: QEI BLOCK DIAGRAM

BUFFER 21-5: ECAN™ MESSAGE BUFFER WORD 4

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 3							
bit 15							
bit 8							

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 2							
bit 7							
bit 0							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Byte 3<15:8>**: ECAN Message Byte 3 bits

bit 7-0 **Byte 2<7:0>**: ECAN Message Byte 2 bits

BUFFER 21-6: ECAN™ MESSAGE BUFFER WORD 5

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 5							
bit 15							
bit 8							

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 4							
bit 7							
bit 0							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **Byte 5<15:8>**: ECAN Message Byte 5 bits

bit 7-0 **Byte 4<7:0>**: ECAN Message Byte 4 bits

REGISTER 25-7: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

U-0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	CVR2OE ⁽¹⁾	—	—	—	VREFSEL	—	—
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVR1OE ⁽¹⁾	CVRR	CVRSS ⁽²⁾	CVR3	CVR2	CVR1	CVR0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'bit 14 **CVR2OE:** Comparator Voltage Reference 2 Output Enable bit⁽¹⁾

1 = (AVDD – AVSS)/2 is connected to the CVREF2O pin

0 = (AVDD – AVSS)/2 is disconnected from the CVREF2O pin

bit 13-11 **Unimplemented:** Read as '0'bit 10 **VREFSEL:** Comparator Voltage Reference Select bit

1 = CVREFIN = VREF+

0 = CVREFIN is generated by the resistor network

bit 9-8 **Unimplemented:** Read as '0'bit 7 **CVREN:** Comparator Voltage Reference Enable bit

1 = Comparator voltage reference circuit is powered on

0 = Comparator voltage reference circuit is powered down

bit 6 **CVR1OE:** Comparator Voltage Reference 1 Output Enable bit⁽¹⁾

1 = Voltage level is output on the CVREF1O pin

0 = Voltage level is disconnected from then CVREF1O pin

bit 5 **CVRR:** Comparator Voltage Reference Range Selection bit

1 = CVRSRC/24 step-size

0 = CVRSRC/32 step-size

bit 4 **CVRSS:** Comparator Voltage Reference Source Selection bit⁽²⁾

1 = Comparator voltage reference source, CVRSRC = (VREF+) – (AVSS)

0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS

bit 3-0 **CVR<3:0>** Comparator Voltage Reference Value Selection $0 \leq \text{CVR<3:0>} \leq 15$ bitsWhen CVRR = 1: $\text{CVREFIN} = (\text{CVR<3:0>}/24) \cdot (\text{CVRSRC})$ When CVRR = 0: $\text{CVREFIN} = (\text{CVRSRC}/4) + (\text{CVR<3:0>}/32) \cdot (\text{CVRSRC})$ **Note 1:** CVR_xOE overrides the TRIS_x and the ANSEL_x bit settings.**Note 2:** In order to operate with CVRSS = 1, at least one of the comparator modules must be enabled.

TABLE 30-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Parameter No.	Typ.	Max.	Units	Conditions		
Operating Current (I _{DD}) ⁽¹⁾						
DC20d	9	15	mA	-40°C	3.3V	10 MIPS
DC20a	9	15	mA	+25°C		
DC20b	9	15	mA	+85°C		
DC20c	9	15	mA	+125°C		
DC22d	16	25	mA	-40°C	3.3V	20 MIPS
DC22a	16	25	mA	+25°C		
DC22b	16	25	mA	+85°C		
DC22c	16	25	mA	+125°C		
DC24d	27	40	mA	-40°C	3.3V	40 MIPS
DC24a	27	40	mA	+25°C		
DC24b	27	40	mA	+85°C		
DC24c	27	40	mA	+125°C		
DC25d	36	55	mA	-40°C	3.3V	60 MIPS
DC25a	36	55	mA	+25°C		
DC25b	36	55	mA	+85°C		
DC25c	36	55	mA	+125°C		
DC26d	41	60	mA	-40°C	3.3V	70 MIPS
DC26a	41	60	mA	+25°C		
DC26b	41	60	mA	+85°C		

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLK0 is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}} = \text{VDD}$, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- CPU is executing `while(1){NOP();}` statement
- JTAG is disabled

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DI50	I _{IL}	Input Leakage Current^(1,2) I/O Pins 5V Tolerant ⁽³⁾	-1	—	+1	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at high-impedance
DI51		I/O Pins Not 5V Tolerant ⁽³⁾	-1	—	+1	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at high-impedance, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
DI51a		I/O Pins Not 5V Tolerant ⁽³⁾	-1	—	+1	μA	Analog pins shared with external reference pins, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
DI51b		I/O Pins Not 5V Tolerant ⁽³⁾	-1	—	+1	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at high-impedance, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$
DI51c		I/O Pins Not 5V Tolerant ⁽³⁾	-1	—	+1	μA	Analog pins shared with external reference pins, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$
DI55		MCLR	-5	—	+5	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD}
DI56		OSC1	-5	—	+5	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT and HS modes

- Note 1:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
- 2:** Negative current is defined as current sourced by the pin.
- 3:** See the “Pin Diagrams” section for the 5V tolerant I/O pins.
- 4:** V_{IL} source < (V_{SS} – 0.3). Characterized but not tested.
- 5:** Non-5V tolerant pins V_{IH} source > (V_{DD} + 0.3), 5V tolerant pins V_{IH} source > 5.5V. Characterized but not tested.
- 6:** Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.
- 7:** Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8:** Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

DMAxSTAH (DMA Channel x Start Address A, High)	144	PTGCST (PTG Control/Status).....	340
DMAxSTAL (DMA Channel x Start Address A, Low)	144	PTGHOLD (PTG Hold)	347
DMAxSTBH (DMA Channel x Start Address B, High)	145	PTGL0 (PTG Literal 0).....	348
DMAxSTBL (DMA Channel x Start Address B, Low)	145	PTGQPTR (PTG Step Queue Pointer)	349
DSADRH (DMA Most Recent RAM High Address)	147	PTGQUEX (PTG Step Queue x)	349
DSADRL (DMA Most Recent RAM Low Address)	147	PTGSDLIM (PTG Step Delay Limit)	346
DTRx (PWMx Dead-Time)	238	PTGT0LIM (PTG Timer0 Limit).....	345
FCLCONx (PWMx Fault Current-Limit Control)	243	PTGT1LIM (PTG Timer1 Limit).....	345
I2CxCON (I2Cx Control)	276	PTPER (PWMx Primary Master Time Base Period).....	233
I2CxMSK (I2Cx Slave Mode Address Mask)	280	PWMCONx (PWMx Control).....	235
I2CxSTAT (I2Cx Status)	278	QE1CON (QE1 Control)	252
ICxCON1 (Input Capture x Control 1)	215	QE1GECH (QE1 Greater Than or Equal Compare High Word).....	262
ICxCON2 (Input Capture x Control 2)	216	QE1GECL (QE1 Greater Than or Equal Compare Low Word)	262
INDX1CNTH (Index Counter 1 High Word)	259	QE1ICH (QE1 Initialization/Capture High Word)	260
INDX1CNTL (Index Counter 1 Low Word)	259	QE1ICL (QE1 Initialization/Capture Low Word)	260
INDX1HLD (Index Counter 1 Hold)	260	QE1IOC (QE1 I/O Control)	254
INT1HLDH (Interval 1 Timer Hold High Word).....	264	QE1LECH (QE1 Less Than or Equal Compare High Word).....	261
INT1HLDL (Interval 1 Timer Hold Low Word)	264	QE1LECL (QE1 Less Than or Equal Compare Low Word)	261
INT1TMRH (Interval 1 Timer High Word).....	263	QE1STAT (QE1 Status).....	256
INT1TMRL (Interval 1 Timer Low Word).....	263	RCON (Reset Control).....	125
INTCON1 (Interrupt Control 1)	134	REFOCON (Reference Oscillator Control)	162
INTCON2 (Interrupt Control 2)	136	RPINR0 (Peripheral Pin Select Input 0).....	183
INTCON2 (Interrupt Control 3).....	137	RPINR1 (Peripheral Pin Select Input 1).....	184
INTCON4 (Interrupt Control 4).....	137	RPINR11 (Peripheral Pin Select Input 11).....	187
INTTREG (Interrupt Control and Status).....	138	RPINR12 (Peripheral Pin Select Input 12).....	188
IOCONx (PWMx I/O Control)	240	RPINR14 (Peripheral Pin Select Input 14).....	189
LEBCONx (PWMx Leading-Edge Blanking Control)	245	RPINR15 (Peripheral Pin Select Input 15).....	190
LEBDLYx (PWMx Leading-Edge Blanking Delay)	246	RPINR18 (Peripheral Pin Select Input 18).....	191
MDC (PWMx Master Duty Cycle).....	234	RPINR19 (Peripheral Pin Select Input 19).....	191
NVMADRH (Nonvolatile Memory Address High)	122	RPINR22 (Peripheral Pin Select Input 22).....	192
NVMADRL (Nonvolatile Memory Address Low).....	122	RPINR23 (Peripheral Pin Select Input 23).....	193
NVMCON (Nonvolatile Memory (NVM) Control)	121	RPINR26 (Peripheral Pin Select Input 26).....	193
NVMKEY (Nonvolatile Memory Key)	122	RPINR3 (Peripheral Pin Select Input 3).....	184
OCxCON1 (Output Compare x Control 1)	221	RPINR37 (Peripheral Pin Select Input 37).....	194
OCxCON2 (Output Compare x Control 2)	223	RPINR38 (Peripheral Pin Select Input 38).....	195
OSCCON (Oscillator Control)	156	RPINR39 (Peripheral Pin Select Input 39).....	196
OSCTUN (FRC Oscillator Tuning)	161	RPINR7 (Peripheral Pin Select Input 7).....	185
PDCx (PWMx Generator Duty Cycle)	237	RPINR8 (Peripheral Pin Select Input 8).....	186
PHASEx (PWMx Primary Phase-Shift)	237	RPOR0 (Peripheral Pin Select Output 0).....	197
PLLFBF (PLL Feedback Divisor)	160	RPOR1 (Peripheral Pin Select Output 1).....	197
PMD1 (Peripheral Module Disable Control 1)	166	RPOR2 (Peripheral Pin Select Output 2).....	198
PMD2 (Peripheral Module Disable Control 2).....	168	RPOR3 (Peripheral Pin Select Output 3).....	198
PMD3 (Peripheral Module Disable Control 3).....	169	RPOR4 (Peripheral Pin Select Output 4).....	199
PMD4 (Peripheral Module Disable Control 4).....	169	RPOR5 (Peripheral Pin Select Output 5).....	199
PMD6 (Peripheral Module Disable Control 6).....	170	RPOR6 (Peripheral Pin Select Output 6).....	200
PMD7 (Peripheral Module Disable Control 7).....	171	RPOR7 (Peripheral Pin Select Output 7).....	200
POS1CNTH (Position Counter 1 High Word)	258	RPOR8 (Peripheral Pin Select Output 8).....	201
POS1CNTL (Position Counter1 Low Word)	258	RPOR9 (Peripheral Pin Select Output 9).....	201
POS1HLD (Position Counter 1 Hold)	258	SEVTCMP (PWMx Primary Special Event Compare)	233
PTCON (PWMx Time Base Control)	230	SPIxCON1 (SPIx Control 1).....	270
PTCON2 (PWMx Primary Master Clock Divider Select 2).....	232	SPIxCON2 (SPIx Control 2).....	272
PTGADJ (PTG Adjust)	348	SPIxSTAT (SPIx Status and Control)	268
PTGBTE (PTG Broadcast Trigger Enable)	343	SR (CPU STATUS).....	40, 132
PTGC0LIM (PTG Counter 0 Limit)	346	T1CON (Timer1 Control)	205
PTGC1LIM (PTG Counter 1 Limit)	347	TRGCONx (PWMx Trigger Control)	239
PTGCON (PTG Control)	342	TRIGx (PWMx Primary Trigger Compare Value).....	242
		TxCON (Timer2 and Timer4 Control)	210