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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc206-i-mr">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc206-i-mr</a>

FIGURE 2-5: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER

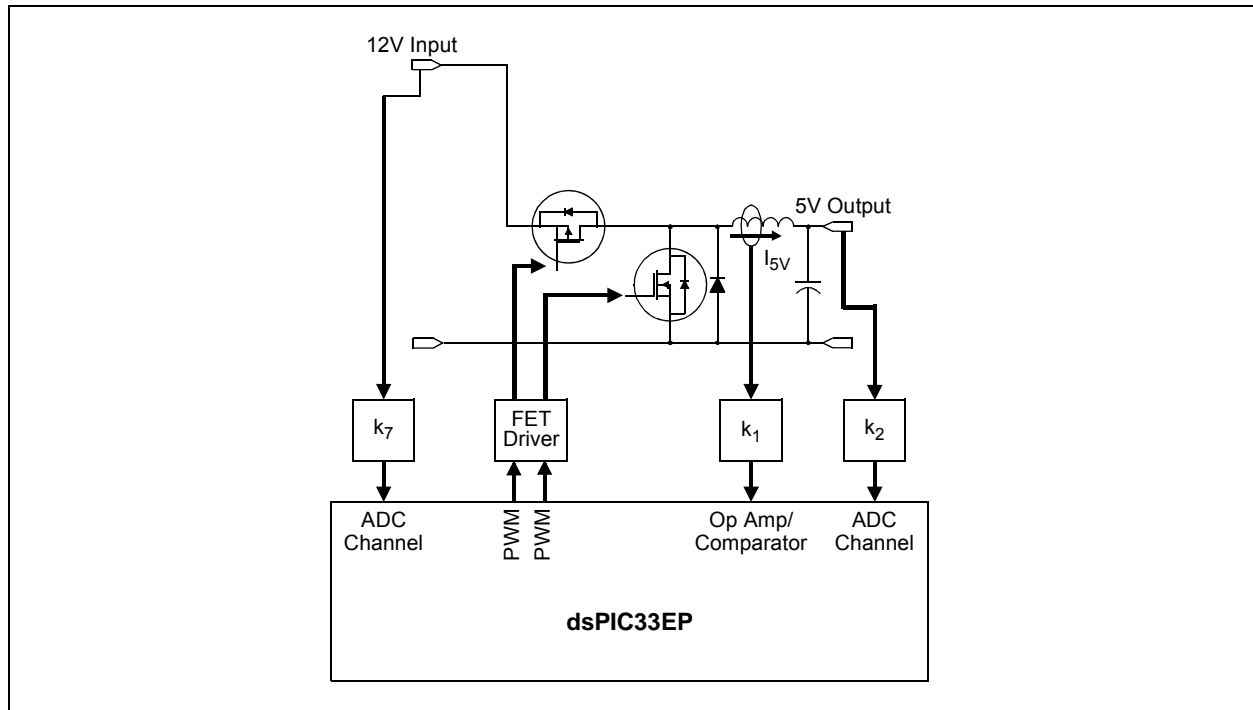
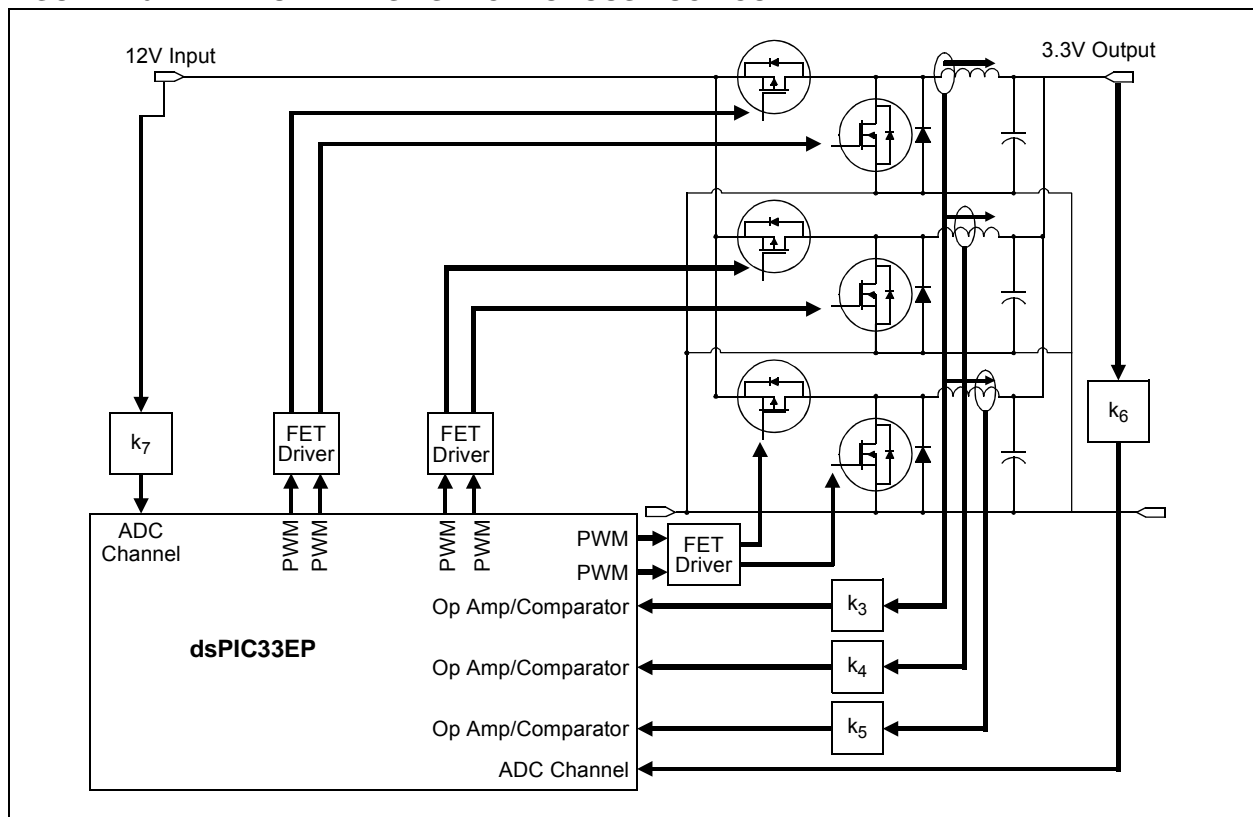


FIGURE 2-6: MULTIPHASE SYNCHRONOUS BUCK CONVERTER



### 3.5 Programmer's Model

The programmer's model for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X is shown in Figure 3-2. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/

MC20X devices contain control registers for Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only), Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only) and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory mapped, as shown in Table 4-1.

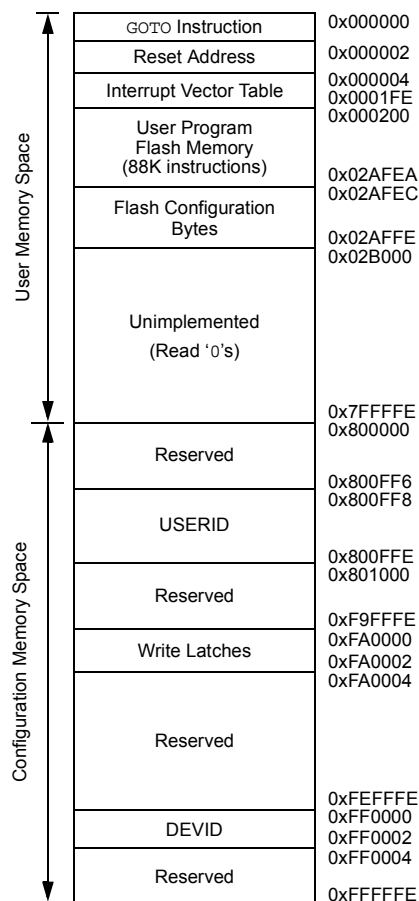
**TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS**

Register(s) Name	Description
W0 through W15	Working Register Array
ACCA, ACBB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
DSRPAG	Extended Data Space (EDS) Read Page Register
DSWPAG	Extended Data Space (EDS) Write Page Register
RCOUNT	REPEAT Loop Count Register
DCOUNT <sup>(1)</sup>	DO Loop Count Register
DOSTARTH <sup>(1,2)</sup> , DOSTARTL <sup>(1,2)</sup>	DO Loop Start Address Register (High and Low)
DOENDH <sup>(1)</sup> , DOENDL <sup>(1)</sup>	DO Loop End Address Register (High and Low)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

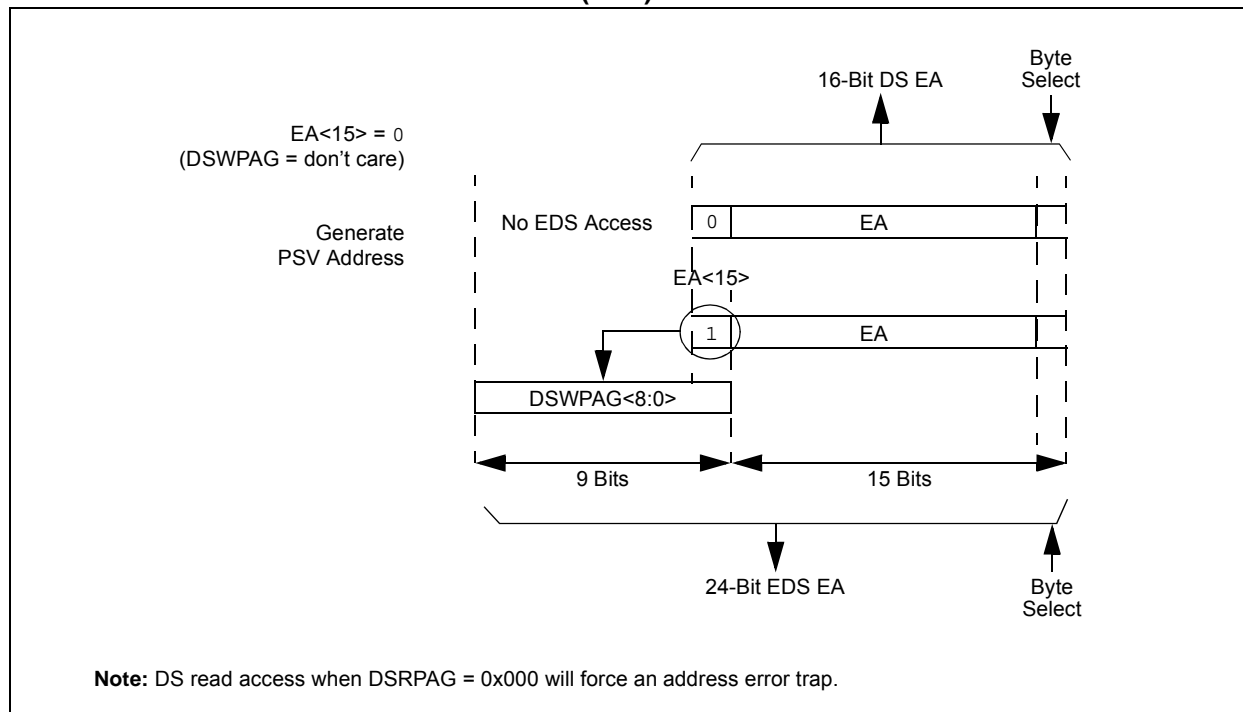
**Note 1:** This register is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

**2:** The DOSTARTH and DOSTARTL registers are read-only.

**FIGURE 4-4: PROGRAM MEMORY MAP FOR dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X AND PIC24EP256GP/MC20X DEVICES**



**Note:** Memory areas are not shown to scale.

**EXAMPLE 4-2: EXTENDED DATA SPACE (EDS) WRITE ADDRESS GENERATION**

The paged memory scheme provides access to multiple 32-Kbyte windows in the EDS and PSV memory. The Data Space Page registers, DSxPAG, in combination with the upper half of the Data Space address, can provide up to 16 Mbytes of additional address space in the EDS and 8 Mbytes (DSRPAG only) of PSV address space. The paged data memory space is shown in Example 4-3.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG. Writes to PS are not supported, so DSWPAG is dedicated to DS, including EDS only. The Data Space and EDS can be read from, and written to, using DSRPAG and DSWPAG, respectively.

#### 4.8.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The **TBLRDH** and **TBLWTL** instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The **TBLRDH** and **TBLWTH** instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit-wide word address spaces, residing side by side, each with the same address range. **TBLRDH** and **TBLWTL** access the space that contains the least significant data word. **TBLRDH** and **TBLWTH** access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

- **TBLRDH** (Table Read High):
  - In Word mode, this instruction maps the lower word of the Program Space location ( $P<15:0>$ ) to a data address ( $D<15:0>$ )

- In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.

- **TBLRDH** (Table Read High):
  - In Word mode, this instruction maps the entire upper word of a program address ( $P<23:16>$ ) to a data address. The 'phantom' byte ( $D<15:8>$ ) is always '0'.
  - In Byte mode, this instruction maps the upper or lower byte of the program word to  $D<7:0>$  of the data address in the **TBLRDH** instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, **TBLWTH** and **TBLWTL**, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (**TBLPAG**). **TBLPAG** covers the entire program memory space of the device, including user application and configuration spaces. When **TBLPAG<7> = 0**, the table page is located in the user memory space. When **TBLPAG<7> = 1**, the page is located in configuration space.

**FIGURE 4-23: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS**

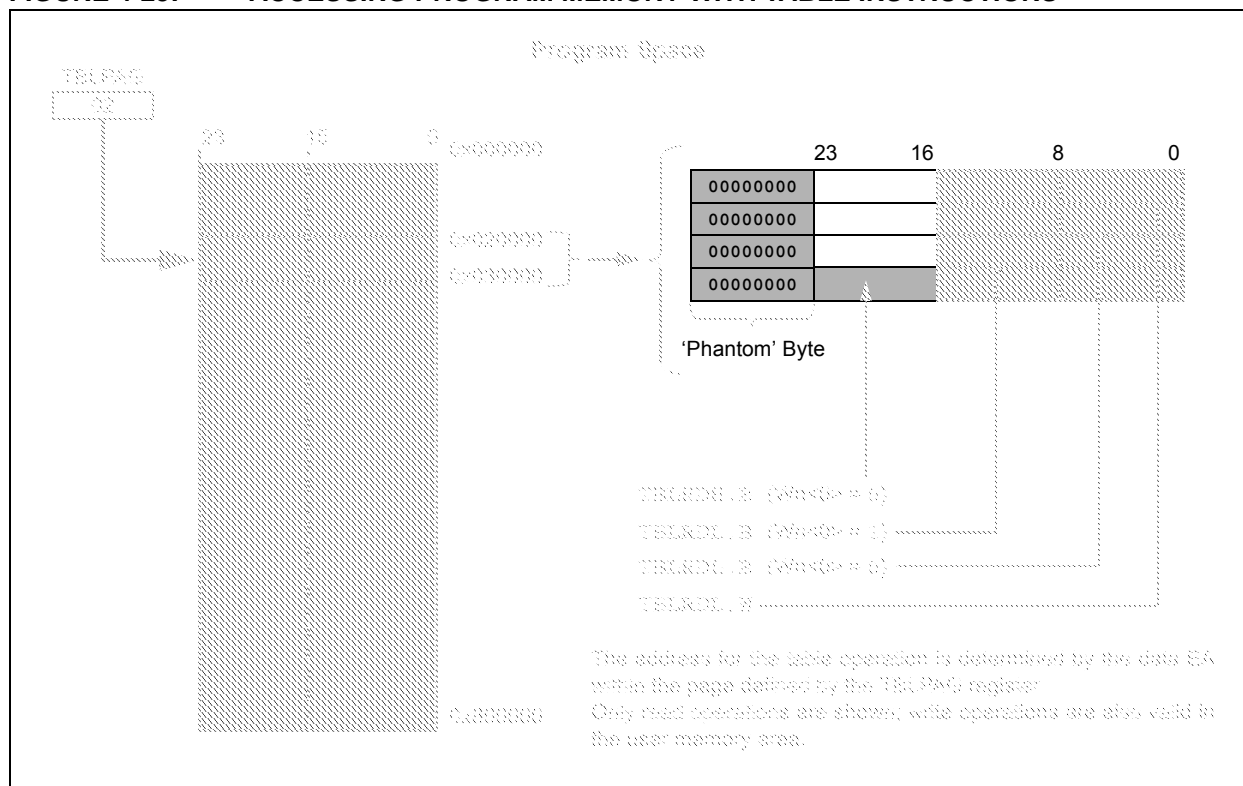


TABLE 7-1: INTERRUPT VECTOR DETAILS

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
Highest Natural Order Priority						
INT0 – External Interrupt 0	8	0	0x000014	IFS0<0>	IEC0<0>	IPC0<2:0>
IC1 – Input Capture 1	9	1	0x000016	IFS0<1>	IEC0<1>	IPC0<6:4>
OC1 – Output Compare 1	10	2	0x000018	IFS0<2>	IEC0<2>	IPC0<10:8>
T1 – Timer1	11	3	0x00001A	IFS0<3>	IEC0<3>	IPC0<14:12>
DMA0 – DMA Channel 0	12	4	0x00001C	IFS0<4>	IEC0<4>	IPC1<2:0>
IC2 – Input Capture 2	13	5	0x00001E	IFS0<5>	IEC0<5>	IPC1<6:4>
OC2 – Output Compare 2	14	6	0x000020	IFS0<6>	IEC0<6>	IPC1<10:8>
T2 – Timer2	15	7	0x000022	IFS0<7>	IEC0<7>	IPC1<14:12>
T3 – Timer3	16	8	0x000024	IFS0<8>	IEC0<8>	IPC2<2:0>
SPI1E – SPI1 Error	17	9	0x000026	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 – SPI1 Transfer Done	18	10	0x000028	IFS0<10>	IEC0<10>	IPC2<10:8>
U1RX – UART1 Receiver	19	11	0x00002A	IFS0<11>	IEC0<11>	IPC2<14:12>
U1TX – UART1 Transmitter	20	12	0x00002C	IFS0<12>	IEC0<12>	IPC3<2:0>
AD1 – ADC1 Convert Done	21	13	0x00002E	IFS0<13>	IEC0<13>	IPC3<6:4>
DMA1 – DMA Channel 1	22	14	0x000030	IFS0<14>	IEC0<14>	IPC3<10:8>
Reserved	23	15	0x000032	—	—	—
SI2C1 – I2C1 Slave Event	24	16	0x000034	IFS1<0>	IEC1<0>	IPC4<2:0>
MI2C1 – I2C1 Master Event	25	17	0x000036	IFS1<1>	IEC1<1>	IPC4<6:4>
CM – Comparator Combined Event	26	18	0x000038	IFS1<2>	IEC1<2>	IPC4<10:8>
CN – Input Change Interrupt	27	19	0x00003A	IFS1<3>	IEC1<3>	IPC4<14:12>
INT1 – External Interrupt 1	28	20	0x00003C	IFS1<4>	IEC1<4>	IPC5<2:0>
Reserved	29-31	21-23	0x00003E-0x000042	—	—	—
DMA2 – DMA Channel 2	32	24	0x000044	IFS1<8>	IEC1<8>	IPC6<2:0>
OC3 – Output Compare 3	33	25	0x000046	IFS1<9>	IEC1<9>	IPC6<6:4>
OC4 – Output Compare 4	34	26	0x000048	IFS1<10>	IEC1<10>	IPC6<10:8>
T4 – Timer4	35	27	0x00004A	IFS1<11>	IEC1<11>	IPC6<14:12>
T5 – Timer5	36	28	0x00004C	IFS1<12>	IEC1<12>	IPC7<2:0>
INT2 – External Interrupt 2	37	29	0x00004E	IFS1<13>	IEC1<13>	IPC7<6:4>
U2RX – UART2 Receiver	38	30	0x000050	IFS1<14>	IEC1<14>	IPC7<10:8>
U2TX – UART2 Transmitter	39	31	0x000052	IFS1<15>	IEC1<15>	IPC7<14:12>
SPI2E – SPI2 Error	40	32	0x000054	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 – SPI2 Transfer Done	41	33	0x000056	IFS2<1>	IEC2<1>	IPC8<6:4>
C1RX – CAN1 RX Data Ready <sup>(1)</sup>	42	34	0x000058	IFS2<2>	IEC2<2>	IPC8<10:8>
C1 – CAN1 Event <sup>(1)</sup>	43	35	0x00005A	IFS2<3>	IEC2<3>	IPC8<14:12>
DMA3 – DMA Channel 3	44	36	0x00005C	IFS2<4>	IEC2<4>	IPC9<2:0>
IC3 – Input Capture 3	45	37	0x00005E	IFS2<5>	IEC2<5>	IPC9<6:4>
IC4 – Input Capture 4	46	38	0x000060	IFS2<6>	IEC2<6>	IPC9<10:8>
Reserved	47-56	39-48	0x000062-0x000074	—	—	—
SI2C2 – I2C2 Slave Event	57	49	0x000076	IFS3<1>	IEC3<1>	IPC12<6:4>
MI2C2 – I2C2 Master Event	58	50	0x000078	IFS3<2>	IEC3<2>	IPC12<10:8>
Reserved	59-64	51-56	0x00007A-0x000084	—	—	—
PSEM – PWM Special Event Match <sup>(2)</sup>	65	57	0x000086	IFS3<9>	IEC3<9>	IPC14<6:4>

**Note 1:** This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

**Note 2:** This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**REGISTER 8-13: DMALCA: DMA LAST CHANNEL ACTIVE STATUS REGISTER**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	R-1	R-1	R-1	R-1
—	—	—	—	LSTCH<3:0>			
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-4

**Unimplemented:** Read as '0'

bit 3-0

**LSTCH<3:0>:** Last DMAC Channel Active Status bits

1111 = No DMA transfer has occurred since system Reset

1110 = Reserved

•

•

•

0100 = Reserved

0011 = Last data transfer was handled by Channel 3

0010 = Last data transfer was handled by Channel 2

0001 = Last data transfer was handled by Channel 1

0000 = Last data transfer was handled by Channel 0



### 11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx and TRISx registers for data control, port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs other than VDD by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum VIH specification for that particular pin.

See the “Pin Diagrams” section for the available 5V tolerant pins and Table 30-11 for the maximum VIH specification for each pin.

## 11.2 Configuring Analog and Digital Port Pins

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of analog in the Pinout I/O Descriptions (see Table 1-1).

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or comparator module.

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

### 11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP, as shown in Example 11-1.

## 11.3 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the Change Notification (CN) functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups and pull-downs act as a current source or sink source connected to the pin and eliminate the need for external resistors when push button, or keypad devices are connected. The pull-ups and pull-downs are enabled separately, using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

**Note:** Pull-ups and pull-downs on Change Notification pins should always be disabled when the port pin is configured as a digital output.

### EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

```
MOV    0xFF00, W0    ; Configure PORTB<15:8>
                        ; as inputs
MOV    W0, TRISB     ; and PORTB<7:0>
                        ; as outputs
NOP                                ; Delay 1 cycle
BTSS   PORTB, #13    ; Next Instruction
```

## 14.2 Input Capture Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—
bit 15						bit 8	

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	IC11	IC10	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7						bit 0	

<b>Legend:</b>	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture Stop in Idle Control bit  
 1 = Input capture will Halt in CPU Idle mode  
 0 = Input capture will continue to operate in CPU Idle mode

bit 12-10 **ICTSEL<2:0>:** Input Capture Timer Select bits  
 111 = Peripheral clock (FP) is the clock source of the ICx  
 110 = Reserved  
 101 = Reserved  
 100 = T1CLK is the clock source of the ICx (only the synchronous clock is supported)  
 011 = T5CLK is the clock source of the ICx  
 010 = T4CLK is the clock source of the ICx  
 001 = T2CLK is the clock source of the ICx  
 000 = T3CLK is the clock source of the ICx

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **IC1<1:0>:** Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)  
 11 = Interrupt on every fourth capture event  
 10 = Interrupt on every third capture event  
 01 = Interrupt on every second capture event  
 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)  
 1 = Input capture buffer overflow occurred  
 0 = No input capture buffer overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)  
 1 = Input capture buffer is not empty, at least one more capture value can be read  
 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits  
 111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)  
 110 = Unused (module is disabled)  
 101 = Capture mode, every 16th rising edge (Prescaler Capture mode)  
 100 = Capture mode, every 4th rising edge (Prescaler Capture mode)  
 011 = Capture mode, every rising edge (Simple Capture mode)  
 010 = Capture mode, every falling edge (Simple Capture mode)  
 001 = Capture mode, every edge rising and falling (Edge Detect mode (IC1<1:0>) is not used in this mode)  
 000 = Input capture module is turned off

**REGISTER 16-10: DTRx: PWMx DEAD-TIME REGISTER**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTRx<7:0>							
bit 7							bit 0

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-14      **Unimplemented:** Read as '0'

bit 13-0      **DTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

**REGISTER 16-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ALTDTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALTDTRx<7:0>							
bit 7							bit 0

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-14      **Unimplemented:** Read as '0'

bit 13-0      **ALTDTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

**REGISTER 21-16: CxRXFnSID: ECANx ACCEPTANCE FILTER n STANDARD IDENTIFIER REGISTER (n = 0-15)**

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15						bit 8	

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	EXIDE	—	EID17	EID16
bit 7						bit 0	

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-5      **SID<10:0>**: Standard Identifier bits  
                  1 = Message address bit, SIDx, must be '1' to match filter  
                  0 = Message address bit, SIDx, must be '0' to match filter
- bit 4      **Unimplemented**: Read as '0'
- bit 3      **EXIDE**: Extended Identifier Enable bit  
                  If MIDE = 1:  
                  1 = Matches only messages with Extended Identifier addresses  
                  0 = Matches only messages with Standard Identifier addresses  
                  If MIDE = 0:  
                  Ignores EXIDE bit.
- bit 2      **Unimplemented**: Read as '0'
- bit 1-0      **EID<17:16>**: Extended Identifier bits  
                  1 = Message address bit, EIDx, must be '1' to match filter  
                  0 = Message address bit, EIDx, must be '0' to match filter

**REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER<sup>(1,2)</sup> (CONTINUED)**

bit 4	<b>OC1CS:</b> Clock Source for OC1 bit 1 = Generates clock pulse when the broadcast command is executed 0 = Does not generate clock pulse when the broadcast command is executed
bit 3	<b>OC4TSS:</b> Trigger/Synchronization Source for OC4 bit 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
bit 2	<b>OC3TSS:</b> Trigger/Synchronization Source for OC3 bit 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
bit 1	<b>OC2TSS:</b> Trigger/Synchronization Source for OC2 bit 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed
bit 0	<b>OC1TSS:</b> Trigger/Synchronization Source for OC1 bit 1 = Generates Trigger/Synchronization when the broadcast command is executed 0 = Does not generate Trigger/Synchronization when the broadcast command is executed

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**2:** This register is only used with the PTGCTRL OPTION = 1111 Step command.

**REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER (CONTINUED)**

- bit 5        **Unimplemented:** Read as '0'
- bit 4        **CREF:** Comparator Reference Select bit (VIN+ input)<sup>(1)</sup>  
              1 = VIN+ input connects to internal CVREFIN voltage  
              0 = VIN+ input connects to C4IN1+ pin
- bit 3-2      **Unimplemented:** Read as '0'
- bit 1-0      **CCH<1:0>:** Comparator Channel Select bits<sup>(1)</sup>  
              11 = VIN- input of comparator connects to OA3/AN6  
              10 = VIN- input of comparator connects to OA2/AN0  
              01 = VIN- input of comparator connects to OA1/AN3  
              00 = VIN- input of comparator connects to C4IN1-

**Note 1:** Inputs that are selected and not available will be tied to Vss. See the “Pin Diagrams” section for available inputs for each package.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles <sup>(2)</sup>	Status Flags Affected
9	BTG	BTG <i>f</i> ,#bit4	Bit Toggle <i>f</i>	1	1	None
		BTG <i>Ws</i> ,#bit4	Bit Toggle <i>Ws</i>	1	1	None
10	BTSC	BTSC <i>f</i> ,#bit4	Bit Test <i>f</i> , Skip if Clear	1	1 (2 or 3)	None
		BTSC <i>Ws</i> ,#bit4	Bit Test <i>Ws</i> , Skip if Clear	1	1 (2 or 3)	None
11	BTSS	BTSS <i>f</i> ,#bit4	Bit Test <i>f</i> , Skip if Set	1	1 (2 or 3)	None
		BTSS <i>Ws</i> ,#bit4	Bit Test <i>Ws</i> , Skip if Set	1	1 (2 or 3)	None
12	BTST	BTST <i>f</i> ,#bit4	Bit Test <i>f</i>	1	1	Z
		BTST.C <i>Ws</i> ,#bit4	Bit Test <i>Ws</i> to C	1	1	C
		BTST.Z <i>Ws</i> ,#bit4	Bit Test <i>Ws</i> to Z	1	1	Z
		BTST.C <i>Ws</i> , <i>Wb</i>	Bit Test <i>Ws</i> < <i>Wb</i> > to C	1	1	C
		BTST.Z <i>Ws</i> , <i>Wb</i>	Bit Test <i>Ws</i> < <i>Wb</i> > to Z	1	1	Z
13	BTSTS	BTSTS <i>f</i> ,#bit4	Bit Test then Set <i>f</i>	1	1	Z
		BTSTS.C <i>Ws</i> ,#bit4	Bit Test <i>Ws</i> to C, then Set	1	1	C
		BTSTS.Z <i>Ws</i> ,#bit4	Bit Test <i>Ws</i> to Z, then Set	1	1	Z
14	CALL	CALL <i>lit</i> 23	Call subroutine	2	4	SFA
		CALL <i>Wn</i>	Call indirect subroutine	1	4	SFA
		CALL.L <i>Wn</i>	Call indirect subroutine (long address)	1	4	SFA
15	CLR	CLR <i>f</i>	<i>f</i> = 0x0000	1	1	None
		CLR WREG	WREG = 0x0000	1	1	None
		CLR <i>Ws</i>	<i>Ws</i> = 0x0000	1	1	None
		CLR <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> , <i>AWB</i> <sup>(1)</sup>	Clear Accumulator	1	1	OA,OB,SA,SB
16	CLRWDT	CLRWDT	Clear Watchdog Timer	1	1	WDTO,Sleep
17	COM	COM <i>f</i>	<i>f</i> = $\bar{f}$	1	1	N,Z
		COM <i>f</i> ,WREG	WREG = $\bar{f}$	1	1	N,Z
		COM <i>Ws</i> , <i>Wd</i>	<i>Wd</i> = $\overline{Ws}$	1	1	N,Z
18	CP	CP <i>f</i>	Compare <i>f</i> with WREG	1	1	C,DC,N,OV,Z
		CP <i>Wb</i> ,#lit8	Compare <i>Wb</i> with lit8	1	1	C,DC,N,OV,Z
		CP <i>Wb</i> , <i>Ws</i>	Compare <i>Wb</i> with <i>Ws</i> ( <i>Wb</i> – <i>Ws</i> )	1	1	C,DC,N,OV,Z
19	CP0	CP0 <i>f</i>	Compare <i>f</i> with 0x0000	1	1	C,DC,N,OV,Z
		CP0 <i>Ws</i>	Compare <i>Ws</i> with 0x0000	1	1	C,DC,N,OV,Z
20	CPB	CPB <i>f</i>	Compare <i>f</i> with WREG, with Borrow	1	1	C,DC,N,OV,Z
		CPB <i>Wb</i> ,#lit8	Compare <i>Wb</i> with lit8, with Borrow	1	1	C,DC,N,OV,Z
		CPB <i>Wb</i> , <i>Ws</i>	Compare <i>Wb</i> with <i>Ws</i> , with Borrow ( <i>Wb</i> – <i>Ws</i> – C)	1	1	C,DC,N,OV,Z
21	CPSEQ	CPSEQ <i>Wb</i> , <i>Wn</i>	Compare <i>Wb</i> with <i>Wn</i> , skip if =	1	1 (2 or 3)	None
	CPBEQ	CPBEQ <i>Wb</i> , <i>Wn</i> , <i>Expr</i>	Compare <i>Wb</i> with <i>Wn</i> , branch if =	1	1 (5)	None
22	CPSGT	CPSGT <i>Wb</i> , <i>Wn</i>	Compare <i>Wb</i> with <i>Wn</i> , skip if >	1	1 (2 or 3)	None
	CPBGT	CPBGT <i>Wb</i> , <i>Wn</i> , <i>Expr</i>	Compare <i>Wb</i> with <i>Wn</i> , branch if >	1	1 (5)	None
23	CPSLT	CPSLT <i>Wb</i> , <i>Wn</i>	Compare <i>Wb</i> with <i>Wn</i> , skip if <	1	1 (2 or 3)	None
	CPBLT	CPBLT <i>Wb</i> , <i>Wn</i> , <i>Expr</i>	Compare <i>Wb</i> with <i>Wn</i> , branch if <	1	1 (5)	None
24	CPSNE	CPSNE <i>Wb</i> , <i>Wn</i>	Compare <i>Wb</i> with <i>Wn</i> , skip if ≠	1	1 (2 or 3)	None
	CPBNE	CPBNE <i>Wb</i> , <i>Wn</i> , <i>Expr</i>	Compare <i>Wb</i> with <i>Wn</i> , branch if ≠	1	1 (5)	None

**Note 1:** These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles <sup>(2)</sup>	Status Flags Affected
25	DAW	DAW Wn	Wn = decimal adjust Wn	1	1	C
26	DEC	DEC f	$f = f - 1$	1	1	C,DC,N,OV,Z
		DEC f, WREG	WREG = $f - 1$	1	1	C,DC,N,OV,Z
		DEC Ws, Wd	$Wd = Ws - 1$	1	1	C,DC,N,OV,Z
27	DEC2	DEC2 f	$f = f - 2$	1	1	C,DC,N,OV,Z
		DEC2 f, WREG	WREG = $f - 2$	1	1	C,DC,N,OV,Z
		DEC2 Ws, Wd	$Wd = Ws - 2$	1	1	C,DC,N,OV,Z
28	DISI	DISI #lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S Wm, Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD Wm, Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U Wm, Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD Wm, Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF Wm, Wn <sup>(1)</sup>	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO #lit15, Expr <sup>(1)</sup>	Do code to PC + Expr, lit15 + 1 times	2	2	None
		DO Wn, Expr <sup>(1)</sup>	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED Wm*Wm, Acc, Wx, Wy, Wxd <sup>(1)</sup>	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB,SA,SB,SAB
33	EDAC	EDAC Wm*Wm, Acc, Wx, Wy, Wxd <sup>(1)</sup>	Euclidean Distance	1	1	OA,OB,OAB,SA,SB,SAB
34	EXCH	EXCH Wns, Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL Ws, Wnd	Find Bit Change from Left (MSb) Side	1	1	C
36	FF1L	FF1L Ws, Wnd	Find First One from Left (MSb) Side	1	1	C
37	FF1R	FF1R Ws, Wnd	Find First One from Right (LSb) Side	1	1	C
38	GOTO	GOTO Expr	Go to address	2	4	None
		GOTO Wn	Go to indirect	1	4	None
		GOTO.L Wn	Go to indirect (long address)	1	4	None
39	INC	INC f	$f = f + 1$	1	1	C,DC,N,OV,Z
		INC f, WREG	WREG = $f + 1$	1	1	C,DC,N,OV,Z
		INC Ws, Wd	$Wd = Ws + 1$	1	1	C,DC,N,OV,Z
40	INC2	INC2 f	$f = f + 2$	1	1	C,DC,N,OV,Z
		INC2 f, WREG	WREG = $f + 2$	1	1	C,DC,N,OV,Z
		INC2 Ws, Wd	$Wd = Ws + 2$	1	1	C,DC,N,OV,Z
41	IOR	IOR f	$f = f .IOR. WREG$	1	1	N,Z
		IOR f, WREG	WREG = $f .IOR. WREG$	1	1	N,Z
		IOR #lit10, Wn	$Wd = lit10 .IOR. Wd$	1	1	N,Z
		IOR Wb, Ws, Wd	$Wd = Wb .IOR. Ws$	1	1	N,Z
		IOR Wb, #lit5, Wd	$Wd = Wb .IOR. lit5$	1	1	N,Z
42	LAC	LAC Wso, #Slit4, Acc	Load Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
43	LNK	LNK #lit14	Link Frame Pointer	1	1	SFA
44	LSR	LSR f	$f = \text{Logical Right Shift } f$	1	1	C,N,OV,Z
		LSR f, WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR Ws, Wd	$Wd = \text{Logical Right Shift } Ws$	1	1	C,N,OV,Z
		LSR Wb, Wns, Wnd	$Wnd = \text{Logical Right Shift } Wb \text{ by } Wns$	1	1	N,Z
		LSR Wb, #lit5, Wnd	$Wnd = \text{Logical Right Shift } Wb \text{ by } lit5$	1	1	N,Z
45	MAC	MAC Wm*Wn, Acc, Wx, Wxd, Wy, Wyd, AWB <sup>(1)</sup>	Multiply and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
		MAC Wm*Wm, Acc, Wx, Wxd, Wy, Wyd <sup>(1)</sup>	Square and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB

**Note 1:** These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.



FIGURE 30-5: TIMER1-TIMER5 EXTERNAL CLOCK TIMING CHARACTERISTICS

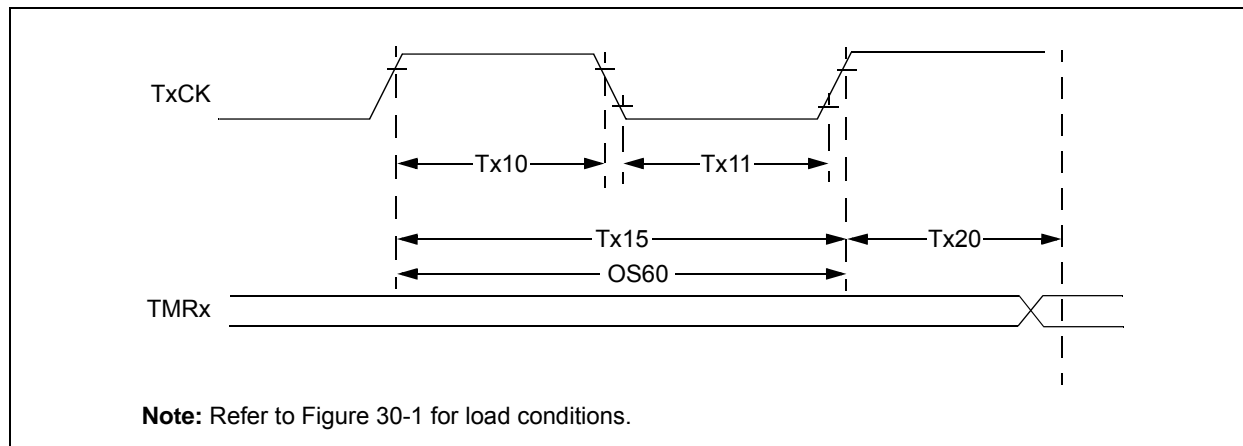


TABLE 30-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS<sup>(1)</sup>

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic <sup>(2)</sup>		Min.	Typ.	Max.	Units	Conditions
TA10	TtxH	T1CK High Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	—	—	ns	Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256)
			Asynchronous	35	—	—	ns	
TA11	TtxL	T1CK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	—	—	ns	Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256)
			Asynchronous	10	—	—	ns	
TA15	TtxP	T1CK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N	—	—	ns	N = prescale value (1, 8, 64, 256)
OS60	Ft1	T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>))		DC	—	50	kHz	
TA20	TCKEXTMRL	Delay from External T1CK Clock Edge to Timer Increment		0.75 Tcy + 40	—	1.75 Tcy + 40	ns	

**Note 1:** Timer1 is a Type A.

**Note 2:** These parameters are characterized, but are not tested in manufacturing.

TABLE 30-58: ADC MODULE SPECIFICATIONS (12-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) <sup>(1)</sup> Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
ADC Accuracy (12-Bit Mode)							
AD20a	Nr	Resolution	12 Data Bits			bits	
AD21a	INL	Integral Nonlinearity	-2.5	—	2.5	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-5.5	—	5.5	LSb	+85°C < TA ≤ +125°C (Note 2)
AD22a	DNL	Differential Nonlinearity	-1	—	1	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-1	—	1	LSb	+85°C < TA ≤ +125°C (Note 2)
AD23a	GERR	Gain Error <sup>(3)</sup>	-10	—	10	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-10	—	10	LSb	+85°C < TA ≤ +125°C (Note 2)
AD24a	EOFF	Offset Error	-5	—	5	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-5	—	5	LSb	+85°C < TA ≤ +125°C (Note 2)
AD25a	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance (12-Bit Mode)							
AD30a	THD	Total Harmonic Distortion <sup>(3)</sup>	—	75	—	dB	
AD31a	SINAD	Signal to Noise and Distortion <sup>(3)</sup>	—	68	—	dB	
AD32a	SFDR	Spurious Free Dynamic Range <sup>(3)</sup>	—	80	—	dB	
AD33a	FNYQ	Input Signal Bandwidth <sup>(3)</sup>	—	250	—	kHz	
AD34a	ENOB	Effective Number of Bits <sup>(3)</sup>	11.09	11.3	—	bits	

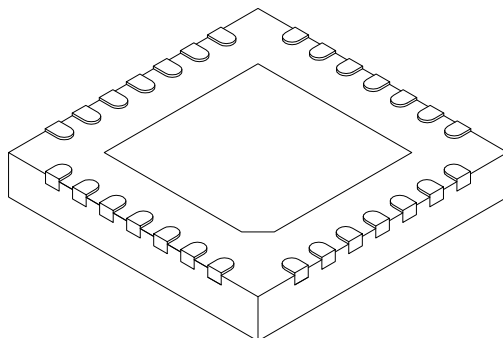
**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

**3:** Parameters are characterized but not tested in manufacturing.

## 28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.70
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.70
Terminal Width	b	0.23	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed Pad	K	0.20	-	-

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

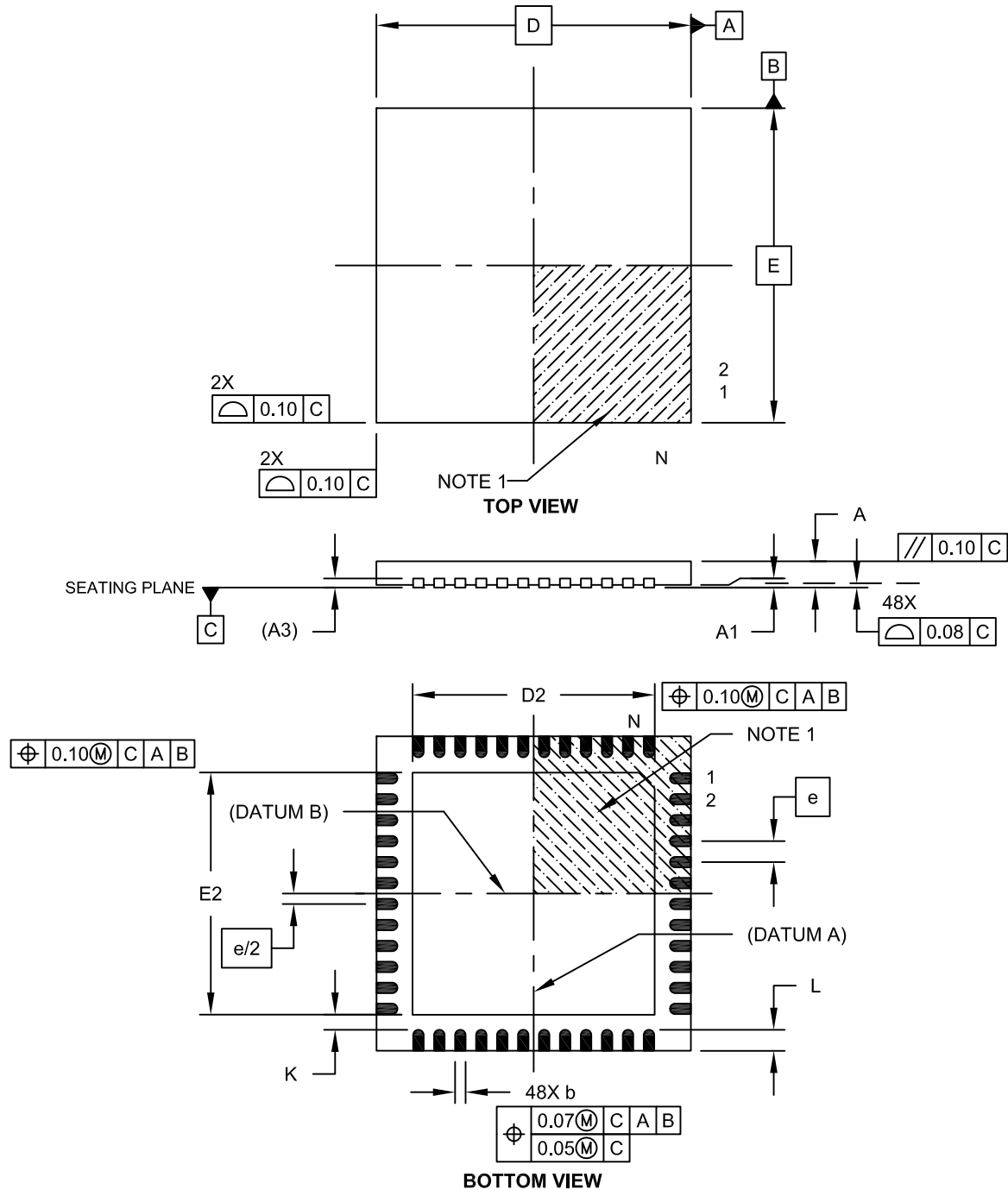
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

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48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-153A Sheet 1 of 2

**Revision E (April 2012)**

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

**TABLE A-4: MAJOR SECTION UPDATES**

Section Name	Update Description
<b>“16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High-Speed PWM, Op amps, and Advanced Analog”</b>	<p>The following 512-Kbyte devices were added to the General Purpose Families table (see Table 1):</p> <ul style="list-style-type: none"> <li>• PIC24EP512GP202</li> <li>• PIC24EP512GP204</li> <li>• PIC24EP512GP206</li> <li>• dsPIC33EP512GP502</li> <li>• dsPIC33EP512GP504</li> <li>• dsPIC33EP512GP506</li> </ul> <p>The following 512-Kbyte devices were added to the Motor Control Families table (see Table 2):</p> <ul style="list-style-type: none"> <li>• PIC24EP512MC202</li> <li>• PIC24EP512MC204</li> <li>• PIC24EP512MC206</li> <li>• dsPIC33EP512MC202</li> <li>• dsPIC33EP512MC204</li> <li>• dsPIC33EP512MC206</li> <li>• dsPIC33EP512MC502</li> <li>• dsPIC33EP512MC504</li> <li>• dsPIC33EP512MC506</li> </ul> <p>Certain Pin Diagrams were updated to include the new 512-Kbyte devices.</p>
<b>Section 4.0 “Memory Organization”</b>	<p>Added a Program Memory Map for the new 512-Kbyte devices (see Figure 4-4).</p> <p>Added a Data Memory Map for the new dsPIC 512-Kbyte devices (see Figure 4-11).</p> <p>Added a Data Memory Map for the new PIC24 512-Kbyte devices (see Figure 4-16).</p>
<b>Section 7.0 “Interrupt Controller”</b>	Updated the VECNUM bits in the INTTREG register (see Register 7-7).
<b>Section 11.0 “I/O Ports”</b>	Added tip 6 to <b>Section 11.5 “I/O Helpful Tips”</b> .
<b>Section 27.0 “Special Features”</b>	<p>The following modifications were made to the Configuration Byte Register Map (see Table 27-1):</p> <ul style="list-style-type: none"> <li>• Added the column Device Memory Size (Kbytes)</li> <li>• Removed Notes 1 through 4</li> <li>• Added addresses for the new 512-Kbyte devices</li> </ul>
<b>Section 30.0 “Electrical Characteristics”</b>	<p>Updated the Minimum value for Parameter DC10 (see Table 30-4).</p> <p>Added Power-Down Current (I<sub>pd</sub>) parameters for the new 512-Kbyte devices (see Table 30-8).</p> <p>Updated the Minimum value for Parameter CM34 (see Table 30-53).</p> <p>Updated the Minimum and Maximum values and the Conditions for parameter SY12 (see Table 30-22).</p>