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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc502-i-mm

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Pin Diagrams (Continued)



3.7 CPU Control Registers

R/W-0) R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0						
0A ⁽¹⁾	OB ⁽¹⁾	SA ^(1,4)	SB ^(1,4)	OAB ⁽¹⁾	SAB ⁽¹⁾	DA ⁽¹⁾	DC						
bit 15							bit 8						
R/W-0 ⁽²	R/W-0 ^(2,3)	R/W-0 ^(2,3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0						
IPL2	IPL1	IPL0	RA	N	OV	Z	С						
bit 7							bit 0						
Legend:		C = Clearable	bit										
R = Reada	able bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'							
-n = Value	e at POR	'1'= Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown						
bit 15	OA: Accumu	lator A Overflow	v Status bit ⁽¹⁾										
	1 = Accumula	ator A has over	flowed										
	0 = Accumula	ator A has not c	verflowed										
bit 14	OB: Accumu	lator B Overflov	v Status bit ⁽¹⁾										
	1 = Accumula	1 = Accumulator B has overflowed 0 = Accumulator B has not overflowed											
hit 13		lator A Saturatio	n 'Sticky' Sta	tue hit(1,4)									
DIL 15	$1 = \Delta c cumula$	ator A is saturat	ed or has her	n saturated at	some time								
	0 = Accumula	ator A is not sat	urated		Some time								
bit 12	SB: Accumu	lator B Saturatio	on 'Sticky' Sta	tus bit ^(1,4)									
	1 = Accumula	ator B is satura	ed or has bee	en saturated at	some time								
	0 = Accumula	ator B is not sat	urated										
bit 11	OAB: OA (OB Combined A	ccumulator O	verflow Status	bit ⁽¹⁾								
	1 = Accumula	ators A or B have	ve overflowed										
	0 = Neither A	Accumulators A	or B have ove	erflowed	(1)								
bit 10	SAB: SA S	B Combined A	cumulator 'Si	icky Status bit		1							
	1 = Accumula 0 = Neither A	ators A or B are	or B are satur	nave been sat	urated at some	time							
hit 9		Active hit(1)		alou									
bit 0	1 = DO loop is	s in progress											
	0 = DO loop is	s not in progres	S										
bit 8	DC: MCU AL	U Half Carry/Bo	orrow bit										
	1 = A carry-o	out from the 4th	low-order bit (for byte-sized o	data) or 8th low-	order bit (for wo	ord-sized data)						
	of the re	sult occurred											
	0 = No carry	-out from the 4	th low-order t	bit (for byte-siz	ed data) or 8th	low-order bit (1	for word-sized						
	uala) U												
Note 1:	This bit is availabl	e on dsPIC33E	PXXXMC20X	/50X and dsPl	C33EPXXXGP	50X devices on	ly.						
2:	The IPL<2:0> bits	are concatenat	ed with the IF	PL<3> bit (COR	RCON<3>) to fo	rm the CPU Inte	errupt Priority						
	Level. The value I IPL< $3 > = 1$.	n parentheses i	naicates the I	PL, IT IPL<3> =	= ⊥. User interru	ipts are disable	a wnen						

REGISTER 3-1: SR: CPU STATUS REGISTER

- 3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- **4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

TABLE 4-20: ADC1 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC1BUF0	0300		ADC1 Data Buffer 0 x2									xxxx						
ADC1BUF1	0302		ADC1 Data Buffer 1 xx											xxxx				
ADC1BUF2	0304		ADC1 Data Buffer 2 x2										xxxx					
ADC1BUF3	0306								ADC1 Data B	uffer 3								xxxx
ADC1BUF4	0308								ADC1 Data B	uffer 4								xxxx
ADC1BUF5	030A								ADC1 Data B	uffer 5								xxxx
ADC1BUF6	030C								ADC1 Data B	uffer 6								xxxx
ADC1BUF7	030E								ADC1 Data B	uffer 7								xxxx
ADC1BUF8	0310								ADC1 Data B	uffer 8								xxxx
ADC1BUF9	0312		ADC1 Data Buffer 9 x2								xxxx							
ADC1BUFA	0314								ADC1 Data Bu	uffer 10								xxxx
ADC1BUFB	0316								ADC1 Data Bu	uffer 11								xxxx
ADC1BUFC	0318								ADC1 Data Bu	uffer 12								xxxx
ADC1BUFD	031A								ADC1 Data Bu	uffer 13								xxxx
ADC1BUFE	031C								ADC1 Data Bu	uffer 14								xxxx
ADC1BUFF	031E								ADC1 Data Bu	uffer 15								xxxx
AD1CON1	0320	ADON	—	ADSIDL	ADDMABM	_	AD12B	FOR	M<1:0>		SSRC<2:0	>	SSRCG	SIMSAM	ASAM	SAMP	DONE	0000
AD1CON2	0322	,	VCFG<2:0	>	—	·	CSCNA	CHP	S<1:0>	BUFS			SMPI<4:0>	>		BUFM	ALTS	0000
AD1CON3	0324	ADRC	—	—		-	SAMC<4:0	>	_		-		ADCS	<7:0>				0000
AD1CHS123	0326	_	—	—	—	·	CH123N	NB<1:0>	CH123SB	_	—		—	—	CH123N	A<1:0>	CH123SA	0000
AD1CHS0	0328	CH0NB	—	—		CH0SB<4:0> CH0NA — — CH0SA<4:0>							0000					
AD1CSSH	032E	CSS31	CSS30	—	CSS26 CSS25 CSS24					—	0000							
AD1CSSL	0330	CSS15	CSS14	4 CSS13 CSS12 CSS11 CSS10 CSS9 CSS8 CSS7 CSS6 CSS5 CSS4 CSS3 CSS2 CSS1 CSS0 (0000							
AD1CON4	0332	_	-	-	-	—	—	_	ADDMAEN	—	—	—	—	—	D	MABL<2:	0>	0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.4 SOFTWARE STACK

The W15 register serves as a dedicated Software Stack Pointer (SSP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating of the Stack Pointer (for example, creating stack frames).

Note:	То	protec	t	agains	st	misal	lign	ed	st	ack
	acc	esses,	W	15<0>	is	fixed	to	'0'	by	the
	hard	dware.								

W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within Data Space.

The Software Stack Pointer always points to the first available free word and fills the software stack working from lower toward higher addresses. Figure 4-19 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> are pushed onto the first available stack word, then PC<22:16> are pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-19. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

- **Note 1:** To maintain system Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging, and is therefore restricted to an address range of 0x0000 to 0xFFFF. The same applies to the W14 when used as a Stack Frame Pointer (SFA = 1).
 - 2: As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a C development environment

FIGURE 4-19: CALL STACK FRAME



10.2.1 SLEEP MODE

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- · Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into Standby when Sleep mode is entered by clearing the VREGS (RCON<8>) and VREGSF (RCON<11>) bits (default configuration).

If the application requires a faster wake-up time, and can accept higher current requirements, the VREGS (RCON<8>) and VREGSF (RCON<11>) bits can be set to keep the internal regulator and the Flash regulator active during Sleep mode.

10.2.2 IDLE MODE

The following occurs in Idle mode:

- The CPU stops executing instructions.
- · The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see Section 10.4 "Peripheral Module Disable").
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- · Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction or the first instruction in the Interrupt Service Routine (ISR).

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral; for example, the TSIDL bit in the Timer1 Control register (T1CON<13>).

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

REGISTER 11-8: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				QEB1R<6:0>	•		
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				QEA1R<6:0>	•		
bit 7							bit 0
Legend:	-1:+		L 14				
R = Readad		vv = vvritable	DIT		nented bit, rea		
-n = Value a	at POR	'1' = Bit is set		0^{\prime} = Bit is clea	ared	x = Bit is unkr	nown
bit 15	Unimplome	ntod: Dood os '	o'				
		nteu: Reau as			- Dia kita		
DIL 14-8	(see Table 1	J>: Assign B (QE 11-2 for input pin	selection nur	nbers)	n Pin dits		
	1111001 =	Input tied to RPI	121				
	•						
	•						
	0000001 =	Input tied to CM	P1				
	0000000 =	Input tied to Vss	;				
bit 7	Unimpleme	ented: Read as '	0'				
bit 6-0	QEA1R<6:0	D>: Assign A (QE	A) to the Cor	responding RP	n Pin bits		
	(see Table ?	11-2 for input pin	selection nur	nbers)			
	1111001 =	Input tied to RPI	121				
	•						
	0000001 =	Input tied to CM	P1				
	0000000 =	Input tied to Vss	;				

12.2 Timer1 Control Register

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON ⁽¹⁾	—	TSIDL	—	_	—	—	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	TCKPS1	TCKPS0	_	TSYNC ⁽¹⁾	TCS ⁽¹⁾	—
bit 7							bit 0
Legend:							
R = Readab	ole bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own
		(1)					
bit 15	TON: Timer1	On bit ⁽¹⁾					
	1 = Starts 16-	bit Limer1 bit Timer1					
bit 1/	Unimplement	ted: Pead as '	ı'				
bit 13		1 Stop in Idle N	/ode hit				
DIC 15	1 = Discontinu	i stop in lae k	eration when a	device enters l	dle mode		
	0 = Continues	module opera	tion in Idle mo	ode			
bit 12-7	Unimplement	ted: Read as ')'				
bit 6	TGATE: Time	r1 Gated Time	Accumulation	Enable bit			
	When TCS =	<u>1:</u> prod					
	When TCS =	0. 0.					
	1 = Gated tim	<u>e</u> accumulatior	n is enabled				
	0 = Gated tim	e accumulatior	n is disabled				
bit 5-4	TCKPS<1:0>	: Timer1 Input	Clock Prescal	e Select bits			
	11 = 1:256						
	10 = 1:64 01 = 1:8						
	01 = 1.0 00 = 1.1						
bit 3	Unimplement	ted: Read as ')'				
bit 2	TSYNC: Time	er1 External Clo	ock Input Sync	chronization Se	elect bit ⁽¹⁾		
	When TCS =	1:					
	1 = Synchroni	izes external cl	ock input				
	0 = Does not	synchronize ex	ternal clock in	nput			
	This bit is jand	<u>ored</u> .					
bit 1	TCS: Timer1 (Clock Source S	Select bit ⁽¹⁾				
	1 = External c	lock is from pir	n, T1CK (on th	ne rising edge)			
	0 = Internal cl	ock (FP)		5 5-7			
bit 0	Unimplement	ted: Read as ')'				
Note 1: \	When Timer1 is en attempts by user so	abled in Exterr oftware to write	al Synchrono to the TMR1	us Counter mo register are ig	ode (TCS = 1, T nored.	SYNC = 1, TO	N = 1), any

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

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REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER (CONTINUED)

- bit 2 INDEX: Status of INDXx Input Pin After Polarity Control
 - 1 = Pin is at logic '1'
 - 0 = Pin is at logic '0'
- bit 1 QEB: Status of QEBx Input Pin After Polarity Control And SWPAB Pin Swapping 1 = Pin is at logic '1' 0 = Pin is at logic '0'
- bit 0 **QEA:** Status of QEAx Input Pin After Polarity Control And SWPAB Pin Swapping 1 = Pin is at logic '1'
 - 0 = Pin is at logic '0'

REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER (CONTINUED)

- bit 1 **RBIF:** RX Buffer Interrupt Flag bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 0 **TBIF:** TX Buffer Interrupt Flag bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0		—
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15	EDG1MOD: E	Edge 1 Edge Sa	ampling Mode	Selection bit			
	1 = Edge 1 is	edge-sensitive	9				
h:+ 4 4		s level-sensitive					
DIT 14	EDG1POL: E	dge 1 Polarity	Select Dit	dao roopopoo			
	1 = Edge 1 is $0 = Edge 1$ is	s programmed f	or a positive e	edae response			
bit 13-10	EDG1SEL<3:	:0>: Edae 1 So	urce Select bits	3			
	1xxx = Rese	rved					
	01xx = Reser	rved					
	0011 = CTED)1 pin					
	0010 = CTEL	module					
	0000 = Timer	1 module					
bit 9	EDG2STAT: E	Edge 2 Status b	it				
	Indicates the	status of Edge	2 and can be v	vritten to contro	ol the edge sou	rce.	
	1 = Edge 2h	as occurred	J				
hit Q] ;+				
DILO	EDGISIAI: E	status of Edge	il 1 and can be y	written to contro	the edge sou	rce	
	1 = Edge 1 h	as occurred			i the edge sou	ice.	
	0 = Edge 1 h	as not occurred	t				
bit 7	EDG2MOD: E	Edge 2 Edge Sa	ampling Mode	Selection bit			
	1 = Edge 2 is	edge-sensitive	9				
	0 = Edge 2 is	s level-sensitive					
bit 6	EDG2POL: E	dge 2 Polarity	Select bit				
	1 = Edge 2 Is 0 = Edge 2 is	s programmed i	or a positive e	age response			
bit 5-2	EDG2SEL<3:	:0>: Edge 2 So	urce Select bits	8			
	1111 = Reser	rved		-			
	01xx = Reser	rved					
	0100 = CMP1	1 module					
	0011 = CIEL 0010 = CTFF	o∠ pin)1 pin					
	0001 = OC1	module					
	0000 = IC1 m	nodule					
bit 1-0	Unimplemen	ted: Read as ')'				

REGISTER 22-2: CTMUCON2: CTMU CONTROL REGISTER 2

REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)

bit 4-0	CH0SA<4:0>: Channel 0 Positive Input Select for Sample MUXA bits ⁽¹⁾
	11111 = Open; use this selection with CTMU capacitive and time measurement
	11110 = Channel 0 positive input is connected to the CTMU temperature measurement diode (CTMU TEMP)
	11101 = Reserved
	11011 = Reserved
	11010 = Channel 0 positive input is the output of OA3/AN6 ^(2,3)
	11001 = Channel 0 positive input is the output of OA2/AN0 ⁽²⁾
	11000 = Channel 0 positive input is the output of OA1/AN3 ⁽²⁾
	10110 = Reserved
	•
	•
	10000 = Reserved
	01111 = Channel 0 positive input is $AN15^{(1,3)}$
	01110 = Channel 0 positive input is AN14 ^(1,3)
	•
	•
	00010 = Channel 0 positive input is AN2 ^(1,3)
	00001 = Channel 0 positive input is AN0(1,3)

- **Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.
 - 2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.
 - 3: See the "Pin Diagrams" section for the available analog channels for each device.

REGISTER 24-8: PTGC1LIM: PTG COUNTER 1 LIMIT REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC1L	IM<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC1L	_IM<7:0>			
bit 7							bit 0
Logond							

Legenu.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGC1LIM<15:0>:** PTG Counter 1 Limit Register bits May be used to specify the loop count for the PTGJMPC1 Step command or as a limit register for the General Purpose Counter 1.

REGISTER 24-9: PTGHOLD: PTG HOLD REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGHOL	_D<15:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGHO	LD<7:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGHOLD<15:0>:** PTG General Purpose Hold Register bits Holds user-supplied data to be copied to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGCOPY command.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

bit 3-0	Step Command	OPTION<3:0>	Option Description						
	PTGWHI(1)	0000	PWM Special Event Trigger. ⁽³⁾						
	or	0001	PWM master time base synchronization output. ⁽³⁾						
	P.I.GWLO(''	0010	PWM1 interrupt. ⁽³⁾						
		0011	PWM2 interrupt. ⁽³⁾						
		0100	PWM3 interrupt. ⁽³⁾						
		0101	Reserved.						
		0110	Reserved.						
		0111	OC1 Trigger event.						
		1000	OC2 Trigger event.						
		1001	IC1 Trigger event.						
		1010	CMP1 Trigger event.						
		1011	CMP2 Trigger event.						
		1100	CMP3 Trigger event.						
		1101	CMP4 Trigger event.						
		1110	ADC conversion done interrupt.						
		1111	INT2 external interrupt.						
	PTGIRQ(1)	0000	Generate PTG Interrupt 0.						
		0001	Generate PTG Interrupt 1.						
		0010	Generate PTG Interrupt 2.						
		0011	Generate PTG Interrupt 3.						
		0100	Reserved.						
		•	•						
		•	•						
		•	•						
	(2)	1111	Reserved.						
	PTGTRIG ⁽²⁾	00000	PTGO0.						
		00001	PTGO1.						
		•	•						
		•	•						
		•							
		11110	PTGO30.						
		11111	PTGO31.						

TABLE 24-1: PTG STEP COMMAND FORMAT (CONTINUED)

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 24-2 for the trigger output descriptions.

3: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

REGISTER 25-5:	CMxMSKCON: COMPARATOR x MASK GATING
	CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS		OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7							bit 0
Legend							
R = Readable	e hit	W = Writable	hit	= Inimple	mented hit read	1 as '0'	
n = Value at	POR	'1' = Rit is set		(0) = 0	eared	x = Ritis unk	nown
	1010	1 - Dit 13 3C			carca		nown
bit 15	HLMS: Hiah	or Low-Level	/asking Select	bits			
	1 = The mask	king (blanking)	function will pre	event any asse	erted ('0') compa	rator signal fro	m propagating
	0 = The mas	king (blanking)	function will pre	event any asse	erted ('1') compa	rator signal fro	m propagating
bit 14	Unimpleme	nted: Read as	'0'				
bit 13	OCEN: OR (Gate C Input Er	nable bit				
	1 = MCI is co	onnected to OF	t gate				
	0 = MCI is no	ot connected to	OR gate				
bit 12	OCNEN: OR	Gate C Input	nverted Enable	e bit			
	1 = Inverted	MCI is connect	ed to OR gate	ate			
hit 11		Sate B Input Fr	heeled to on g	juic			
bit II	1 = MBI is co	onnected to OR	aate				
	0 = MBI is no	ot connected to	OR gate				
bit 10	OBNEN: OR	Gate B Input I	nverted Enable	e bit			
	1 = Inverted	MBI is connect	ed to OR gate				
	0 = Inverted	MBI is not con	nected to OR g	jate			
bit 9	OAEN: OR (Gate A Input Er	nable bit				
	1 = MAI is co	onnected to OF	l gate				
hit 8			Norted Enable	o hit			
DILO	1 = Inverted	MAL is connect	red to OR date				
	0 = Inverted	MAI is not con	nected to OR g	gate			
bit 7	NAGS: AND	Gate Output In	nverted Enable	e bit			
	1 = Inverted	ANDI is conne	cted to OR gat	e			
	0 = Inverted	ANDI is not co		gate			
bit 6	PAGS: AND Gate Output Enable bit						
	1 = ANDI is 0 0 = ANDI is r	not connected to O	to OR gate				
bit 5	ACEN: AND	Gate C Input E	Enable bit				
	1 = MCI is co	onnected to AN	D gate				
	0 = MCI is no	ot connected to	AND gate				
bit 4	ACNEN: AN	D Gate C Input	Inverted Enab	ole bit			
	1 = Inverted	MCI is connect	ed to AND gat	e,			
	0 = Inverted	MCI is not con	nected to AND	gate			

27.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a То comprehensive reference source. complement the information in this data sheet, refer to the related section of the "dsPIC33/PIC24 Familv Reference Manual', which is available from the Microchip web site (www.microchip.com).

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard[™] Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming[™] (ICSP[™])
- In-Circuit Emulation

27.1 Configuration Bits

In dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored in at the top of the on-chip program memory space, known as the Flash Configuration bytes. Their specific locations are shown in Table 27-1. The configuration data is automatically loaded from the Flash Configuration bytes to the proper Configuration Shadow registers during device Resets.

Note:	Configuration data is reloaded on all types
	of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration bytes for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled.

The upper 2 bytes of all Flash Configuration Words in program memory should always be '1111 1111 1111 1111 1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '1's to these locations has no effect on device operation.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

The Configuration Flash bytes map is shown in Table 27-1.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 27-1: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R	R	R
			DEVID<2	3:16> (1)			
bit 23							bit 16
R	R	R	R	R	R	R	R
			DEVID<	15:8> (1)			
bit 15							bit 8
R	R	R	R	R	R	R	R
			DEVID<	7:0> ⁽¹⁾			
bit 7							bit 0
Legend:	R = Read-Only bit			U = Unimplen	nented bit		

bit 23-0 **DEVID<23:0>:** Device Identifier bits⁽¹⁾

Note 1: Refer to the "dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration *Bits*" (DS70663) for the list of device ID values.

REGISTER 27-2: DEVREV: DEVICE REVISION REGISTER

R	R	R	R	R	R	R	R
			DEVREV<	<23:16> ⁽¹⁾			
bit 23							bit 16
R	R	R	R	R	R	R	R
			DEVREV	<15:8> (1)			
bit 15							bit 8
R	R	R	R	R	R	R	R
			DEVRE	/<7:0> ⁽¹⁾			
bit 7							bit 0
Legend:	R = Read-only bit			U = Unimpler	nented bit		

bit 23-0 **DEVREV<23:0>:** Device Revision bits⁽¹⁾

Note 1: Refer to the "dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration *Bits*" (DS70663) for the list of device revision values.

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
1	ADD	ADD	Acc ⁽¹⁾	Add Accumulators	1	1	OA,OB,SA,SB
		ADD	f	f = f + WREG	1	1	C,DC,N,OV,Z
		ADD	f,WREG	WREG = f + WREG	1	1	C,DC,N,OV,Z
		ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z
		ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z
		ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z
		ADD	Wso,#Slit4,Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC	f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	f,WREG	WREG = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	#lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z
3	AND	AND	f	f = f .AND. WREG	1	1	N,Z
		AND	f,WREG	WREG = f .AND. WREG	1	1	N,Z
		AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N,Z
		AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N,Z
		AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N,Z
4	ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z
		ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z
		ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z
5	BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
		BCLR	Ws,#bit4	Bit Clear Ws	1	1	None
6	BRA	BRA	C,Expr	Branch if Carry	1	1 (4)	None
		BRA	GE, Expr	Branch if greater than or equal	1	1 (4)	None
		BRA	GEU, Expr	Branch if unsigned greater than or equal	1	1 (4)	None
		BRA	GT, Expr	Branch if greater than	1	1 (4)	None
		BRA	GTU, Expr	Branch if unsigned greater than	1	1 (4)	None
		BRA	LE, Expr	Branch if less than or equal	1	1 (4)	None
		BRA	LEU, Expr	Branch if unsigned less than or equal	1	1 (4)	None
		BRA	LT,Expr	Branch if less than	1	1 (4)	None
		BRA	LTU, Expr	Branch if unsigned less than	1	1 (4)	None
		BRA	N,Expr	Branch if Negative	1	1 (4)	None
		BRA	NC, Expr	Branch if Not Carry	1	1 (4)	None
		BRA	NN, Expr	Branch if Not Negative	1	1 (4)	None
		BRA	NOV, Expr	Branch if Not Overflow	1	1 (4)	None
		BRA	NZ,Expr	Branch if Not Zero	1	1 (4)	None
		BRA	OA, Expr(1)	Branch if Accumulator A overflow	1	1 (4)	None
		BRA	OB, Expr(1)	Branch if Accumulator B overflow	1	1 (4)	None
		BRA	OV, Expr(1)	Branch if Overflow	1	1 (4)	None
		BRA	SA, Expr(1)	Branch if Accumulator A saturated	1	1 (4)	None
		BRA	SB, Expr(1)	Branch if Accumulator B saturated	1	1 (4)	None
		BRA	Expr	Branch Unconditionally	1	4	None
		BRA	Z,Expr	Branch if Zero	1	1 (4)	None
L		BRA	Wn	Computed Branch	1	4	None
7	BSET	BSET	f,#bit4	Bit Set f	1	1	None
		BSET	Ws,#bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C	Ws,Wb	Write C bit to Ws <wb></wb>	1	1	None
		BSW.Z	Ws,Wb	Write Z bit to Ws <wb></wb>	1	1	None

TABLE 28-2: INSTRUCTION SET OVERVIEW

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

DC CHARACTERISTICS			Standard Oper (unless otherw Operating temp	ating Conditions: 3.0V t rise stated) perature $-40^{\circ}C \le TA \le +8$ $-40^{\circ}C \le TA \le +7$	o 3.6V 35°C for Industrial 125°C for Extended		
Parameter No.	Тур.	Max.	Units	Units Conditions			
DC61d	8		μΑ	-40°C			
DC61a	10	—	μA	+25°C			
DC61b	12	_	μA	+85°C 3.3V			
DC61c	13		μA +125°C				

TABLE 30-9: DC CHARACTERISTICS: WATCHDOG TIMER DELTA CURRENT (Δ Iwdt)⁽¹⁾

Note 1: The \triangle IwDT current is the additional current consumed when the module is enabled. This current should be added to the base IPD current. All parameters are characterized but not tested during manufacturing.

TABLE 30-10: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

DC CHARACTER	Standard C (unless oth Operating to	perating erwise st emperatur	Condition ated) e -40°C -40°C	s: 3.0V to ≤ Ta ≤ +8 ≤ Ta ≤ +1	3.6V 5°C for Industrial 25°C for Extended				
Parameter No.	Тур.	Max.	Doze Ratio	Units	Conditions				
Doze Current (IDOZE) ⁽¹⁾									
DC73a ⁽²⁾	35	_	1:2	mA	40°C	3.3V	Fosc = 140 MHz		
DC73g	20	30	1:128	mA	-40 C				
DC70a ⁽²⁾	35	—	1:2	mA	+25%	2 21/	E000 - 140 MH7		
DC70g	20	30	1:128	mA	720 C	3.3V	FUSC = 140 MHZ		
DC71a ⁽²⁾	35	—	1:2	mA	+95°C	2 21/	E000 - 140 MHz		
DC71g	20	30	1:128	mA	+05 C	3.3V	FUSC = 140 MHZ		
DC72a ⁽²⁾	28	_	1:2	mA	±125°C	3 3//	Fosc = 120 MHz		
DC72g	15	30	1:128	mA	+120 C	3.3V			

Note 1: IDOZE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDOZE measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- · All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- CPU is executing while(1) statement
- · JTAG is disabled
- 2: Parameter is characterized but not tested in manufacturing.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

FIGURE 30-6: INPUT CAPTURE x (ICx) TIMING CHARACTERISTICS



TABLE 30-26: INPUT CAPTURE x MODULE TIMING REQUIREMENTS

АС СНА	RACTERI	STICS	Standard Operati (unless otherwise Operating temperation	ng Con e stated ature	ditions:) -40°C ≤ -40°C ≤	3.0V to 3.6V TA \leq +85°C for Indu TA \leq +125°C for Ext	strial ended	
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Max.	Units	Conditions		
IC10	TccL	ICx Input Low Time	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	—	ns	Must also meet Parameter IC15		
IC11	ТссН	ICx Input High Time	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	—	ns	Must also meet Parameter IC15	N = prescale value (1, 4, 16)	
IC15	TccP	ICx Input Period	Greater of 25 + 50 or (1 Tcy/N) + 50	_	ns			

Note 1: These parameters are characterized, but not tested in manufacturing.

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DC CHARACT	ERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				0V to 3.6V ≤ +150°C	
Parameter No.	Typical	Max	Units	Conditions			
Power-Down	Current (IPD)						
HDC60e	1400	2500	μA	+150°C 3.3V Base Power-Down Current (Notes 1, 3)			
HDC61c	15	—	μA	+150°C	3.3V	Watchdog Timer Current: ∆IWDT (Notes 2, 4)	

TABLE 31-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

Note 1: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled to Vss. WDT, etc., are all switched off and VREGS (RCON<8>) = 1.

2: The ∆ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

3: These currents are measured on the device containing the most memory in this family.

4: These parameters are characterized, but are not tested in manufacturing.

TABLE 31-5: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				
Parameter No.	Typical	Max	Units	Conditions			
HDC44e	12	30	mA	+150°C	3.3V	40 MIPS	

TABLE 31-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				
Parameter No.	Typical	Мах	Units	Conditions			
HDC20	9	15	mA	+150°C	3.3V	10 MIPS	
HDC22	16	25	mA	+150°C	3.3V	20 MIPS	
HDC23	30	50	mA	+150°C	3.3V	40 MIPS	

TABLE 31-7: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				
Parameter No.	Typical	Мах	Doze Ratio	Units	Conditions		
HDC72a	24	35	1:2	mA			
HDC72f ⁽¹⁾	14	—	1:64	mA	+150°C	3.3V	40 MIPS
HDC72g ⁽¹⁾	12	_	1:128	mA			

Note 1: Parameters with Doze ratios of 1:64 and 1:128 are characterized, but are not tested in manufacturing.