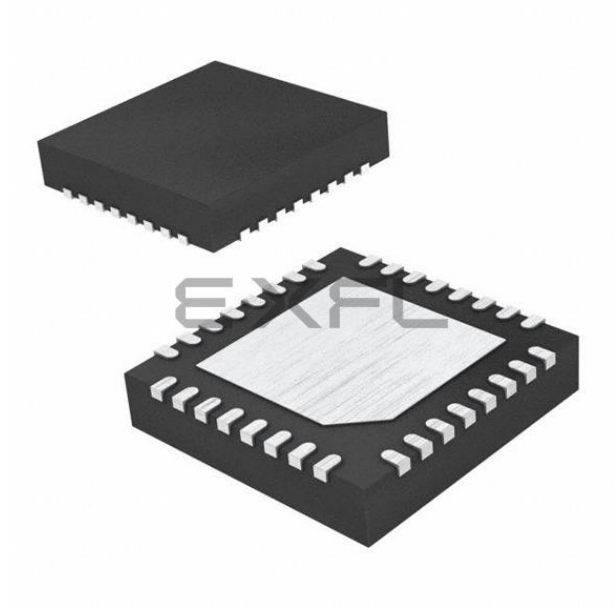
# Microchip Technology - DSPIC33EP512MC502T-I/MM Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

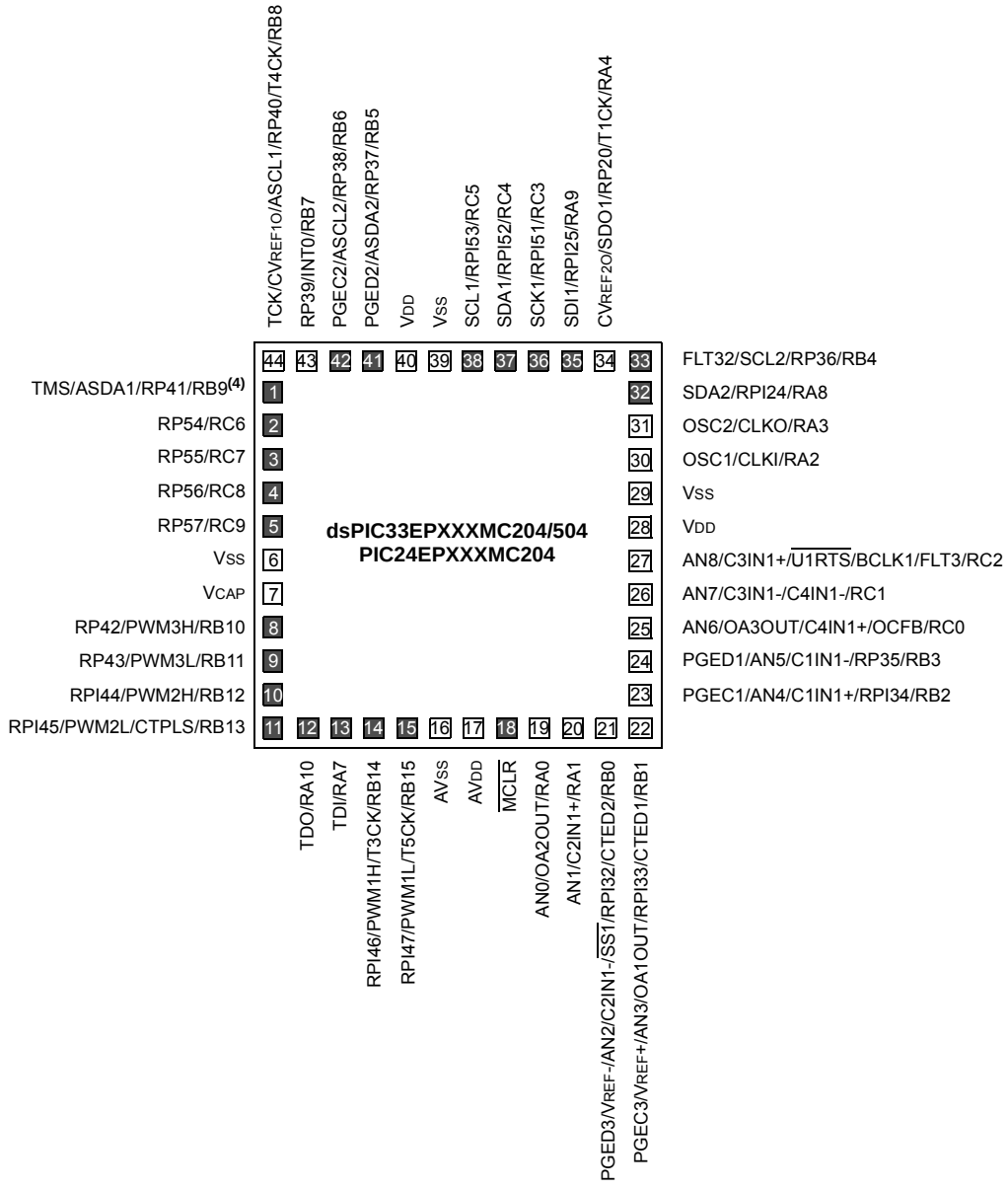
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 512KB (170K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 24K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 6x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VQFN Exposed Pad |
| Supplier Device Package | 28-QFN-S (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc502t-i-mm |

## Pin Diagrams (Continued)

**44-Pin VTLA(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

**TABLE 4-2: CPU CORE REGISTER MAP FOR PIC24EPXXXGP/MC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W0 | 0000 | W0 (WREG) | | | | | | | | | | | | | | | | xxxx |
| W1 | 0002 | W1 | | | | | | | | | | | | | | | | xxxx |
| W2 | 0004 | W2 | | | | | | | | | | | | | | | | xxxx |
| W3 | 0006 | W3 | | | | | | | | | | | | | | | | xxxx |
| W4 | 0008 | W4 | | | | | | | | | | | | | | | | xxxx |
| W5 | 000A | W5 | | | | | | | | | | | | | | | | xxxx |
| W6 | 000C | W6 | | | | | | | | | | | | | | | | xxxx |
| W7 | 000E | W7 | | | | | | | | | | | | | | | | xxxx |
| W8 | 0010 | W8 | | | | | | | | | | | | | | | | xxxx |
| W9 | 0012 | W9 | | | | | | | | | | | | | | | | xxxx |
| W10 | 0014 | W10 | | | | | | | | | | | | | | | | xxxx |
| W11 | 0016 | W11 | | | | | | | | | | | | | | | | xxxx |
| W12 | 0018 | W12 | | | | | | | | | | | | | | | | xxxx |
| W13 | 001A | W13 | | | | | | | | | | | | | | | | xxxx |
| W14 | 001C | W14 | | | | | | | | | | | | | | | | xxxx |
| W15 | 001E | W15 | | | | | | | | | | | | | | | | xxxx |
| SPLIM | 0020 | SPLIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PCL | 002E | PCL<15:1> | | | | | | | | | | | | | | | — | 0000 |
| PCH | 0030 | — | — | — | — | — | — | — | — | — | PCH<6:0> | | | | | | | 0000 |
| DSRPAG | 0032 | — | — | — | — | — | — | DSRPAG<9:0> | | | | | | | | | | 0001 |
| DSWPAG | 0034 | — | — | — | — | — | — | — | DSWPAG<8:0> | | | | | | | | | 0001 |
| RCOUNT | 0036 | RCOUNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| SR | 0042 | — | — | — | — | — | — | — | DC | IPL2 | IPL1 | IPL0 | RA | N | OV | Z | C | 0000 |
| CORCON | 0044 | VAR | — | — | — | — | — | — | — | — | — | — | — | IPL3 | SFA | — | — | 0020 |
| DISICNT | 0052 | — | — | DISICNT<13:0> | | | | | | | | | | | | | | 0000 |
| TBLPAG | 0054 | — | — | — | — | — | — | — | — | TBLPAG<7:0> | | | | | | | | 0000 |
| MSTRPR | 0058 | MSTRPR<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IFS0 | 0800 | — | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | — | — | — | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | — | — | — | — | — | — | — | — | — | IC4IF | IC3IF | DMA3IF | C1IF | C1RXIF | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | — | — | — | — | — | QEI1IF | PSEMIF | — | — | — | — | — | — | MI2C2IF | SI2C2IF | — | 0000 |
| IFS4 | 0808 | — | — | CTMUIF | — | — | — | — | — | — | C1TXIF | — | — | CRCIF | U2EIF | U1EIF | — | 0000 |
| IFS5 | 080A | PWM2IF | PWM1IF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS6 | 080C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IF | 0000 |
| IFS8 | 0810 | JTAGIF | ICDIF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS9 | 0812 | — | — | — | — | — | — | — | — | — | PTG3IF | PTG2IF | PTG1IF | PTG0IF | PTGWDTIF | PTGSTEPIF | — | 0000 |
| IEC0 | 0820 | — | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | — | — | — | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | — | — | — | — | — | — | — | — | — | IC4IE | IC3IE | DMA3IE | C1IE | C1RXIE | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | — | — | — | — | — | QEI1IE | PSEMIE | — | — | — | — | — | — | MI2C2IE | SI2C2IE | — | 0000 |
| IEC4 | 0828 | — | — | CTMUIE | — | — | — | — | — | — | C1TXIE | — | — | CRCIE | U2EIE | U1EIE | — | 0000 |
| IEC5 | 082A | PWM2IE | PWM1IE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC6 | 082C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IE | 0000 |
| IEC7 | 082E | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC8 | 0830 | JTAGIE | ICDIE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC9 | 0832 | — | — | — | — | — | — | — | — | — | PTG3IE | PTG2IE | PTG1IE | PTG0IE | PTGWDTIE | PTGSTEPIE | — | 0000 |
| IPC0 | 0840 | — | T1IP<2:0> | | | — | OC1IP<2:0> | | | — | IC1IP<2:0> | | | — | INT0IP<2:0> | | | 4444 |
| IPC1 | 0842 | — | T2IP<2:0> | | | — | OC2IP<2:0> | | | — | IC2IP<2:0> | | | — | DMA0IP<2:0> | | | 4444 |
| IPC2 | 0844 | — | U1RXIP<2:0> | | | — | SPI1IP<2:0> | | | — | SPI1EIP<2:0> | | | — | T3IP<2:0> | | | 4444 |
| IPC3 | 0846 | — | — | — | — | — | DMA1IP<2:0> | | | — | AD1IP<2:0> | | | — | U1TXIP<2:0> | | | 0444 |
| IPC4 | 0848 | — | CNIP<2:0> | | | — | CMIP<2:0> | | | — | MI2C1IP<2:0> | | | — | SI2C1IP<2:0> | | | 4444 |
| IPC5 | 084A | — | — | — | — | — | — | — | — | — | — | — | — | — | INT1IP<2:0> | | | 0004 |
| IPC6 | 084C | — | T4IP<2:0> | | | — | OC4IP<2:0> | | | — | OC3IP<2:0> | | | — | DMA2IP<2:0> | | | 4444 |
| IPC7 | 084E | — | U2TXIP<2:0> | | | — | U2RXIP<2:0> | | | — | INT2IP<2:0> | | | — | T5IP<2:0> | | | 4444 |
| IPC8 | 0850 | — | C1IP<2:0> | | | — | C1RXIP<2:0> | | | — | SPI2IP<2:0> | | | — | SPI2EIP<2:0> | | | 4444 |
| IPC9 | 0852 | — | — | — | — | — | IC4IP<2:0> | | | — | IC3IP<2:0> | | | — | DMA3IP<2:0> | | | 0444 |
| IPC12 | 0858 | — | — | — | — | — | MI2C2IP<2:0> | | | — | SI2C2IP<2:0> | | | — | — | — | — | 0440 |
| IPC14 | 085C | — | — | — | — | — | QEI1IP<2:0> | | | — | PSEMIP<2:0> | | | — | — | — | — | 0440 |
| IPC16 | 0860 | — | CRCIP<2:0> | | | — | U2EIP<2:0> | | | — | U1EIP<2:0> | | | — | — | — | — | 4440 |
| IPC17 | 0862 | — | — | — | — | — | C1TXIP<2:0> | | | — | — | — | — | — | — | — | — | 0400 |
| IPC19 | 0866 | — | — | — | — | — | — | — | — | — | CTMUIP<2:0> | | | — | — | — | — | 0040 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-14: PWM GENERATOR 2 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWMCON2 | 0C40 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC<1:0> | | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON2 | 0C42 | PENH | PENL | POLH | POLL | PMOD<1:0> | | OVRENH | OVRENL | OVRDAT<1:0> | | FLTDAT<1:0> | | CLDAT<1:0> | | SWAP | OSYNC | C000 |
| FCLCON2 | 0C44 | — | CLSRC<4:0> | | | | | CLPOL | CLMOD | FLTSRC<4:0> | | | | | FLTPOL | FLTMOD<1:0> | | 00F8 |
| PDC2 | 0C46 | PDC2<15:0> | | | | | | | | | | | | | | | | 0000 |
| PHASE2 | 0C48 | PHASE2<15:0> | | | | | | | | | | | | | | | | 0000 |
| DTR2 | 0C4A | — | — | DTR2<13:0> | | | | | | | | | | | | | | 0000 |
| ALTDTR2 | 0C4C | — | — | ALTDTR2<13:0> | | | | | | | | | | | | | | 0000 |
| TRIG2 | 0C52 | TRGCMP<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRGCON2 | 0C54 | TRGDIV<3:0> | | | | — | — | — | — | — | — | TRGSTRT<5:0> | | | | | | 0000 |
| LEBCON2 | 0C5A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY2 | 0C5C | — | — | — | — | LEB<11:0> | | | | | | | | | | | | 0000 |
| AUXCON2 | 0C5E | — | — | — | — | BLANKSEL<3:0> | | | | — | — | CHOPSEL<3:0> | | | | CHOPHEN | CHOPLEN | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-15: PWM GENERATOR 3 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWMCON3 | 0C60 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC<1:0> | | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON3 | 0C62 | PENH | PENL | POLH | POLL | PMOD<1:0> | | OVRENH | OVRENL | OVRDAT<1:0> | | FLTDAT<1:0> | | CLDAT<1:0> | | SWAP | OSYNC | C000 |
| FCLCON3 | 0C64 | — | CLSRC<4:0> | | | | | CLPOL | CLMOD | FLTSRC<4:0> | | | | | FLTPOL | FLTMOD<1:0> | | 00F8 |
| PDC3 | 0C66 | PDC3<15:0> | | | | | | | | | | | | | | | | 0000 |
| PHASE3 | 0C68 | PHASE3<15:0> | | | | | | | | | | | | | | | | 0000 |
| DTR3 | 0C6A | — | — | DTR3<13:0> | | | | | | | | | | | | | | 0000 |
| ALTDTR3 | 0C6C | — | — | ALTDTR3<13:0> | | | | | | | | | | | | | | 0000 |
| TRIG3 | 0C72 | TRGCMP<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRGCON3 | 0C74 | TRGDIV<3:0> | | | | — | — | — | — | — | — | TRGSTRT<5:0> | | | | | | 0000 |
| LEBCON3 | 0C7A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY3 | 0C7C | — | — | — | — | LEB<11:0> | | | | | | | | | | | | 0000 |
| AUXCON3 | 0C7E | — | — | — | — | BLANKSEL<3:0> | | | | — | — | CHOPSEL<3:0> | | | | CHOPHEN | CHOPLEN | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-24: CRC REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CRCCON1 | 0640 | CRCEN | — | CSIDL | VWORD<4:0> | | | | | CRCFUL | CRCMPT | CRCISEL | CRCGO | LENDIAN | — | — | — | 0000 |
| CRCCON2 | 0642 | — | — | — | DWIDTH<4:0> | | | | | — | — | — | PLEN<4:0> | | | | | 0000 |
| CRCXORL | 0644 | X<15:1> | | | | | | | | | | | | | | | — | 0000 |
| CRCXORH | 0646 | X<31:16> | | | | | | | | | | | | | | | | 0000 |
| CRCDATL | 0648 | CRC Data Input Low Word | | | | | | | | | | | | | | | | 0000 |
| CRCDATH | 064A | CRC Data Input High Word | | | | | | | | | | | | | | | | 0000 |
| CRCWDATL | 064C | CRC Result Low Word | | | | | | | | | | | | | | | | 0000 |
| CRCWDATH | 064E | CRC Result High Word | | | | | | | | | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Shaded bits are not used in the operation of the programmable CRC module.

**TABLE 4-25: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC202/502 AND PIC24EPXXXGP/MC202 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPOR0 | 0680 | — | — | RP35R<5:0> | | | | | | — | — | RP20R<5:0> | | | | | | 0000 |
| RPOR1 | 0682 | — | — | RP37R<5:0> | | | | | | — | — | RP36R<5:0> | | | | | | 0000 |
| RPOR2 | 0684 | — | — | RP39R<5:0> | | | | | | — | — | RP38R<5:0> | | | | | | 0000 |
| RPOR3 | 0686 | — | — | RP41R<5:0> | | | | | | — | — | RP40R<5:0> | | | | | | 0000 |
| RPOR4 | 0688 | — | — | RP43R<5:0> | | | | | | — | — | RP42R<5:0> | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-26: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC203/503 AND PIC24EPXXXGP/MC203 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPOR0 | 0680 | — | — | RP35R<5:0> | | | | | | — | — | RP20R<5:0> | | | | | | 0000 |
| RPOR1 | 0682 | — | — | RP37R<5:0> | | | | | | — | — | RP36R<5:0> | | | | | | 0000 |
| RPOR2 | 0684 | — | — | RP39R<5:0> | | | | | | — | — | RP38R<5:0> | | | | | | 0000 |
| RPOR3 | 0686 | — | — | RP41R<5:0> | | | | | | — | — | RP40R<5:0> | | | | | | 0000 |
| RPOR4 | 0688 | — | — | RP43R<5:0> | | | | | | — | — | RP42R<5:0> | | | | | | 0000 |
| RPOR5 | 068A | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| RPOR6 | 068C | — | — | — | — | — | — | — | — | — | — | RP56R<5:0> | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-31: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | — | — | — | — | — | — | — | — | INT2R<6:0> | | | | | | | 0000 |
| RPINR3 | 06A6 | — | — | — | — | — | — | — | — | — | T2CKR<6:0> | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R<6:0> | | | | | | | — | IC1R<6:0> | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R<6:0> | | | | | | | — | IC3R<6:0> | | | | | | | 0000 |
| RPINR11 | 06B6 | — | — | — | — | — | — | — | — | — | OCFAR<6:0> | | | | | | | 0000 |
| RPINR18 | 06C4 | — | — | — | — | — | — | — | — | — | U1RXR<6:0> | | | | | | | 0000 |
| RPINR19 | 06C6 | — | — | — | — | — | — | — | — | — | U2RXR<6:0> | | | | | | | 0000 |
| RPINR22 | 06CC | — | SCK2INR<6:0> | | | | | | | — | SDI2R<6:0> | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R<6:0> | | | | | | | 0000 |
| RPINR26 | 06D4 | — | — | — | — | — | — | — | — | — | C1RXR<6:0> | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-32: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | — | — | — | — | — | — | — | — | INT2R<6:0> | | | | | | | 0000 |
| RPINR3 | 06A6 | — | — | — | — | — | — | — | — | — | T2CKR<6:0> | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R<6:0> | | | | | | | — | IC1R<6:0> | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R<6:0> | | | | | | | — | IC3R<6:0> | | | | | | | 0000 |
| RPINR11 | 06B6 | — | — | — | — | — | — | — | — | — | OCFAR<6:0> | | | | | | | 0000 |
| RPINR12 | 06B8 | — | FLT2R<6:0> | | | | | | | — | FLT1R<6:0> | | | | | | | 0000 |
| RPINR14 | 06BC | — | QEB1R<6:0> | | | | | | | — | QEA1R<6:0> | | | | | | | 0000 |
| RPINR15 | 06BE | — | HOME1R<6:0> | | | | | | | — | INDX1R<6:0> | | | | | | | 0000 |
| RPINR18 | 06C4 | — | — | — | — | — | — | — | — | — | U1RXR<6:0> | | | | | | | 0000 |
| RPINR19 | 06C6 | — | — | — | — | — | — | — | — | — | U2RXR<6:0> | | | | | | | 0000 |
| RPINR22 | 06CC | — | SCK2INR<6:0> | | | | | | | — | SDI2R<6:0> | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R<6:0> | | | | | | | 0000 |
| RPINR26 | 06D4 | — | — | — | — | — | — | — | — | — | C1RXR<6:0> | | | | | | | 0000 |
| RPINR37 | 06EA | — | SYNCI1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR38 | 06EC | — | DTCMP1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR39 | 06EE | — | DTCMP3R<6:0> | | | | | | | — | DTCMP2R<6:0> | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 7-1: INTERRUPT VECTOR DETAILS**

| Interrupt Source | Vector # | IRQ # | IVT Address | Interrupt Bit Location | | |
|---|---|---|---|---|---|---|
| | | | | Flag | Enable | Priority |
| Highest Natural Order Priority | | | | | | |
| INT0 – External Interrupt 0 | 8 | 0 | 0x000014 | IFS0<0> | IEC0<0> | IPC0<2:0> |
| IC1 – Input Capture 1 | 9 | 1 | 0x000016 | IFS0<1> | IEC0<1> | IPC0<6:4> |
| OC1 – Output Compare 1 | 10 | 2 | 0x000018 | IFS0<2> | IEC0<2> | IPC0<10:8> |
| T1 – Timer1 | 11 | 3 | 0x00001A | IFS0<3> | IEC0<3> | IPC0<14:12> |
| DMA0 – DMA Channel 0 | 12 | 4 | 0x00001C | IFS0<4> | IEC0<4> | IPC1<2:0> |
| IC2 – Input Capture 2 | 13 | 5 | 0x00001E | IFS0<5> | IEC0<5> | IPC1<6:4> |
| OC2 – Output Compare 2 | 14 | 6 | 0x000020 | IFS0<6> | IEC0<6> | IPC1<10:8> |
| T2 – Timer2 | 15 | 7 | 0x000022 | IFS0<7> | IEC0<7> | IPC1<14:12> |
| T3 – Timer3 | 16 | 8 | 0x000024 | IFS0<8> | IEC0<8> | IPC2<2:0> |
| SPI1E – SPI1 Error | 17 | 9 | 0x000026 | IFS0<9> | IEC0<9> | IPC2<6:4> |
| SPI1 – SPI1 Transfer Done | 18 | 10 | 0x000028 | IFS0<10> | IEC0<10> | IPC2<10:8> |
| U1RX – UART1 Receiver | 19 | 11 | 0x00002A | IFS0<11> | IEC0<11> | IPC2<14:12> |
| U1TX – UART1 Transmitter | 20 | 12 | 0x00002C | IFS0<12> | IEC0<12> | IPC3<2:0> |
| AD1 – ADC1 Convert Done | 21 | 13 | 0x00002E | IFS0<13> | IEC0<13> | IPC3<6:4> |
| DMA1 – DMA Channel 1 | 22 | 14 | 0x000030 | IFS0<14> | IEC0<14> | IPC3<10:8> |
| Reserved | 23 | 15 | 0x000032 | — | — | — |
| SI2C1 – I2C1 Slave Event | 24 | 16 | 0x000034 | IFS1<0> | IEC1<0> | IPC4<2:0> |
| MI2C1 – I2C1 Master Event | 25 | 17 | 0x000036 | IFS1<1> | IEC1<1> | IPC4<6:4> |
| CM – Comparator Combined Event | 26 | 18 | 0x000038 | IFS1<2> | IEC1<2> | IPC4<10:8> |
| CN – Input Change Interrupt | 27 | 19 | 0x00003A | IFS1<3> | IEC1<3> | IPC4<14:12> |
| INT1 – External Interrupt 1 | 28 | 20 | 0x00003C | IFS1<4> | IEC1<4> | IPC5<2:0> |
| Reserved | 29-31 | 21-23 | 0x00003E-0x000042 | — | — | — |
| DMA2 – DMA Channel 2 | 32 | 24 | 0x000044 | IFS1<8> | IEC1<8> | IPC6<2:0> |
| OC3 – Output Compare 3 | 33 | 25 | 0x000046 | IFS1<9> | IEC1<9> | IPC6<6:4> |
| OC4 – Output Compare 4 | 34 | 26 | 0x000048 | IFS1<10> | IEC1<10> | IPC6<10:8> |
| T4 – Timer4 | 35 | 27 | 0x00004A | IFS1<11> | IEC1<11> | IPC6<14:12> |
| T5 – Timer5 | 36 | 28 | 0x00004C | IFS1<12> | IEC1<12> | IPC7<2:0> |
| INT2 – External Interrupt 2 | 37 | 29 | 0x00004E | IFS1<13> | IEC1<13> | IPC7<6:4> |
| U2RX – UART2 Receiver | 38 | 30 | 0x000050 | IFS1<14> | IEC1<14> | IPC7<10:8> |
| U2TX – UART2 Transmitter | 39 | 31 | 0x000052 | IFS1<15> | IEC1<15> | IPC7<14:12> |
| SPI2E – SPI2 Error | 40 | 32 | 0x000054 | IFS2<0> | IEC2<0> | IPC8<2:0> |
| SPI2 – SPI2 Transfer Done | 41 | 33 | 0x000056 | IFS2<1> | IEC2<1> | IPC8<6:4> |
| C1RX – CAN1 RX Data Ready(1) | 42 | 34 | 0x000058 | IFS2<2> | IEC2<2> | IPC8<10:8> |
| C1 – CAN1 Event(1) | 43 | 35 | 0x00005A | IFS2<3> | IEC2<3> | IPC8<14:12> |
| DMA3 – DMA Channel 3 | 44 | 36 | 0x00005C | IFS2<4> | IEC2<4> | IPC9<2:0> |
| IC3 – Input Capture 3 | 45 | 37 | 0x00005E | IFS2<5> | IEC2<5> | IPC9<6:4> |
| IC4 – Input Capture 4 | 46 | 38 | 0x000060 | IFS2<6> | IEC2<6> | IPC9<10:8> |
| Reserved | 47-56 | 39-48 | 0x000062-0x000074 | — | — | — |
| SI2C2 – I2C2 Slave Event | 57 | 49 | 0x000076 | IFS3<1> | IEC3<1> | IPC12<6:4> |
| MI2C2 – I2C2 Master Event | 58 | 50 | 0x000078 | IFS3<2> | IEC3<2> | IPC12<10:8> |
| Reserved | 59-64 | 51-56 | 0x00007A-0x000084 | — | — | — |
| PSEM – PWM Special Event Match(2) | 65 | 57 | 0x000086 | IFS3<9> | IEC3<9> | IPC14<6:4> |

**Note 1:** This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

**2:** This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**REGISTER 8-3: DMAxSTAH: DMA CHANNEL x START ADDRESS REGISTER A (HIGH)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STA<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **STA<23:16>:** Primary Start Address bits (source or destination)

**REGISTER 8-4: DMAxSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STA<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STA<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **STA<15:0>:** Primary Start Address bits (source or destination)

**REGISTER 9-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | TUN5 | TUN4 | TUN3 | TUN2 | TUN1 | TUN0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits

011111 = Maximum frequency deviation of 1.453% (7.477 MHz)
011110 = Center frequency + 1.406% (7.474 MHz)
• • •
000001 = Center frequency + 0.047% (7.373 MHz)
000000 = Center frequency (7.37 MHz nominal)
111111 = Center frequency – 0.047% (7.367 MHz)
• • •
100001 = Center frequency – 1.453% (7.263 MHz)
100000 = Minimum frequency deviation of -1.5% (7.259 MHz)

# 10.0 POWER-SAVING FEATURES

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Watchdog Timer and Power-Saving Modes"** (DS70615) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

## 10.1 Clock Frequency and Clock Switching

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

## 10.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 10-1.

**Note:** SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

**EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX**

```
PWRSAV  #SLEEP_MODE    ; Put the device into Sleep mode
PWRSAV  #IDLE_MODE     ; Put the device into Idle mode
```

**REGISTER 16-7: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)**

bit 7-6 **DTC<1:0>:** Dead-Time Control bits
11 = Dead-Time Compensation mode
10 = Dead-time function is disabled
01 = Negative dead time is actively applied for Complementary Output mode
00 = Positive dead time is actively applied for all output modes

bit 5 **DTCP:** Dead-Time Compensation Polarity bit(3)
When Set to '1':
If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened.
If DTCMPx = 1, PWMxH is shortened and PWMxL is lengthened.
When Set to '0':
If DTCMPx = 0, PWMxH is shortened and PWMxL is lengthened.
If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened.

bit 4 **Unimplemented:** Read as '0'

bit 3 **MTBS:** Master Time Base Select bit
1 = PWM generator uses the secondary master time base for synchronization and as the clock source for the PWM generation logic (if secondary time base is available)
0 = PWM generator uses the primary master time base for synchronization and as the clock source for the PWM generation logic

bit 2 **CAM:** Center-Aligned Mode Enable bit(2,4)
1 = Center-Aligned mode is enabled
0 = Edge-Aligned mode is enabled

bit 1 **XPRES:** External PWMx Reset Control bit(5)
1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
0 = External pins do not affect PWMx time base

bit 0 **IUE:** Immediate Update Enable bit(2)
1 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are immediate
0 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are synchronized to the PWMx period boundary

**Note 1:** Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
**2:** These bits should not be changed after the PWMx is enabled (PTEN = 1).
**3:** DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.
**4:** The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
**5:** To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

**REGISTER 16-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PDCx<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PDCx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **PDCx<15:0>:** PWMx Generator # Duty Cycle Value bits

**REGISTER 16-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PHASEx<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PHASEx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **PHASEx<15:0>:** PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

**Note 1:** If ITB (PWMCONx<9>) = `0`, the following applies based on the mode of operation:
Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = `00`, `01` or `10`),
PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs

**2:** If ITB (PWMCONx<9>) = `1`, the following applies based on the mode of operation:
Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = `00`, `01` or `10`),
PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL

**REGISTER 16-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER(1)**

bit 7-3 **FLTSRC<4:0>:** Fault Control Signal Source Select for PWM Generator # bits
11111 = Fault 32 **(default)**
11110 = Reserved
•
•
•
01100 = Reserved
01011 = Comparator 4
01010 = Op Amp/Comparator 3
01001 = Op Amp/Comparator 2
01000 = Op Amp/Comparator 1
00111 = Reserved
00110 = Reserved
00101 = Reserved
00100 = Reserved
00011 = Fault 4
00010 = Fault 3
00001 = Fault 2
00000 = Fault 1

bit 2 **FLTPOL:** Fault Polarity for PWM Generator # bit(2)
1 = The selected Fault source is active-low
0 = The selected Fault source is active-high

bit 1-0 **FLTMOD<1:0>:** Fault Mode for PWM Generator # bits
11 = Fault input is disabled
10 = Reserved
01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (cycle)
00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (latched condition)

**Note 1:** If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

**2:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

## 17.1 QEI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 17.1.1 KEY RESOURCES

- **"Quadrature Encoder Interface"** (DS70601) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 24.2 PTG Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 24.2.1 KEY RESOURCES

- **"Peripheral Trigger Generator"** (DS70669) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

**REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CON | COE | CPOL | — | — | — | CEVT | COUT |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| EVPOL1 | EVPOL0 | — | CREF(1) | — | — | CCH1(1) | CCH0(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
1 = Comparator event according to EVPOL<1:0> settings occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur

bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (non-inverted polarity):
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1 (inverted polarity):
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output.
If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output.
01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)
If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output.
If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output.
00 = Trigger/event/interrupt generation is disabled

**Note 1:** Inputs that are selected and not available will be tied to VSS. See the **"Pin Diagrams"** section for available inputs for each package.

# 30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

## Absolute Maximum Ratings(1)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to $V_{SS}$(3) ..... -0.3V to ($V_{DD}$ + 0.3V)
Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD} \geq 3.0V$(3) ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when $V_{DD} < 3.0V$(3) ..... -0.3V to +3.6V
Maximum current out of $V_{SS}$ pin ..... 300 mA
Maximum current into $V_{DD}$ pin(2) ..... 300 mA
Maximum current sunk/sourced by any 4x I/O pin ..... 15 mA
Maximum current sunk/sourced by any 8x I/O pin ..... 25 mA
Maximum current sunk by all ports(2,4) ..... 200 mA

**Note 1:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**2:** Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

**3:** See the **“Pin Diagrams”** section for the 5V tolerant pins.

**4:** Exceptions are: dsPIC33EPXXXGP502, dsPIC33EPXXXMC202/502 and PIC24EPXXXGP/MC202 devices, which have a maximum sink/source capability of 130 mA.

**TABLE 30-18: PLL CLOCK TIMING SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| OS50 | FPLLI | PLL Voltage Controlled Oscillator (VCO) Input Frequency Range | 0.8 | — | 8.0 | MHz | ECPLL, XTPLL modes |
| OS51 | FVCO | On-Chip VCO System Frequency | 120 | — | 340 | MHz | |
| OS52 | TLOCK | PLL Start-up Time (Lock Time) | 0.9 | 1.5 | 3.1 | ms | |
| OS53 | DCLK | CLKO Stability (Jitter)(2) | -3 | 0.5 | 3 | % | |

**Note 1:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases, or communication clocks used by the application, use the following formula:

$$Effective\ Jitter = \frac{DCLK}{\sqrt{\frac{FOSC}{Time\ Base\ or\ Communication\ Clock}}}$$

For example, if FOSC = 120 MHz and the SPIx bit rate = 10 MHz, the effective jitter is as follows:

$$Effective\ Jitter = \frac{DCLK}{\sqrt{\frac{120}{10}}} = \frac{DCLK}{\sqrt{12}} = \frac{DCLK}{3.464}$$

**TABLE 30-19: INTERNAL FRC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| **Internal FRC Accuracy @ FRC Frequency = 7.37 MHz(1)** | | | | | | | |
| F20a | FRC | -1.5 | 0.5 | +1.5 | % | -40°C ≤ TA ≤ -10°C | VDD = 3.0-3.6V |
| | | -1 | 0.5 | +1 | % | -10°C ≤ TA ≤ +85°C | VDD = 3.0-3.6V |
| F20b | FRC | -2 | 1 | +2 | % | +85°C ≤ TA ≤ +125°C | VDD = 3.0-3.6V |

**Note 1:** Frequency is calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

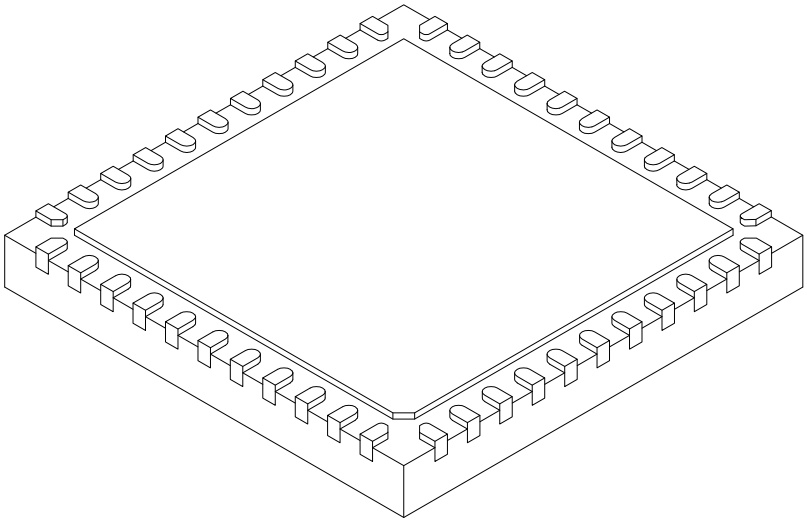
**TABLE 30-20: INTERNAL LPRC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| **LPRC @ 32.768 kHz(1)** | | | | | | | |
| F21a | LPRC | -30 | — | +30 | % | -40°C ≤ TA ≤ -10°C | VDD = 3.0-3.6V |
| | | -20 | — | +20 | % | -10°C ≤ TA ≤ +85°C | VDD = 3.0-3.6V |
| F21b | LPRC | -30 | — | +30 | % | +85°C ≤ TA ≤ +125°C | VDD = 3.0-3.6V |

**Note 1:** The change of LPRC frequency as VDD changes.

## 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 44 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 8.00 BSC | |
| Exposed Pad Width | E2 | 6.25 | 6.45 | 6.60 |
| Overall Length | D | | 8.00 BSC | |
| Exposed Pad Length | D2 | 6.25 | 6.45 | 6.60 |
| Terminal Width | b | 0.20 | 0.30 | 0.35 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Terminal-to-Exposed-Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2

**TABLE A-5: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 30.0 "Electrical Characteristics"** | • Throughout: qualifies all footnotes relating to the operation of analog modules below VDDMIN (replaces "will have" with "may have")<br>• Throughout: changes all references of SPI timing parameter symbol "TscP" to "FscP"<br>• Table 30-1: changes VDD range to 3.0V to 3.6V<br>• Table 30-4: removes Parameter DC12 (RAM Retention Voltage)<br>• Table 30-7: updates Maximum values at 10 and 20 MIPS<br>• Table 30-8: adds Maximum IPD values, and removes all ΔIWDT entries<br>• Adds new Table 30-9 (Watchdog Timer Delta Current) with consolidated values removed from Table 30-8. All subsequent tables are renumbered accordingly.<br>• Table 30-10: adds footnote for all parameters for 1:2 Doze ratio<br>• Table 30-11:<br>- changes Minimum and Maximum values for D120 and D130<br>- adds Minimum and Maximum values for D131<br>- adds Minimum and Maximum values for D150 through D156, and removes Typical values<br>• Table 30-12:<br>- reformats table for readability<br>- changes IOL conditions for DO10<br>• Table 30-14: adds footnote to D135<br>• Table 30-17: changes Minimum and Maximum values for OS30<br>• Table 30-19:<br>- splits temperature range and adds new values for F20a<br>- reduces temperature range for F20b to extended temperatures only<br>• Table 30-20:<br>- splits temperature range and adds new values for F21a<br>- reduces temperature range for F20b to extended temperatures only<br>• Table 30-53:<br>- adds Maximum value to CM30<br>- adds footnote ("Parameter characterized...") to multiple parameters<br>• Table 30-55: adds Minimum and Maximum values for all CTMUI specifications, and removes Typical values<br>• Table 30-57: adds new footnote to AD09<br>• Table 30-58:<br>- removes all specifications for accuracy with external voltage references<br>- removes Typical values for AD23a and AD24a<br>- replaces Minimum and Maximum values for AD21a, AD22a, AD23a and AD24a with new values, split by Industrial and Extended temperatures<br>- removes Maximum value of AD30<br>- removes Minimum values from AD31a and AD32a<br>- adds or changes Typical values for AD30, AD31a, AD32a and AD33a<br>• Table 30-59:<br>- removes all specifications for accuracy with external voltage references<br>- removes Maximum value of AD30<br>- removes Typical values for AD23b and AD24b<br>- replaces Minimum and Maximum values for AD21b, AD22b, AD23b and AD24b with new values, split by Industrial and Extended temperatures<br>- removes Minimum and Maximum values from AD31b, AD32b, AD33b and AD34b<br>- adds or changes Typical values for AD30, AD31a, AD32a and AD33a<br>• Table 30-61: Adds footnote to AD51 |
| **Section 32.0 "DC and AC Device Characteristics Graphs"** | • Updates Figure 32-6 (Typical IDD @ 3.3V) with individual current vs. processor speed curves for the different program memory sizes |
| **Section 33.0 "Packaging Information"** | • Replaces drawing C04-149C (64-pin QFN, 7.15 x 7.15 exposed pad) with C04-154A (64-pin QFN, 5.4 x 5.4 exposed pad) |