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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

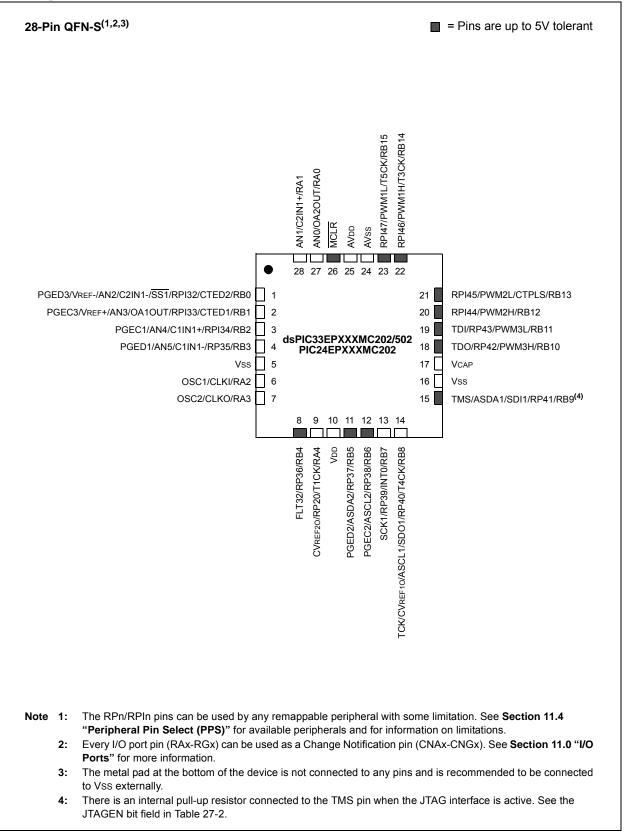
#### Details

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc504-e-tl

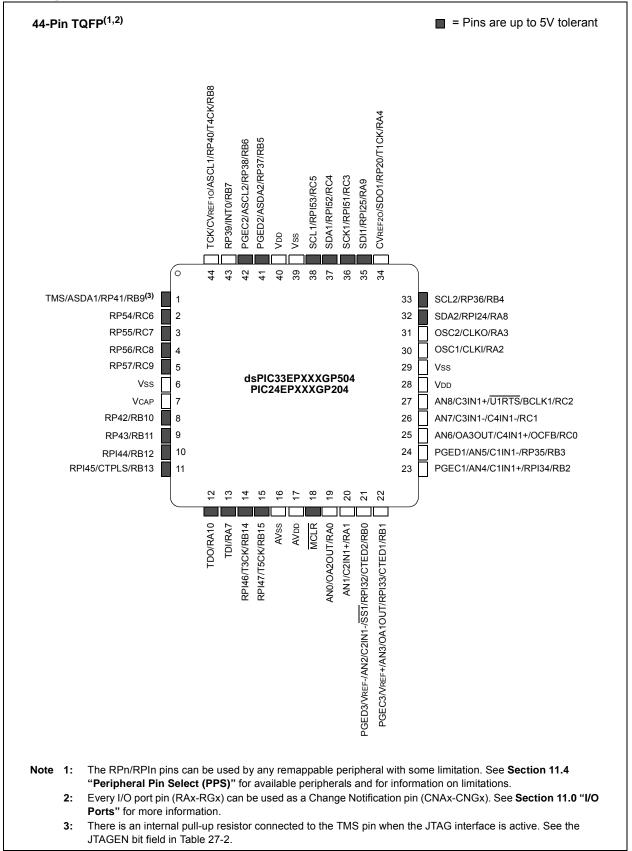
Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

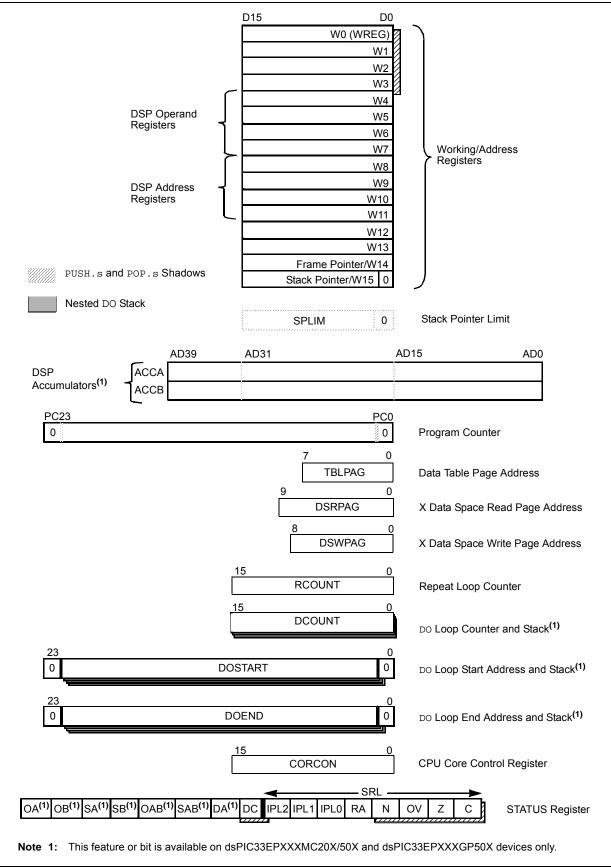
#### Pin Diagrams (Continued)

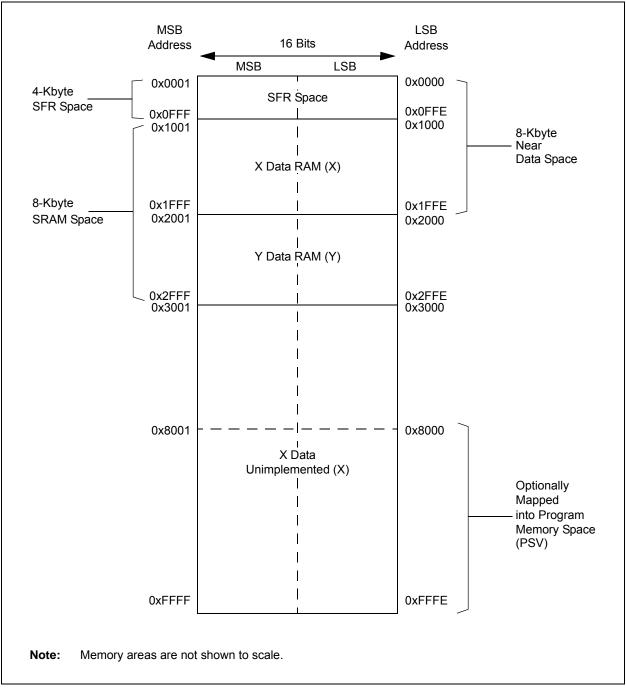


#### **Pin Diagrams (Continued)**









# FIGURE 4-8: DATA MEMORY MAP FOR dsPIC33EP64MC20X/50X AND dsPIC33EP64GP50X DEVICES

TABLE	4-2:	CPU C	CORE RE	EGISTER	R MAP F	FOR PIC	24EPX)	XGP/M	C20X D	EVICES	ONLY							
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000								W0 (WR	EG)								xxxx
W1	0002								W1									xxxx
W2	0004								W2									xxxx
W3	0006								W3									xxxx
W4	0008								W4									xxxx
W5	000A								W5									xxxx
W6	000C								W6									xxxx
W7	000E								W7									xxxx
W8	0010								W8									xxxx
W9	0012								W9									xxxx
W10	0014								W10									xxxx
W11	0016								W11									xxxx
W12	0018								W12									xxxx
W13	001A								W13									xxxx
W14	001C								W14									xxxx
W15	001E								W15									xxxx
SPLIM	0020								SPLIM<1	5:0>								0000
PCL	002E							P	CL<15:1>								—	0000
PCH	0030	—	-	_	_	—	—	—	—	_				PCH<6:0>				0000
DSRPAG	0032	—	-	_	_	—	—					DSRPA	G<9:0>					0001
DSWPAG	0034	_				_		_				DS	SWPAG<8:0	>				0001
RCOUNT	0036								RCOUNT<	15:0>								0000
SR	0042	_				—		_	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	С	0000
CORCON	0044	VAR	_	-	-	—		—	_	-	_	—	-	IPL3	SFA	—	_	0020
DISICNT	0052	_	_							DISICNT<	:13:0>							0000
TBLPAG	0054	_	_	-	-	—		—	_				TBLPA	G<7:0>				0000
MSTRPR	0058								MSTRPR<	15:0>								0000

#### **D** I -4.0 - -

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

# 4.4.3 DATA MEMORY ARBITRATION AND BUS MASTER PRIORITY

EDS accesses from bus masters in the system are arbitrated.

The arbiter for data memory (including EDS) arbitrates between the CPU, the DMA and the ICD module. In the event of coincidental access to a bus by the bus masters, the arbiter determines which bus master access has the highest priority. The other bus masters are suspended and processed after the access of the bus by the bus master with the highest priority.

By default, the CPU is Bus Master 0 (M0) with the highest priority and the ICD is Bus Master 4 (M4) with the lowest priority. The remaining bus master (DMA Controller) is allocated to M3 (M1 and M2 are reserved and cannot be used). The user application may raise or lower the priority of the DMA Controller to be above that of the CPU by setting the appropriate bits in the EDS Bus Master Priority Control (MSTRPR) register. All bus masters with raised priorities will maintain the same priority relationship relative to each other (i.e., M1 being highest and M3 being lowest, with M2 in between). Also, all the bus masters with priorities below

### FIGURE 4-18: ARBITER ARCHITECTURE

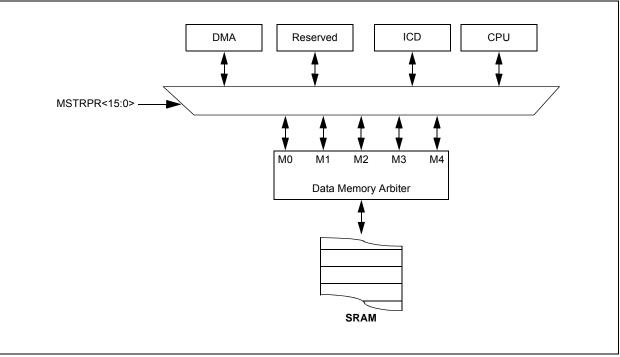
that of the CPU maintain the same priority relationship relative to each other. The priority schemes for bus masters with different MSTRPR values are tabulated in Table 4-62.

This bus master priority control allows the user application to manipulate the real-time response of the system, either statically during initialization or dynamically in response to real-time events.

TABLE 4-62:	DATA MEMORY BUS
	ARBITER PRIORITY

Drierity	MSTRPR<15:0	> Bit Setting <sup>(1)</sup>
Priority	0x0000	0x0020
M0 (highest)	CPU	DMA
M1	Reserved	CPU
M2	Reserved	Reserved
M3	DMA	Reserved
M4 (lowest)	ICD	ICD

**Note 1:** All other values of MSTRPR<15:0> are reserved.



#### 4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

#### 4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

#### 4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- · Register Indirect
- · Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal
- Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

#### TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
TRAPF	R IOPUWR	—	_	VREGSF	—	CM	VREGS
bit 15							bit 8
<b>D</b> 4440		DANIO	DAMO	DAMA	DAMO		
R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR bit 7	SWR	SWDTEN <sup>(2)</sup>	WDTO	SLEEP	IDLE	BOR	POR
							bit (
Legend:							
R = Reada	able bit	W = Writable I	oit	U = Unimpler	mented bit, read	d as '0'	
-n = Value	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkı	nown
bit 15	•	Reset Flag bit					
		onflict Reset ha onflict Reset ha		d			
bit 14	•	gal Opcode or			et Flag bit		
		I opcode detec			•	lized W registe	er used as ar
		Pointer caused					
	-	l opcode or Uni		egister Reset h	as not occurred	d	
bit 13-12	-	ted: Read as '			. 1.9		
bit 11		ash Voltage Reg Itage regulator i			p bit		
		ltage regulator (		•	ing Sleep		
bit 10		ted: Read as '	-	,,	5		
bit 9	CM: Configur	ation Mismatch	Flag bit				
	1 = A Configu	uration Mismatc uration Mismatc	h Reset has				
bit 8	VREGS: Volta	age Regulator S	Standby Durir	ng Sleep bit			
	•	egulator is active egulator goes in	•	•	еер		
bit 7	EXTR: Extern	nal Reset (MCL	R) Pin bit				
		Clear (pin) Res Clear (pin) Res					
bit 6	SWR: Softwa	re RESET (Instr	uction) Flag	bit			
		instruction has instruction has					
bit 5	SWDTEN: So	oftware Enable/	Disable of W	DT bit <sup>(2)</sup>			
	1 = WDT is e 0 = WDT is di						
bit 4	WDTO: Watc	hdog Timer Tim	e-out Flag bi	it			
		e-out has occur e-out has not oc					
Note 1:	All of the Reset sta cause a device Re		set or cleare	d in software. S	Setting one of th	ese bits in soft	ware does not
2:	If the FWDTEN Co SWDTEN bit settir	onfiguration bit i	s '1' (unprog	rammed), the V	VDT is always e	enabled, regard	lless of the

# REGISTER 6-1: RCON: RESET CONTROL REGISTER<sup>(1)</sup>

# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

#### REGISTER 8-3: DMAXSTAH: DMA CHANNEL X START ADDRESS REGISTER A (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_	—	—	—	—	—	—
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STA<	23:16>			
bit 7							bit 0
Legend:							
R = Readable b	oit	W = Writable b	it	U = Unimpler	mented bit, read	as '0'	

-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 15-8 Unimplemented: Read as '0'

bit 7-0 STA<23:16>: Primary Start Address bits (source or destination)

#### REGISTER 8-4: DMAXSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			STA	<15:8>				
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			STA	A<7:0>				
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable b	oit	U = Unimpler	mented bit, rea	ad as '0'		
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown		

bit 15-0 STA<15:0>: Primary Start Address bits (source or destination)

#### 10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the powersaving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the ECAN<sup>™</sup> module has been configured for 500 kbps, based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the ECAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

#### 10.4 Peripheral Module Disable

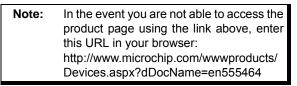
The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC<sup>®</sup> DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note:	If a PMD bit is set, the corresponding
	module is disabled after a delay of one
	instruction cycle. Similarly, if a PMD bit is
	cleared, the corresponding module is
	enabled after a delay of one instruction
	cycle (assuming the module control regis-
	ters are already configured to enable
	module operation).

### 10.5 Power-Saving Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.



#### 10.5.1 KEY RESOURCES

- "Watchdog Timer and Power-Saving Modes" (DS70615) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—	—	—	_	—	—	—	_		
bit 15							bit 8		
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—		INT2R<6:0>							
bit 7	t.								
Legend:									
R = Readal	ole bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'			
-n = Value at POR '1' =		'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown			
bit 15-7	Unimplemen	ted: Read as 'd	)'						
bit 6-0		INT2R<6:0>: Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)							
	1111001 <b>= lr</b>	put tied to RPI	121						
	0000001 – Ir	put tied to CMI	⊃1						
		put tied to Civil							

#### REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

#### REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 — T2CKR<6:0>										
U-0       R/W-0       R	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
U-0       R/W-0       R	_	-	—	_	—	—	—	—		
—       T2CKR<6:0>         bit 7       t         Legend:       R = Readable bit       W = Writable bit       U = Unimplemented bit, read as '0'         -n = Value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15-7       Unimplemented: Read as '0'         bit 6-0       T2CKR<6:0>: Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers)         1111001 = Input tied to RPI121       .         .	bit 15							bit 8		
bit 7       Image: Constraint of the system of	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
Legend:         R = Readable bit       W = Writable bit       U = Unimplemented bit, read as '0'         -n = Value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15-7       Unimplemented: Read as '0'         bit 6-0       T2CKR<6:0>: Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers)         1111001 = Input tied to RPI121         . <td< td=""><td>—</td><td></td><td colspan="8">T2CKR&lt;6:0&gt;</td></td<>	—		T2CKR<6:0>							
R = Readable bit       W = Writable bit       U = Unimplemented bit, read as '0'         -n = Value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15-7       Unimplemented: Read as '0'         bit 6-0       T2CKR<6:0>: Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers)         1111001 = Input tied to RPI121         .      <	bit 7		bit							
R = Readable bit       W = Writable bit       U = Unimplemented bit, read as '0'         -n = Value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15-7       Unimplemented: Read as '0'         bit 6-0       T2CKR<6:0>: Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers)         1111001 = Input tied to RPI121         .      <										
-n = Value at POR       '1' = Bit is set       '0' = Bit is cleared       x = Bit is unknown         bit 15-7       Unimplemented: Read as '0'         bit 6-0       T2CKR<6:0>: Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers)         1111001 = Input tied to RPI121         .	Legend:									
bit 15-7 Unimplemented: Read as '0' bit 6-0 T2CKR<6:0>: Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121 0000001 = Input tied to CMP1	R = Readab	ole bit	W = Writable I	bit	U = Unimpler	mented bit, read	as '0'			
bit 6-0 <b>T2CKR&lt;6:0&gt;:</b> Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121	-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown			
bit 6-0 <b>T2CKR&lt;6:0&gt;:</b> Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121										
(see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121 0000001 = Input tied to CMP1	bit 15-7	Unimplemen	ted: Read as 'd	)'						
1111001 = Input tied to RPI121	bit 6-0									
		0000001 = Ir	nout tied to CM	⊃1						
·										
		0000000 <b>- II</b>	iput tied to vss							

#### REGISTER 11-8: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				QEB1R<6:0>			
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				QEA1R<6:0>			
bit 7							bit 0
Legend:							
R = Readat	ole bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	
	1111001 =	1-2 for input pin Input tied to RPI Input tied to CM Input tied to Vss	121 P1				
bit 7	Unimpleme	nted: Read as '	0'				
bit 6-0	(see Table 1 1111001 =	>: Assign A (QE 1-2 for input pin Input tied to RPI Input tied to CM Input tied to Vss	selection nun 121 P1		n Pin bits		

### 13.2 Timer Control Registers

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0				
TON		TSIDL	—	_			_				
bit 15							bit 8				
U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0				
_	TGATE	TCKPS1	TCKPS0	T32	_	TCS	_				
bit 7							bit (				
<u> </u>											
Legend:	- 1-:4			II II.							
R = Readable		W = Writable		-	nented bit, rea						
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own				
bit 15	TON: Timerx	On hit									
	When T32 = 2										
	1 = Starts 32-	bit Timerx/y									
	•	0 = Stops 32-bit Timerx/y									
	<u>When T32 = 0</u> 1 = Starts 16-										
	0 = Stops 16-										
bit 14	Unimplemen	Unimplemented: Read as '0'									
bit 13	TSIDL: Timer	x Stop in Idle M	lode bit								
	1 = Discontinues module operation when device enters Idle mode										
		0 = Continues module operation in Idle mode									
bit 12-7	-	ted: Read as '									
bit 6		TGATE: Timerx Gated Time Accumulation Enable bit									
	<u>When TCS = 1:</u> This bit is ignored.										
	When TCS = $0$ :										
	1 = Gated time accumulation is enabled										
		e accumulation									
bit 5-4		: Timerx Input	Clock Prescal	e Select bits							
	11 = 1:256 10 = 1:64										
	01 = 1:8										
	00 = 1:1										
bit 3	T32: 32-Bit Ti	mer Mode Sele	ect bit								
		nd Timery form nd Timery act as									
bit 2	Unimplemen	ted: Read as '	)'								
bit 1	TCS: Timerx	Clock Source S	elect bit								
	1 = External c 0 = Internal cl	clock is from pir lock (FP)	n, TxCK (on th	ne rising edge)							
bit 0	Unimplomen	ted: Read as '	.,								

# REGISTER 13-1: TxCON: (TIMER2 AND TIMER4) CONTROL REGISTER

### dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—	-		DTRx<13:8>						
bit 15							bit 8		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
			DTR	x<7:0>					
bit 7							bit 0		
Legend:									
R = Readable bit W = Writable bit U = Uni			U = Unimpler	U = Unimplemented bit, read as '0'					
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown			nown						

### REGISTER 16-10: DTRx: PWMx DEAD-TIME REGISTER

bit 15-14 Unimplemented: Read as '0'

bit 13-0 DTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

#### REGISTER 16-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
_	_		ALTDTRx<13:8>						
bit 15							bit 8		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
			ALTDT	Rx<7:0>					
bit 7							bit 0		
Legend:									
R = Readable bit W = Writable bit			oit	U = Unimplemented bit, read as '0'					
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown		

bit 15-14 Unimplemented: Read as '0'

bit 13-0 ALTDTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	AMSK9	AMSK8
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0
bit 7							bit 0

#### REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	t, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 Unimplemented: Read as '0'

bit 9-0

AMSK<9:0>: Address Mask Select bits

For 10-Bit Address:

1 = Enables masking for bit Ax of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax; bit match is required in this position

For 7-Bit Address (I2CxMSK<6:0> only):

1 = Enables masking for bit Ax + 1 of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax + 1; bit match is required in this position

NOTES:

### 24.2 PTG Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

#### 24.2.1 KEY RESOURCES

- "Peripheral Trigger Generator" (DS70669) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

# TABLE 30-38:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	-	_	Lesser of FP or 11	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	_	-	-	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	-	-	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	—	_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—		ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	-	ns	
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	_	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 TCY + 40	—	_	ns	(Note 4)
SP60	TssL2doV	SDO2 Data Output Valid after SS2 Edge	—	—	50	ns	

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

# TABLE 30-39:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industria} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	—	—	15	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	-	_	ns	
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 TCY + 40	—		ns	(Note 4)

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

DMAxSTAH (DMA Channel x	
Start Address A, High)	144
DMAxSTAL (DMA Channel x	
Start Address A, Low)	144
DMAxSTBH (DMA Channel x	
Start Address B, High)	145
DMAxSTBL (DMA Channel x	
Start Address B, Low)	145
DSADRH (DMA Most Recent RAM	4 4 7
High Address)	147
DSADRL (DMA Most Recent RAM	1 4 7
Low Address) DTRx (PWMx Dead-Time)	
FCLCONx (PWMx Fault Current-Limit Control)	
I2CxCON (I2Cx Control)	
I2CxMSK (I2Cx Slave Mode Address Mask)	280
I2CxSTAT (I2Cx Status)	
ICxCON1 (Input Capture x Control 1)	
ICxCON2 (Input Capture x Control 2)	
INDX1CNTH (Index Counter 1 High Word)	
INDX1CNTL (Index Counter 1 Low Word)	259
INDX1HLD (Index Counter 1 Hold)	
INT1HLDH (Interval 1 Timer Hold High Word)	
INT1HLDL (Interval 1 Timer Hold Low Word)	
INT1TMRH (Interval 1 Timer High Word)	
INT1TMRL (Interval 1 Timer Low Word)	263
INTCON1 (Interrupt Control 1)	
INTCON2 (Interrupt Control 2)	136
INTCON2 (Interrupt Control 3)	
INTCON4 (Interrupt Control 4)	
INTTREG (Interrupt Control and Status)	
IOCONx (PWMx I/O Control)	240
LEBCONx (PWMx Leading-Edge	- · -
Blanking Control)	245
Blanking Control) LEBDLYx (PWMx Leading-Edge	
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay)	246
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle)	246 234
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High)	246 234 122
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low)	246 234 122 122
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control)	246 234 122 122 121
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key)	246 234 122 122 121 122
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1)	246 234 122 122 121 122 221
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2)	246 234 122 122 121 122 221 223
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control)	246 234 122 122 121 122 221 223 156
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning)	246 234 122 122 121 122 221 223 156 161
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle)	246 234 122 122 121 221 223 156 161 237
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning)	246 234 122 121 121 221 223 156 161 237 237
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift)	246 234 122 121 122 221 223 156 161 237 237 237 237
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PLLFBD (PLL Feedback Divisor)	246 234 122 121 122 221 223 156 161 237 237 237 160 166
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PLLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 1) PMD2 (Peripheral Module Disable Control 2)	246 234 122 121 122 221 223 156 161 237 237 237 160 166 168 169
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PLLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 2) PMD3 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 4)	246 234 122 121 122 221 223 156 161 237 237 237 160 166 168 169 169 169
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PLLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 2) PMD3 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 4)	246 234 122 121 122 221 223 156 161 237 237 160 166 168 169 169 170
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PLLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 2) PMD3 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 4) PMD6 (Peripheral Module Disable Control 6)	246 234 122 121 122 221 223 156 161 237 160 166 168 169 169 170 171
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PLLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 1) PMD2 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 4) PMD6 (Peripheral Module Disable Control 4) PMD6 (Peripheral Module Disable Control 6) PMD7 (Peripheral Module Disable Control 7) POS1CNTH (Position Counter 1 High Word)	246 234 122 121 122 221 223 156 161 237 160 166 168 169 169 170 171 258
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PHLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 1) PMD3 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 4) PMD6 (Peripheral Module Disable Control 6) PMD7 (Peripheral Module Disable Control 6) PMD7 (Peripheral Module Disable Control 7) POS1CNTH (Position Counter 1 High Word)	246 234 122 121 122 221 223 156 161 161 160 166 168 169 169 170 171 258 258
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PHLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 2) PMD3 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 4) PMD6 (Peripheral Module Disable Control 4) PMD7 (Peripheral Module Disable Control 6) PMD7 (Peripheral Module Disable Control 7) POS1CNTH (Position Counter 1 High Word) POS1LNTL (Position Counter 1 Hold)	246 234 122 121 122 221 223 156 161 237 160 160 168 169 169 170 171 258 258 258
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PHLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 1) PMD3 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 4) PMD6 (Peripheral Module Disable Control 6) PMD7 (Peripheral Module Disable Control 7) POS1CNTH (Position Counter 1 High Word) POS1LNTL (Position Counter 1 Hold) PTCON (PWMx Time Base Control)	246 234 122 121 122 221 223 156 161 237 160 160 168 169 169 170 171 258 258 258
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory Address Low) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PHLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 1) PMD2 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 3) PMD7 (Peripheral Module Disable Control 4) PMD7 (Peripheral Module Disable Control 6) PMD7 (Peripheral Module Disable Control 7) POS1CNTH (Position Counter 1 High Word) POS1CNTL (Position Counter 1 Hold) PTCON (PWMx Time Base Control)	246 234 122 121 122 221 223 156 161 237 160 160 168 169 169 170 171 258 258 230
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) OSCCON (Oscillator Control) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PLLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 1) PMD2 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 3) PMD5 (Peripheral Module Disable Control 4) PMD7 (Peripheral Module Disable Control 7) POS1CNTH (Position Counter 1 High Word) POS1HLD (Position Counter 1 Hold) PTCON (PWMx Time Base Control)	246 234 122 121 122 221 223 156 161 237 160 166 168 169 169 171 258 258 258 230 232
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCTUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PHLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 1) PMD2 (Peripheral Module Disable Control 3) PMD3 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 4) PMD7 (Peripheral Module Disable Control 6) PMD7 (Peripheral Module Disable Control 7) POS1CNTH (Position Counter 1 High Word) POS1CNTL (Position Counter 1 Hold) PTCON2 (PWMx Time Base Control) PTCON2 (PWMx Primary Master Clock Divider Select 2) PTGADJ (PTG Adjust)	246 234 122 121 122 221 223 156 161 237 237 160 166 168 169 169 169 169 170 171 258 258 258 230 232 348
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) OSCCUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PHLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 1) PMD2 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 3) PMD7 (Peripheral Module Disable Control 4) PMD7 (Peripheral Module Disable Control 6) PMD7 (Peripheral Module Disable Control 7) POS1CNTH (Position Counter 1 High Word) POS1CNTL (Position Counter 1 Hold) PTCON (PWMx Time Base Control) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable)	246 234 122 121 122 221 223 156 161 237 160 160 160 168 169 169 170 171 258 258 258 230 232 348 343
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) OSCCON (Oscillator Control) OSCCUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PHLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 1) PMD2 (Peripheral Module Disable Control 2) PMD3 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 4) PMD7 (Peripheral Module Disable Control 6) PMD7 (Peripheral Module Disable Control 7) POS1CNTH (Position Counter 1 High Word) POS1CNTL (Position Counter 1 Hold) PTCON2 (PWMx Time Base Control) PTCON2 (PWMx Primary Master Clock Divider Select 2) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable) PTGCOLIM (PTG Counter 0 Limit)	246 234 122 121 122 221 223 156 161 237 237 237 160 166 168 169 169 169 169 170 258 258 258 258 230 232 348 343 346
Blanking Control) LEBDLYx (PWMx Leading-Edge Blanking Delay) MDC (PWMx Master Duty Cycle) NVMADRH (Nonvolatile Memory Address High) NVMADRL (Nonvolatile Memory Address Low) NVMCON (Nonvolatile Memory (NVM) Control) NVMKEY (Nonvolatile Memory Key) OCxCON1 (Output Compare x Control 1) OCxCON2 (Output Compare x Control 2) OSCCON (Oscillator Control) OSCCON (Oscillator Control) OSCCUN (FRC Oscillator Tuning) PDCx (PWMx Generator Duty Cycle) PHASEx (PWMx Primary Phase-Shift) PHLFBD (PLL Feedback Divisor) PMD1 (Peripheral Module Disable Control 1) PMD2 (Peripheral Module Disable Control 3) PMD4 (Peripheral Module Disable Control 3) PMD7 (Peripheral Module Disable Control 4) PMD7 (Peripheral Module Disable Control 6) PMD7 (Peripheral Module Disable Control 7) POS1CNTH (Position Counter 1 High Word) POS1CNTL (Position Counter 1 Hold) PTCON (PWMx Time Base Control) PTGADJ (PTG Adjust) PTGBTE (PTG Broadcast Trigger Enable)	246 234 122 121 122 221 223 156 161 237 237 237 160 166 168 169 169 169 169 169 170 258 258 258 258 230 348 343 346 347

PTGCST (PTG Control/Status)	340
PTGHOLD (PTG Hold)	347
PTGL0 (PTG Literal 0)	
PTGQPTR (PTG Step Queue Pointer)	
PTGQUEx (PTG Step Queue x)	
PTGSDLIM (PTG Step Delay Limit)	
PTGT0LIM (PTG Timer0 Limit)	
PTGT1LIM (PTG Timer1 Limit)	345
PTPER (PWMx Primary Master Time	
Base Period)	233
PWMCONx (PWMx Control)	
QEI1CON (QEI1 Control)	252
QEI1GECH (QEI1 Greater Than or Equal	
Compare High Word)	262
QEI1GECL (QEI1 Greater Than or Equal	
Compare Low Word)	262
QEI1ICH (QEI1 Initialization/Capture	
High Word)	260
QEI1ICL (QEI1 Initialization/Capture	
Low Word)	260
QEI1IOC (QEI1 I/O Control)	254
QEI1LECH (QEI1 Less Than or Equal	004
Compare High Word)	261
QEI1LECL (QEI1 Less Than or Equal	061
Compare Low Word) QEI1STAT (QEI1 Status)	
RCON (Reset Control) REFOCON (Reference Oscillator Control)	
RPINR0 (Peripheral Pin Select Input 0)	
RPINR1 (Peripheral Pin Select Input 0)	
RPINR1 (Peripheral Pin Select Input 1)	
RPINR12 (Peripheral Pin Select Input 12)	
RPINR14 (Peripheral Pin Select Input 12)	
RPINR15 (Peripheral Pin Select Input 15)	
RPINR18 (Peripheral Pin Select Input 18)	
RPINR19 (Peripheral Pin Select Input 19)	
RPINR22 (Peripheral Pin Select Input 22)	
RPINR23 (Peripheral Pin Select Input 23)	
RPINR26 (Peripheral Pin Select Input 26)	
RPINR3 (Peripheral Pin Select Input 3)	
RPINR37 (Peripheral Pin Select Input 37)	
RPINR38 (Peripheral Pin Select Input 38)	
RPINR39 (Peripheral Pin Select Input 39)	
RPINR7 (Peripheral Pin Select Input 7)	
RPINR8 (Peripheral Pin Select Input 8)	
RPOR0 (Peripheral Pin Select Output 0)	
RPOR1 (Peripheral Pin Select Output 1)	
RPOR2 (Peripheral Pin Select Output 2)	198
RPOR3 (Peripheral Pin Select Output 3)	
RPOR4 (Peripheral Pin Select Output 4)	199
RPOR5 (Peripheral Pin Select Output 5)	199
RPOR6 (Peripheral Pin Select Output 6)	200
RPOR7 (Peripheral Pin Select Output 7)	200
RPOR8 (Peripheral Pin Select Output 8)	
RPOR9 (Peripheral Pin Select Output 9)	201
SEVTCMP (PWMx Primary Special	
Event Compare)	
SPIxCON1 (SPIx Control 1)	
SPIxCON2 (SPIx Control 2)	
SPIxSTAT (SPIx Status and Control)	
SR (CPU STATUS) 40,	
T1CON (Timer1 Centrel)	
T1CON (Timer1 Control)	205
TRGCONx (PWMx Trigger Control)	205 239
	205 239 242