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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc504-h-tl

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Pin Diagrams (Continued)



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4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP/MC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Program Memory" (DS70613) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

4.1 Program Address Space

The program address memory space of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in Section 4.8 "Interfacing Program and Data Memory Spaces".

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to read Device ID sections of the configuration memory space.

The program memory maps, which are presented by device family and memory size, are shown in Figure 4-1 through Figure 4-5.

FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X AND PIC24EP32GP/MC20X DEVICES



TABLE 4-59: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00		—	—				—			—		TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	001F
PORTA	0E02		—	_		_		—			—		RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04		—	—				—			—		LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06		—	—				—			—		ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08		—	—				—			—		CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A		—	—				—			—		CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C		—	—				—			—		CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	-	—	—			-	—		_	_		ANSA4	_	—	ANSA1	ANSA0	0013

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-60: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E			_	-	—	—	—	ANSB8		_	—		ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-17). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



11.4.4.1 Virtual Connections

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support virtual (internal) connections to the output of the op amp/ comparator module (see Figure 25-1 in Section 25.0 "Op Amp/Comparator Module"), and the PTG module (see Section 24.0 "Peripheral Trigger Generator (PTG) Module").

In addition, dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support virtual connections to the filtered QEI module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)".

Virtual connections provide a simple way of interperipheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of `b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QEI module allows peripherals to be connected to the QEI digital filter input. To utilize this filter, the QEI module must be enabled and its inputs must be connected to a physical RPn pin. Example 11-2 illustrates how the input capture module can be connected to the QEI digital filter.

EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QEI1 DIGITAL FILTER INPUT ON PIN 43 OF THE dsPIC33EPXXXMC206 DEVICE

RPINR15 = 0x2500;	/* Connect the QEI1 HOME1 input to RP37 (pin 43) */
RPINR7 = 0x009;	/* Connect the IC1 input to the digital filter on the FHOME1 input */
QEI1IOC = 0x4000;	/* Enable the QEI digital filter */
QEI1CON = 0x8000;	/* Enable the QEI module */

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	-	_	_	—	_	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				OCFAR<6:0>	>		
bit 7	-						bit 0
Legend:							

REGISTER 11-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 Unimplemented: Read as '0'

bit 6-0 OCFAR<6:0>: Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121

> . 0000001 = Input tied to CMP1 0000000 = Input tied to Vss

REGISTER 11-9: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				HOME1R<6:0	>		
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				INDX1R<6:0>	>		
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit				U = Unimplen	nented bit, rea	ad as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	Unimpleme	ented: Read as '	0'				
bit 15 bit 14-8	HOME1R<6	5:0>: Assign QEI	0 1 HOME1 (H selection nun	OME1) to the C	Corresponding	RPn Pin bits	
	1111001 =	Input tied to RPI	121	,			
		Input tied to CM	D1				
	0000000 =	Input tied to Vss	;				
bit 7	Unimpleme	ented: Read as '	0'				
bit 6-0	IND1XR<6: (see Table 2	0>: Assign QEI1 I1-2 for input pin	INDEX1 (INE selection nun	0X1) to the Cor nbers)	responding R	Pn Pin bits	
	1111001 =	Input tied to RPI	121	,			
	•						
	0000001 =	Input tied to CM	P1				
	0000000 =	Input tied to Vss					

12.0 TIMER1

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated in Asynchronous Counter mode from an external clock source
- The external clock input (T1CK) can optionally be synchronized to the internal device clock and the clock synchronization is performed after the prescaler
- A block diagram of Timer1 is shown in Figure 12-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- · Gated Timer mode
- Synchronous Counter mode
- · Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit setting for different operating modes are given in the Table 12-1.

Mode	TCS	TGATE	TSYNC
Timer	0	0	x
Gated Timer	0	1	х
Synchronous Counter	1	x	1
Asynchronous Counter	1	x	0

TABLE 12-1: TIMER MODE SETTINGS

FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM

15.2 Output Compare Control Registers

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0			
		OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	_	ENFLTB			
bit 15							bit 8			
R/W-0	U-0	R/W-0, HSC	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0			
ENFLTA		OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0			
bit 7							bit 0			
Legend:		HSC = Hardw	are Settable/Cl	earable bit						
R = Reada	ible bit	W = Writable I	Writable bit U = Unimplemented bit, read as '0'							
-n = Value	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown			
bit 15-14	Unimplemen	ted: Read as '0)'							
bit 13	OCSIDL: Out	tput Compare x	Stop in Idle Mo	de Control bit						
	1 = Output C	compare x Halts	in CPU Idle me	ode via CDU Idia m	odo					
bit 12 10	0 = Output Compare x continues to operate in CPU Idle mode									
DIL 12-10	OCISEL<2:0>: Output Compare X Clock Select bits									
	110 = Reserv	/ed								
	101 = PTGO	x clock ⁽²⁾								
	100 = T1CLK	is the clock so	urce of the OC	k (only the sync	hronous clock	is supported)				
	011 = 15CLK	is the clock sou	urce of the OC	Х У						
	010 = T4CLK 001 = T3CLK	is the clock so	urce of the OC	x X						
	000 = T2CLK	is the clock so	urce of the OC	ĸ						
bit 9	Unimplemen	ted: Read as '0)'							
bit 8	ENFLTB: Fau	ult B Input Enab	le bit							
	1 = Output C 0 = Output C	ompare Fault B compare Fault B	input (OCFB) input (OCFB)	is enabled is disabled						
bit 7	ENFLTA: Fau	ult A Input Enabl	le bit							
	1 = Output C	ompare Fault A	input (OCFA)	is enabled						
	0 = Output C	ompare Fault A	input (OCFA)	is disabled						
bit 6	Unimplemen	ted: Read as '0)'							
bit 5	OCFLTB: PW	M Fault B Cond	dition Status bit							
	1 = PWM Fa 0 = No PWM	ult B condition of Fault B condition	on OCFB pin ha on on OCFB pi	as occurred n has occurred						
bit 4	OCFLTA: PW	/M Fault A Cond	dition Status bit							
	1 = PWM Fault A condition on OCFA pin has occurred									
	0 = No PWM	I Fault A condition	on on OCFA pi	n has occurred						
Note 1:	OCxR and OCxF	RS are double-b	ouffered in PWN	A mode only.						
2:	Each Output Cor	mpare x module	(OCx) has one	PTG clock sou	urce. See Secti	on 24.0 "Perip	oheral Trigger			
	Generator (PTG PTGO4 = OC1) wodule" for r	nore informatio	n.						
	PTGO5 = OC2									
	PTGO6 = OC3									
	PTGO7 = OC4									

REGISTER 16-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER⁽¹⁾

- bit 7-3 FLTSRC<4:0>: Fault Control Signal Source Select for PWM Generator # bits 11111 = Fault 32 (default) 11110 = Reserved . . 01100 = Reserved 01011 = Comparator 4 01010 = Op Amp/Comparator 3
 - 01001 = Op Amp/Comparator 2
 - 01000 = Op Amp/Comparator 1
 - 00111 = Reserved
 - 00110 = Reserved
 - 00101 = Reserved
 - 00100 = Reserved
 - 00011 = Fault 4
 - 00010 = Fault 3
 - 00001 = Fault 2 00000 = Fault 1
- bit 2 ELTROL Fault Delarity for DWM Concrete

bit 2 **FLTPOL:** Fault Polarity for PWM Generator # bit⁽²⁾

- 1 = The selected Fault source is active-low
- 0 = The selected Fault source is active-high
- bit 1-0 FLTMOD<1:0>: Fault Mode for PWM Generator # bits
 - 11 = Fault input is disabled
 - 10 = Reserved
 - 01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (cycle)
 - 00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (latched condition)
- **Note 1:** If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.
 - **2:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 21-8:	CxEC: ECANx TRANSMIT/RECEIVE ERROR COUNT REGISTER
REGISTER 21-8:	CXEC: ECANX TRANSMIT/RECEIVE ERROR COUNT REGISTE

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			TERR	CNT<7:0>			
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			RERR	CNT<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'				
-n = Value at PC	R	'1' = Bit is set	'1' = Bit is set '0' = Bit is cleared x = Bit is unknow			x = Bit is unknowr	า

bit 15-8	TERRCNT<7:0>:	Transmit Error	Count bits
DIL 10-0	IERRGNI < 1.0>.	Hanshill Enoi	Count bits

bit 7-0 **RERRCNT<7:0>:** Receive Error Count bits

REGISTER 21-9: CxCFG1: ECANx BAUD RATE CONFIGURATION REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SJW1 | SJW0 | BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 |
| bit 7 | | | • | • | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8	Unimplemented: Read as '0'
----------	----------------------------

bit 7-6	SJW<1:0>: Synchronization Jump Width bits
	11 = Length is 4 x TQ
	$10 = \text{Length is } 3 \times \text{Tq}$
	01 = Length is 2 x TQ
	00 = Length is 1 x TQ

```
bit 5-0 BRP<5:0>: Baud Rate Prescaler bits
```

```
11 1111 = TQ = 2 x 64 x 1/FCAN
```

•

- 00 0010 = TQ = 2 x 3 x 1/FCAN 00 0001 = TQ = 2 x 2 x 1/FCAN
- 00 0000 = Tq = 2 x 1 x 1/FCAN

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1		
bit 15				·	- -	·	bit 8		
U-x	U-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
_	—	—	RB0	DLC3	DLC2	DLC1	DLC0		
bit 7						bit 0			
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'					
-n = Value at	POR	'1' = Bit is set	t	'0' = Bit is cleared x = Bit is unknown					
bit 15-10	EID<5:0>: E>	ktended Identifi	er bits						
bit 9	RTR: Remote	e Transmission	Request bit						
	When IDE =	<u>1:</u>							
	1 = Message	will request re	mote transmis	ssion					
		lessage							
	When $IDE = 0$:								
hit 9	BB1 : Boson	od Dit 1							
DILO	Llear must so	t this hit to '0'	oor CAN proto						
DIT 7-5	Unimplemen	ted: Read as	0						
bit 4	RB0: Reserve	ed Bit 0							
	User must se	t this bit to '0' p	per CAN proto	COI.					

BUFFER 21-3: ECAN™ MESSAGE BUFFER WORD 2

bit 3-0 DLC<3:0>: Data Length Code bits

BUFFER 21-4: ECAN[™] MESSAGE BUFFER WORD 3

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
			B	/te 1				
bit 15							bit 8	
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
			B	/te 0				
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set			'0' = Bit is clea	ared	x = Bit is unkr	nown		

bit 15-8 Byte 1<15:8>: ECAN Message Byte 1 bits

bit 7-0 Byte 0<7:0>: ECAN Message Byte 0 bits

NOTES:

26.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Programmable Cyclic Redundancy Check (CRC)" (DS70346) of the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The programmable CRC generator offers the following features:

- User-programmable (up to 32nd order) polynomial CRC equation
- Interrupt output
- Data FIFO

The programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-programmable CRC polynomial equation, up to 32 bits
- Programmable shift direction (little or big-endian)
- · Independent data and polynomial lengths
- Configurable interrupt output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 26-1. A simple version of the CRC shift engine is shown in Figure 26-2.

FIGURE 26-1: CRC BLOCK DIAGRAM

27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

TABLE 27-3: USER ID WORDS REGISTER MAP

File Name	Address	Bits 23-16	Bits 15-0
FUID0	0x800FF8	—	UID0
FUID1	0x800FFA	—	UID1
FUID2	0x800FFC	—	UID2
FUID3	0x800FFE	—	UID3

Legend: — = unimplemented, read as '1'.

27.3 On-Chip Voltage Regulator

All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family incorporate an onchip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in **Section 30.0 "Electrical Characteristics"**.

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE

REGULATOR^(1,2,3)

27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 30-22 of **Section 30.0 "Electrical Characteristics"** for specific TFSCM values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

Field	Description
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 working registers ∈ {W0W15}
Wnd	One of 16 destination working registers ∈ {W0W15}
Wns	One of 16 source working registers ∈ {W0W15}
WREG	W0 (working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb] }
Wx	X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}
Wxd	X Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}
Wy	Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}
Wyd	Y Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}

TABLE 28-1:	SYMBOLS USED IN OPCODE DESCRIPTIONS ((CONTINUED)

FIGURE 30-11: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

TABLE 30-30: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Chara	cteristic ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions
TQ10	TtQH	TQCK High Time	Synchronous, with prescaler	Greater of 12.5 + 25 or (0.5 TCY/N) + 25			ns	Must also meet Parameter TQ15
TQ11	TtQL	TQCK Low Time	Synchronous, with prescaler	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	_	_	ns	Must also meet Parameter TQ15
TQ15	TtQP	TQCP Input Period	Synchronous, with prescaler	Greater of 25 + 50 or (1 Tcy/N) + 50	_	_	ns	
TQ20	TCKEXTMRL	Delay from External TQCK Clock Edge to Timer Increment		_	1	Тсү	—	

Note 1: These parameters are characterized but not tested in manufacturing.

48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

	N	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	
Number of Pins	N		48		
Pitch	е		0.40 BSC		
Overall Height	Α	0.45	0.50	0.55	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3	0.127 REF			
Overall Width	E	6.00 BSC			
Exposed Pad Width	E2	4.45	4.60	4.75	
Overall Length	D	6.00 BSC			
Exposed Pad Length	D2	4.45	4.60	4.75	
Contact Width	b	0.15	0.20	0.25	
Contact Length	L	0.30	0.40	0.50	
Contact-to-Exposed Pad	K	0.20	-	_	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

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