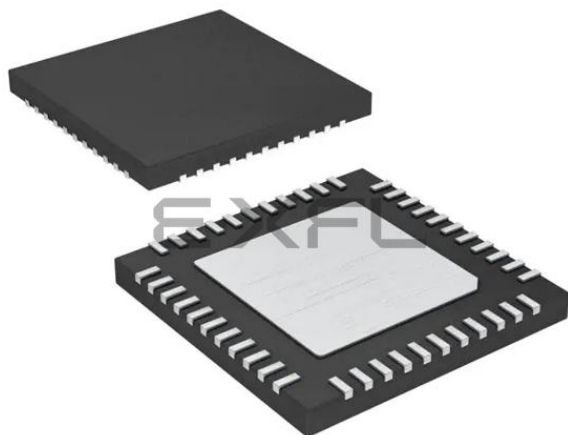




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Details

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc504t-e-ml

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name ⁽⁴⁾	Pin Type	Buffer Type	PPS	Description
AN0-AN15	I	Analog	No	Analog input channels.
CLKI	I	ST/ CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/ CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
REFCLKO	O	—	Yes	Reference clock output.
IC1-IC4	I	ST	Yes	Capture Inputs 1 through 4.
OCFA	I	ST	Yes	Compare Fault A input (for Compare channels).
OCFB	I	ST	No	Compare Fault B input (for Compare channels).
OC1-OC4	O	—	Yes	Compare Outputs 1 through 4.
INT0	I	ST	No	External Interrupt 0.
INT1	I	ST	Yes	External Interrupt 1.
INT2	I	ST	Yes	External Interrupt 2.
RA0-RA4, RA7-RA12	I/O	ST	No	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	No	PORTB is a bidirectional I/O port.
RC0-RC13, RC15	I/O	ST	No	PORTC is a bidirectional I/O port.
RD5, RD6, RD8	I/O	ST	No	PORTD is a bidirectional I/O port.
RE12-RE15	I/O	ST	No	PORTE is a bidirectional I/O port.
RF0, RF1	I/O	ST	No	PORTF is a bidirectional I/O port.
RG6-RG9	I/O	ST	No	PORTG is a bidirectional I/O port.
T1CK	I	ST	No	Timer1 external clock input.
T2CK	I	ST	Yes	Timer2 external clock input.
T3CK	I	ST	No	Timer3 external clock input.
T4CK	I	ST	No	Timer4 external clock input.
T5CK	I	ST	No	Timer5 external clock input.
CTPLS	O	ST	No	CTMU pulse output.
CTED1	I	ST	No	CTMU External Edge Input 1.
CTED2	I	ST	No	CTMU External Edge Input 2.
U1CTS	I	ST	No	UART1 Clear-To-Send.
U1RTS	O	—	No	UART1 Ready-To-Send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
BCLK1	O	ST	No	UART1 IrDA [®] baud clock output.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
PPS = Peripheral Pin Select TTL = TTL input buffer

- Note 1:** This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- 2:** This pin is available on dsPIC33EPXXXGP/MC50X devices only.
- 3:** This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 “High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”** for more information.
- 4:** Not all pins are available in all packages variants. See the **“Pin Diagrams”** section for pin availability.
- 5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	—	—	—	—	—	—	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	CTMUIF	—	—	—	—	—	—	C1TXIF	—	—	CRCIF	U2EIF	U1EIF	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTIEIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	—	—	—	—	—	—	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	—	C1TXIE	—	—	CRCIE	U2EIE	U1EIE	—	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTIEIE	—	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	C1IP<2:0>			—	C1RXIP<2:0>			—	SPI2IP<2:0>			—	SPI2EIP<2:0>			4444
IPC9	0852	—	—	—	—	—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			0444
IPC11	0856	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IPC12	0858	—	—	—	—	—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	—	—	—	0440
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC17	0862	—	—	—	—	—	C1TXIP<2:0>			—	—	—	—	—	—	—	—	0400
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP<2:0>			—	—	—	—	0040
IPC35	0886	—	JTAGIP<2:0>			—	ICDIP<2:0>			—	—	—	—	—	—	—	—	4400
IPC36	0888	—	PTG0IP<2:0>			—	PTGWDIP<2:0>			—	PTGSTIEIP<2:0>			—	—	—	—	4440
IPC37	088A	—	—	—	—	—	PTG3IP<2:0>			—	PTG2IP<2:0>			—	PTG1IP<2:0>			0444

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 8-1: DMAxCON: DMA CHANNEL x CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CHEN	SIZE	DIR	HALF	NULLW	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	—	AMODE1	AMODE0	—	—	MODE1	MODE0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CHEN:** DMA Channel Enable bit
 1 = Channel is enabled
 0 = Channel is disabled
- bit 14 **SIZE:** DMA Data Transfer Size bit
 1 = Byte
 0 = Word
- bit 13 **DIR:** DMA Transfer Direction bit (source/destination bus select)
 1 = Reads from RAM address, writes to peripheral address
 0 = Reads from peripheral address, writes to RAM address
- bit 12 **HALF:** DMA Block Transfer Interrupt Select bit
 1 = Initiates interrupt when half of the data has been moved
 0 = Initiates interrupt when all of the data has been moved
- bit 11 **NULLW:** Null Data Peripheral Write Mode Select bit
 1 = Null data write to peripheral in addition to RAM write (DIR bit must also be clear)
 0 = Normal operation
- bit 10-6 **Unimplemented:** Read as '0'
- bit 5-4 **AMODE<1:0>:** DMA Channel Addressing Mode Select bits
 11 = Reserved
 10 = Peripheral Indirect Addressing mode
 01 = Register Indirect without Post-Increment mode
 00 = Register Indirect with Post-Increment mode
- bit 3-2 **Unimplemented:** Read as '0'
- bit 1-0 **MODE<1:0>:** DMA Channel Operating Mode Select bits
 11 = One-Shot, Ping-Pong modes are enabled (one block transfer from/to each DMA buffer)
 10 = Continuous, Ping-Pong modes are enabled
 01 = One-Shot, Ping-Pong modes are disabled
 00 = Continuous, Ping-Pong modes are disabled

REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/S-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
FORCE ⁽¹⁾	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0
bit 7							bit 0

Legend:	S = Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15	FORCE: Force DMA Transfer bit ⁽¹⁾ 1 = Forces a single DMA transfer (Manual mode) 0 = Automatic DMA transfer initiation by DMA request
bit 14-8	Unimplemented: Read as '0'
bit 7-0	IRQSEL<7:0>: DMA Peripheral IRQ Number Select bits 01000110 = ECAN1 – TX Data Request ⁽²⁾ 00100110 = IC4 – Input Capture 4 00100101 = IC3 – Input Capture 3 00100010 = ECAN1 – RX Data Ready ⁽²⁾ 00100001 = SPI2 Transfer Done 00011111 = UART2TX – UART2 Transmitter 00011110 = UART2RX – UART2 Receiver 00011100 = TMR5 – Timer5 00011011 = TMR4 – Timer4 00011010 = OC4 – Output Compare 4 00011001 = OC3 – Output Compare 3 00001101 = ADC1 – ADC1 Convert done 00001100 = UART1TX – UART1 Transmitter 00001011 = UART1RX – UART1 Receiver 00001010 = SPI1 – Transfer Done 00001000 = TMR3 – Timer3 00000111 = TMR2 – Timer2 00000110 = OC2 – Output Compare 2 00000101 = IC2 – Input Capture 2 00000010 = OC1 – Output Compare 1 00000001 = IC1 – Input Capture 1 00000000 = INT0 – External Interrupt 0

- Note 1:** The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).
- 2:** This selection is available in dsPIC33EPXXXGP/MC50X devices only.

15.0 OUTPUT COMPARE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Output Compare**” (DS70358) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The output compare module can select one of seven available clock sources for its time base. The module compares the value of the timer with the value of one or two compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the compare register value. The output compare module generates either a single output pulse or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Note: See “**Output Compare**” (DS70358) in the “dsPIC33/PIC24 Family Reference Manual” for OCxR and OCxRS register restrictions.

FIGURE 15-1: OUTPUT COMPARE x MODULE BLOCK DIAGRAM

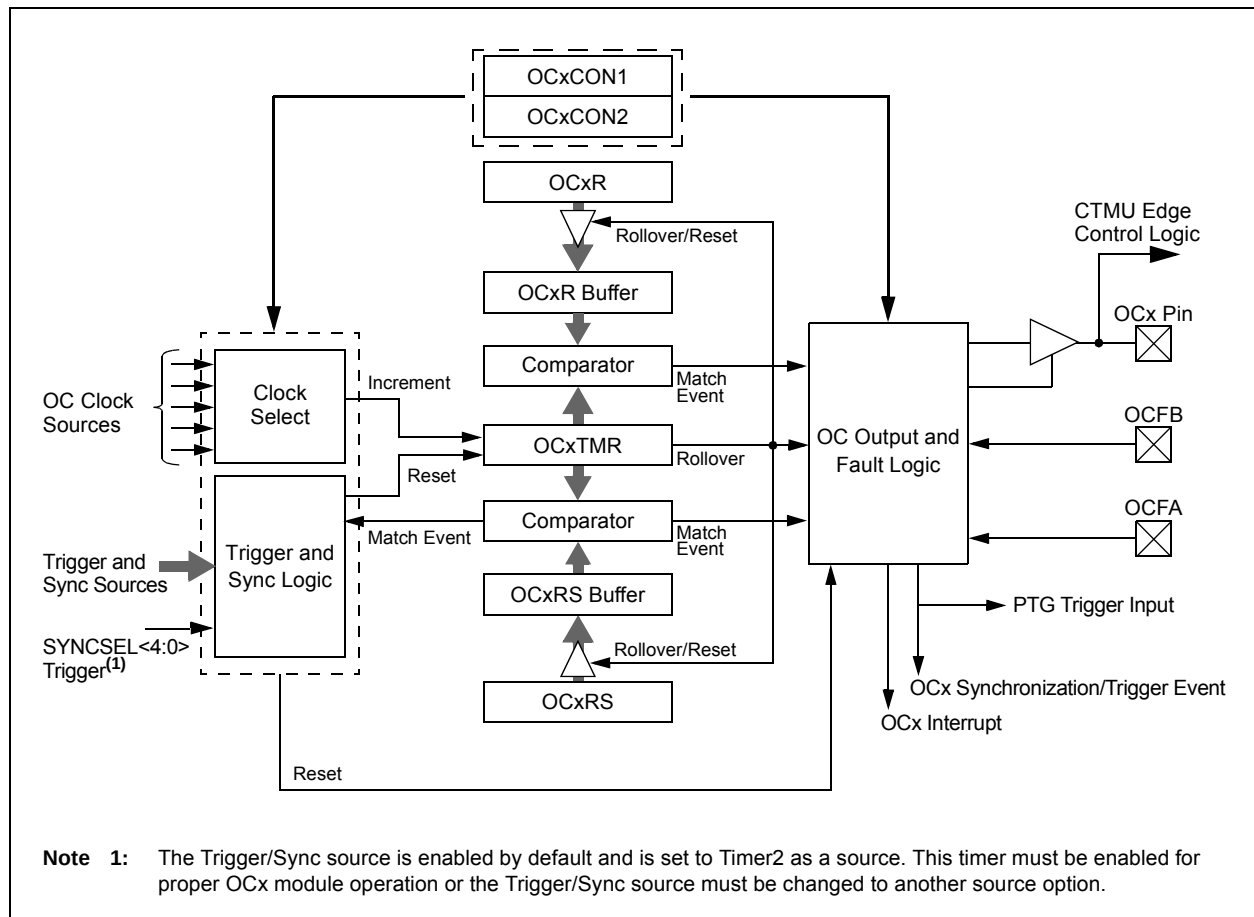
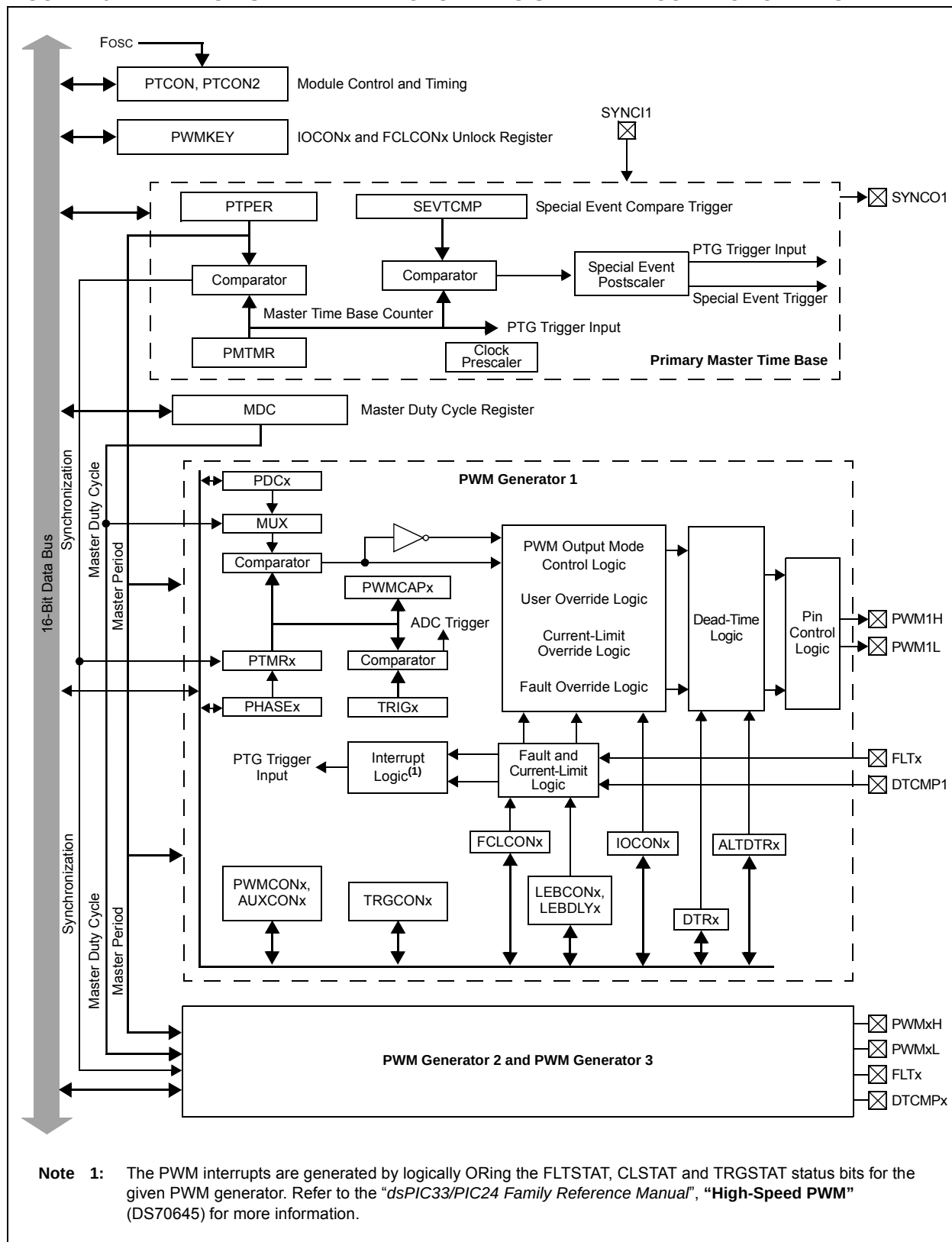


FIGURE 16-2: HIGH-SPEED PWMx MODULE REGISTER INTERCONNECTION DIAGRAM

REGISTER 16-16: LEBCONx: PWMx LEADING-EDGE BLANKING CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—
bit 15						bit 8	
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	BCH ⁽¹⁾	BCL ⁽¹⁾	BPHH	BPHL	BPLH	BPLL
bit 7						bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **PHR:** PWMxH Rising Edge Trigger Enable bit
 1 = Rising edge of PWMxH will trigger Leading-Edge Blanking counter
 0 = Leading-Edge Blanking ignores rising edge of PWMxH
- bit 14 **PHF:** PWMxH Falling Edge Trigger Enable bit
 1 = Falling edge of PWMxH will trigger Leading-Edge Blanking counter
 0 = Leading-Edge Blanking ignores falling edge of PWMxH
- bit 13 **PLR:** PWMxL Rising Edge Trigger Enable bit
 1 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter
 0 = Leading-Edge Blanking ignores rising edge of PWMxL
- bit 12 **PLF:** PWMxL Falling Edge Trigger Enable bit
 1 = Falling edge of PWMxL will trigger Leading-Edge Blanking counter
 0 = Leading-Edge Blanking ignores falling edge of PWMxL
- bit 11 **FLTLEBEN:** Fault Input Leading-Edge Blanking Enable bit
 1 = Leading-Edge Blanking is applied to selected Fault input
 0 = Leading-Edge Blanking is not applied to selected Fault input
- bit 10 **CLLEBEN:** Current-Limit Leading-Edge Blanking Enable bit
 1 = Leading-Edge Blanking is applied to selected current-limit input
 0 = Leading-Edge Blanking is not applied to selected current-limit input
- bit 9-6 **Unimplemented:** Read as '0'
- bit 5 **BCH:** Blanking in Selected Blanking Signal High Enable bit⁽¹⁾
 1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is high
 0 = No blanking when selected blanking signal is high
- bit 4 **BCL:** Blanking in Selected Blanking Signal Low Enable bit⁽¹⁾
 1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low
 0 = No blanking when selected blanking signal is low
- bit 3 **BPHH:** Blanking in PWMxH High Enable bit
 1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is high
 0 = No blanking when PWMxH output is high
- bit 2 **BPHL:** Blanking in PWMxH Low Enable bit
 1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low
 0 = No blanking when PWMxH output is low
- bit 1 **BPLH:** Blanking in PWMxL High Enable bit
 1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high
 0 = No blanking when PWMxL output is high
- bit 0 **BPLL:** Blanking in PWMxL Low Enable bit
 1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is low
 0 = No blanking when PWMxL output is low

Note 1: The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

NOTES:

FIGURE 18-1: SPIx MODULE BLOCK DIAGRAM

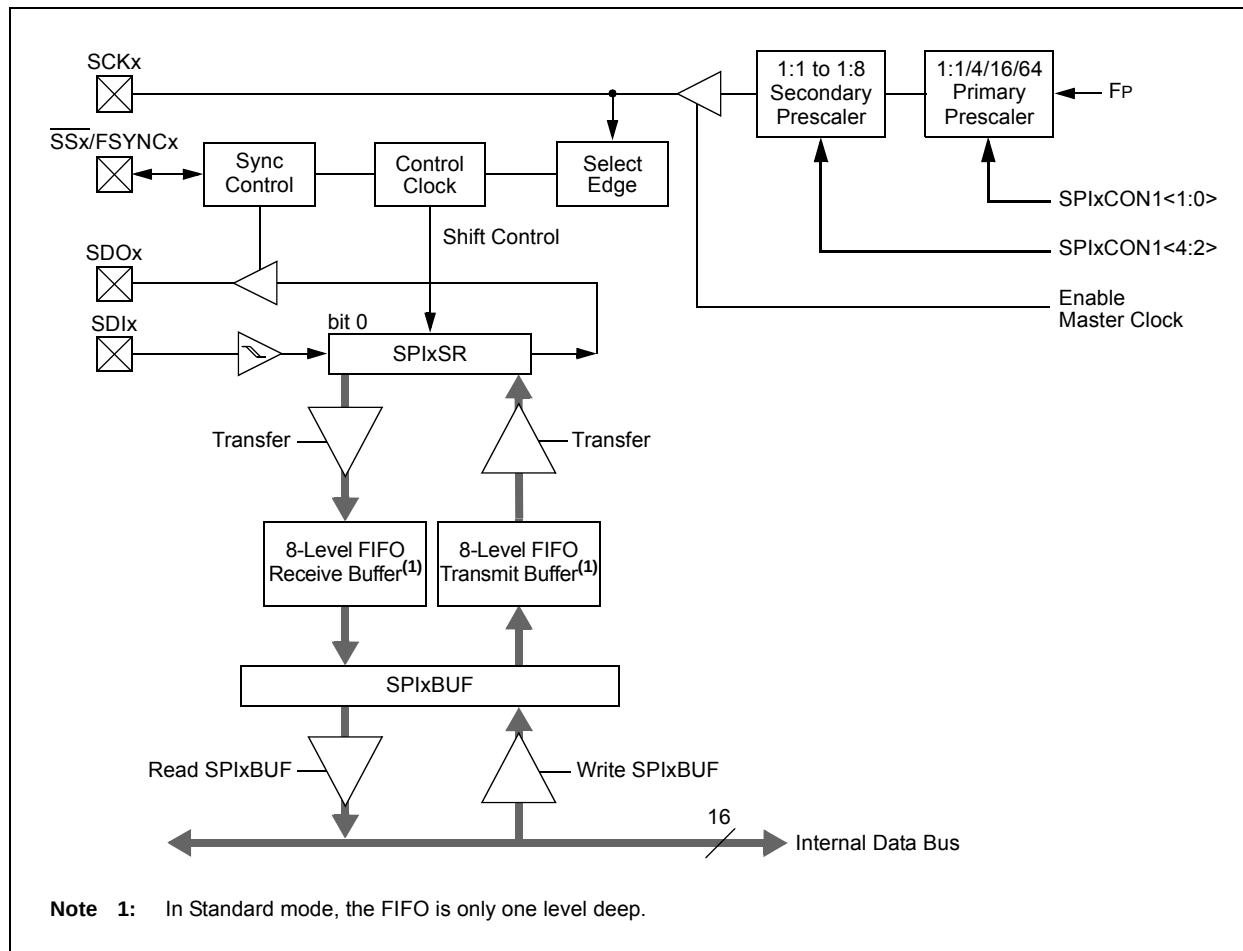
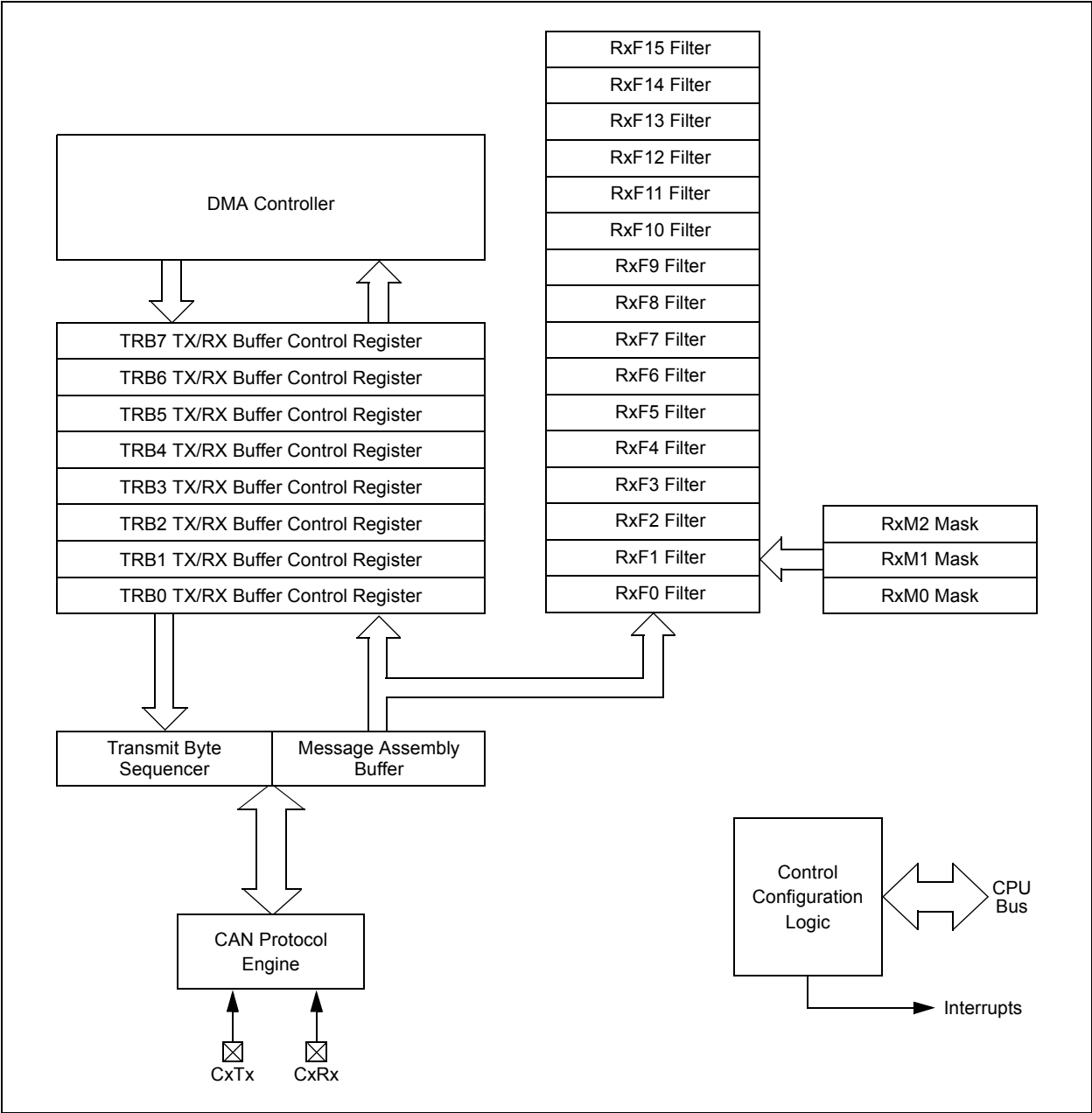


FIGURE 21-1: ECAN™ MODULE BLOCK DIAGRAM



REGISTER 21-4: CxFCTRL: ECANx FIFO CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
DMABS2	DMABS1	DMABS0	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FSA4	FSA3	FSA2	FSA1	FSA0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **DMABS<2:0>**: DMA Buffer Size bits

111 = Reserved

110 = 32 buffers in RAM

101 = 24 buffers in RAM

100 = 16 buffers in RAM

011 = 12 buffers in RAM

010 = 8 buffers in RAM

001 = 6 buffers in RAM

000 = 4 buffers in RAM

bit 12-5 **Unimplemented**: Read as '0'

bit 4-0 **FSA<4:0>**: FIFO Area Starts with Buffer bits

11111 = Read Buffer RB31

11110 = Read Buffer RB30

•

•

•

00001 = TX/RX Buffer TRB1

00000 = TX/RX Buffer TRB0

REGISTER 21-26: CxTRmnCON: ECANx TX/RX BUFFER mn CONTROL REGISTER
(m = 0,2,4,6; n = 1,3,5,7)

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI1	TXnPRI0
bit 15						bit 8	

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm ⁽¹⁾	TXLARBm ⁽¹⁾	TXERRm ⁽¹⁾	TXREQm	RTRENm	TXmPRI1	TXmPRI0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 See Definition for bits<7:0>, Controls Buffer n

bit 7 **TXENm**: TX/RX Buffer Selection bit

1 = Buffer TRBn is a transmit buffer

0 = Buffer TRBn is a receive buffer

bit 6 **TXABTm**: Message Aborted bit⁽¹⁾

1 = Message was aborted

0 = Message completed transmission successfully

bit 5 **TXLARBm**: Message Lost Arbitration bit⁽¹⁾

1 = Message lost arbitration while being sent

0 = Message did not lose arbitration while being sent

bit 4 **TXERRm**: Error Detected During Transmission bit⁽¹⁾

1 = A bus error occurred while the message was being sent

0 = A bus error did not occur while the message was being sent

bit 3 **TXREQm**: Message Send Request bit

1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent

0 = Clearing the bit to '0' while set requests a message abort

bit 2 **RTRENm**: Auto-Remote Transmit Enable bit

1 = When a remote transmit is received, TXREQ will be set

0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXmPRI<1:0>**: Message Transmission Priority bits

11 = Highest message priority

10 = High intermediate message priority

01 = Low intermediate message priority

00 = Lowest message priority

Note 1: This bit is cleared when TXREQ is set.

Note: The buffers, SID, EID, DLC, Data Field, and Receive Status registers are located in DMA RAM.

TABLE 24-1: PTG STEP COMMAND FORMAT (CONTINUED)

bit 3-0	Step Command	OPTION<3:0>	Option Description
	PTGWHI ⁽¹⁾ or PTGWLO ⁽¹⁾	0000	PWM Special Event Trigger. ⁽³⁾
		0001	PWM master time base synchronization output. ⁽³⁾
		0010	PWM1 interrupt. ⁽³⁾
		0011	PWM2 interrupt. ⁽³⁾
		0100	PWM3 interrupt. ⁽³⁾
		0101	Reserved.
		0110	Reserved.
		0111	OC1 Trigger event.
		1000	OC2 Trigger event.
		1001	IC1 Trigger event.
		1010	CMP1 Trigger event.
		1011	CMP2 Trigger event.
		1100	CMP3 Trigger event.
		1101	CMP4 Trigger event.
		1110	ADC conversion done interrupt.
		1111	INT2 external interrupt.
	PTGIRQ ⁽¹⁾	0000	Generate PTG Interrupt 0.
		0001	Generate PTG Interrupt 1.
		0010	Generate PTG Interrupt 2.
		0011	Generate PTG Interrupt 3.
		0100	Reserved.
		.	.
		.	.
		1111	Reserved.
	PTGTRIG ⁽²⁾	00000	PTGO0.
		00001	PTGO1.
		.	.
		.	.
		.	.
		11110	PTGO30.
		11111	PTGO31.

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 24-2 for the trigger output descriptions.

3: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

TABLE 24-2: PTG OUTPUT DESCRIPTIONS

PTG Output Number	PTG Output Description
PTGO0	Trigger/Synchronization Source for OC1
PTGO1	Trigger/Synchronization Source for OC2
PTGO2	Trigger/Synchronization Source for OC3
PTGO3	Trigger/Synchronization Source for OC4
PTGO4	Clock Source for OC1
PTGO5	Clock Source for OC2
PTGO6	Clock Source for OC3
PTGO7	Clock Source for OC4
PTGO8	Trigger/Synchronization Source for IC1
PTGO9	Trigger/Synchronization Source for IC2
PTGO10	Trigger/Synchronization Source for IC3
PTGO11	Trigger/Synchronization Source for IC4
PTGO12	Sample Trigger for ADC
PTGO13	Sample Trigger for ADC
PTGO14	Sample Trigger for ADC
PTGO15	Sample Trigger for ADC
PTGO16	PWM Time Base Synchronous Source for PWM ⁽¹⁾
PTGO17	PWM Time Base Synchronous Source for PWM ⁽¹⁾
PTGO18	Mask Input Select for Op Amp/Comparator
PTGO19	Mask Input Select for Op Amp/Comparator
PTGO20	Reserved
PTGO21	Reserved
PTGO22	Reserved
PTGO23	Reserved
PTGO24	Reserved
PTGO25	Reserved
PTGO26	Reserved
PTGO27	Reserved
PTGO28	Reserved
PTGO29	Reserved
PTGO30	PTG Output to PPS Input Selection
PTGO31	PTG Output to PPS Input Selection

Note 1: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**REGISTER 25-4: CMxMSKSRG: COMPARATOR x MASK SOURCE SELECT
CONTROL REGISTER (CONTINUED)**

bit 3-0 **SELSRCA<3:0>**: Mask A Input Select bits

1111 = FLT4
1110 = FLT2
1101 = PTGO19
1100 = PTGO18
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

**REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING
CONTROL REGISTER**

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **HLMS:** High or Low-Level Masking Select bits
1 = The masking (blanking) function will prevent any asserted ('0') comparator signal from propagating
0 = The masking (blanking) function will prevent any asserted ('1') comparator signal from propagating
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **OCEN:** OR Gate C Input Enable bit
1 = MCI is connected to OR gate
0 = MCI is not connected to OR gate
- bit 12 **OCNEN:** OR Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to OR gate
0 = Inverted MCI is not connected to OR gate
- bit 11 **OBEN:** OR Gate B Input Enable bit
1 = MBI is connected to OR gate
0 = MBI is not connected to OR gate
- bit 10 **OBNEN:** OR Gate B Input Inverted Enable bit
1 = Inverted MBI is connected to OR gate
0 = Inverted MBI is not connected to OR gate
- bit 9 **OAEN:** OR Gate A Input Enable bit
1 = MAI is connected to OR gate
0 = MAI is not connected to OR gate
- bit 8 **OANEN:** OR Gate A Input Inverted Enable bit
1 = Inverted MAI is connected to OR gate
0 = Inverted MAI is not connected to OR gate
- bit 7 **NAGS:** AND Gate Output Inverted Enable bit
1 = Inverted ANDI is connected to OR gate
0 = Inverted ANDI is not connected to OR gate
- bit 6 **PAGS:** AND Gate Output Enable bit
1 = ANDI is connected to OR gate
0 = ANDI is not connected to OR gate
- bit 5 **ACEN:** AND Gate C Input Enable bit
1 = MCI is connected to AND gate
0 = MCI is not connected to AND gate
- bit 4 **ACNEN:** AND Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to AND gate
0 = Inverted MCI is not connected to AND gate

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DI10 DI18 DI19	V _{IL}	Input Low Voltage					
		Any I/O Pin and $\overline{\text{MCLR}}$	V _{SS}	—	0.2 V _{DD}	V	
		I/O Pins with SDAx, SCLx	V _{SS}	—	0.3 V _{DD}	V	SMBus disabled
		I/O Pins with SDAx, SCLx	V _{SS}	—	0.8	V	SMBus enabled
DI20	V _{IH}	Input High Voltage					
		I/O Pins Not 5V Tolerant	0.8 V _{DD}	—	V _{DD}	V	(Note 3)
		I/O Pins 5V Tolerant and $\overline{\text{MCLR}}$	0.8 V _{DD}	—	5.5	V	(Note 3)
		I/O Pins with SDAx, SCLx	0.8 V _{DD}	—	5.5	V	SMBus disabled
		I/O Pins with SDAx, SCLx	2.1	—	5.5	V	SMBus enabled
DI30	ICNPU	Change Notification Pull-up Current	150	250	550	μA	V _{DD} = 3.3V, V _{PIN} = V _{SS}
DI31	ICNPD	Change Notification Pull-Down Current⁽⁴⁾	20	50	100	μA	V _{DD} = 3.3V, V _{PIN} = V _{DD}

Note 1: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

3: See the “Pin Diagrams” section for the 5V tolerant I/O pins.

4: V_{IL} source < (V_{SS} – 0.3). Characterized but not tested.

5: Non-5V tolerant pins V_{IH} source > (V_{DD} + 0.3), 5V tolerant pins V_{IH} source > 5.5V. Characterized but not tested.

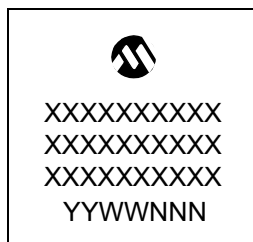
6: Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.

7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

8: Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

33.1 Package Marking Information (Continued)

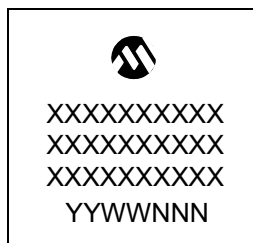
36-Lead VTLA (TLA)



Example



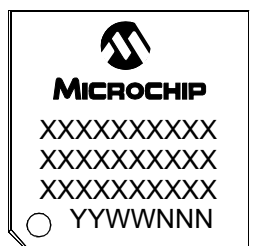
44-Lead VTLA (TLA)



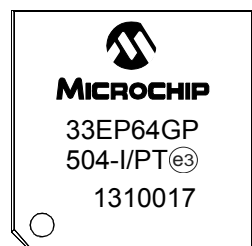
Example



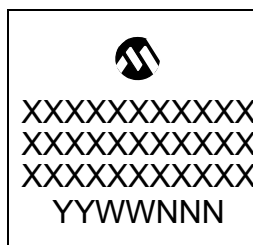
44-Lead TQFP



Example



44-Lead QFN (8x8x0.9 mm)

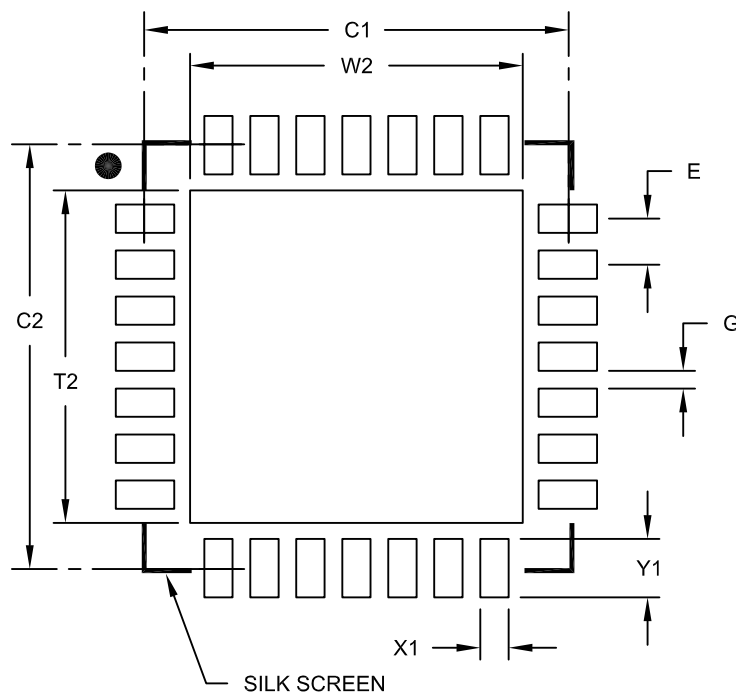


Example



**28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S]
with 0.40 mm Contact Length**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (Y28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A

INDEX

A

Absolute Maximum Ratings	401
AC Characteristics	413, 471
10-Bit ADC Conversion Requirements	465
12-Bit ADC Conversion Requirements	463
ADC Module	459
ADC Module (10-Bit Mode)	461, 473
ADC Module (12-Bit Mode)	460, 473
Capacitive Loading Requirements on Output Pins	413
DMA Module Requirements	465
ECANx I/O Requirements	454
External Clock	414
High-Speed PWMx Requirements	422
I/O Timing Requirements	416
I2Cx Bus Data Requirements (Master Mode)	451
I2Cx Bus Data Requirements (Slave Mode)	453
Input Capture x Requirements	420
Internal FRC Accuracy	415
Internal LPRC Accuracy	415
Internal RC Accuracy	472
Load Conditions	413, 471
OCx/PWMx Mode Requirements	421
Op Amp/Comparator Voltage Reference Settling Time Specifications	457
Output Compare x Requirements	421
PLL Clock	415, 471
QE1 External Clock Requirements	423
QE1 Index Pulse Requirements	425
Quadrature Decoder Requirements	424
Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer Requirements	417
SPI1 Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1) Requirements	441
SPI1 Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1) Requirements	440
SPI1 Master Mode (Half-Duplex, Transmit Only) Requirements	439
SPI1 Maximum Data/Clock Rate Summary	438
SPI1 Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0) Requirements	449
SPI1 Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0) Requirements	447
SPI1 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0) Requirements	443
SPI1 Slave Mode (Full-Duplex, CKE = 1, CKP = 1, SMP = 0) Requirements	445
SPI2 Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1) Requirements	429
SPI2 Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1) Requirements	428
SPI2 Master Mode (Half-Duplex, Transmit Only) Requirements	427
SPI2 Maximum Data/Clock Rate Summary	426
SPI2 Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0) Requirements	437
SPI2 Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0) Requirements	435
SPI2 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0) Requirements	431
SPI2 Slave Mode (Full-Duplex, CKE = 1, CKP = 1, SMP = 0) Requirements	433

Timer1 External Clock Requirements	418
Timer2/Timer4 External Clock Requirements	419
Timer3/Timer5 External Clock Requirements	419
UARTx I/O Requirements	454
ADC	
Control Registers	325
Helpful Tips	324
Key Features	321
Resources	324
Arithmetic Logic Unit (ALU)	44
Assembler	
MPASM Assembler	398
B	
Bit-Reversed Addressing	115
Example	116
Implementation	115
Sequence Table (16-Entry)	116
Block Diagrams	
Data Access from Program Space	
Address Generation	117
16-Bit Timer1 Module	203
ADC Conversion Clock Period	323
ADC with Connection Options for ANx Pins and Op Amps	322
Arbiter Architecture	110
BEMF Voltage Measurement Using ADC	34
Boost Converter Implementation	32
CALL Stack Frame	111
Comparator (Module 4)	356
Connections for On-Chip Voltage Regulator	384
CPU Core	36
CRC Module	373
CRC Shift Engine	374
CTMU Module	316
Digital Filter Interconnect	357
DMA Controller	141
DMA Controller Module	139
dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X	25
ECAN Module	288
EDS Read Address Generation	105
EDS Write Address Generation	106
Example of MCLR Pin Connections	30
High-Speed PWMx Architectural Overview	227
High-Speed PWMx Register Interconnection	228
I2Cx Module	274
Input Capture x	213
Interleaved PFC	34
Multiphase Synchronous Buck Converter	33
Multiplexing Remappable Output for RPN	180
Op Amp Configuration A	358
Op Amp Configuration B	359
Op Amp/Comparator Voltage Reference Module	356
Op Amp/Comparator x (Modules 1, 2, 3)	355
Oscillator System	153
Output Compare x Module	219
PLL	154
Programmer's Model	38
PTG Module	338
Quadrature Encoder Interface	250
Recommended Minimum Connection	30