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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24К х 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc506-h-pt

Email: info@E-XFL.COM

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TABLE 4-42: OP AMP/COMPARATOR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	0A80	PSIDL	—	—	—	C4EVT	C3EVT	C2EVT	C1EVT	—	-	—	—	C4OUT	C3OUT	C2OUT	C10UT	0000
CVRCON	0A82	_	CVR2OE	_	_	_	VREFSEL	_	—	CVREN	CVR10E	CVRR	CVRSS		CVR<	3:0>		0000
CM1CON	0A84	CON	COE	CPOL	—		OPMODE	CEVT	COUT	EVPO	_<1:0>	—	CREF		_	CCH	<1:0>	0000
CM1MSKSRC	0A86		—		—		SELSR	CC<3:0>			SELSRC	B<3:0>			SELSRC	A<3:0>		0000
CM1MSKCON	0A88	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM1FLTR	0A8A		—		—		_		—		C	FSEL<2:0	>	CFLTREN	0	CFDIV<2:0	>	0000
CM2CON	0A8C	CON	COE	CPOL	—		OPMODE	CEVT	COUT	EVPO	_<1:0>	—	CREF		_	CCH	<1:0>	0000
CM2MSKSRC	0A8E		—		—		SELSR	CC<3:0>			SELSRC	B<3:0>			SELSRC	A<3:0>		0000
CM2MSKCON	0A90	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM2FLTR	0A92		—		—		—		—		C	FSEL<2:0	>	CFLTREN	0	CFDIV<2:0	>	0000
CM3CON ⁽¹⁾	0A94	CON	COE	CPOL	—		OPMODE	CEVT	COUT	EVPO	_<1:0>	—	CREF		_	CCH	<1:0>	0000
CM3MSKSRC(1)	0A96		—		—		SELSR	CC<3:0>			SELSRC	B<3:0>			SELSRC	A<3:0>		0000
CM3MSKCON ⁽¹⁾	0A98	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM3FLTR ⁽¹⁾	0A9A	_	_	_	_	_	_	_	_	_	C	FSEL<2:0	>	CFLTREN	(CFDIV<2:0	>	0000
CM4CON	0A9C	CON	COE	CPOL	_	_	_	CEVT	COUT	EVPO	_<1:0>	_	CREF	_	_	CCH	<1:0>	0000
CM4MSKSRC	0A9E		—		—		SELSR	CC<3:0>			SELSRC	B<3:0>			SELSRC	A<3:0>		0000
CM4MSKCON	0AA0	HLMS	_	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM4FLTR	0AA2	_	—	—	—	—	-	—	_	—	C	FSEL<2:0	>	CFLTREN	(CFDIV<2:0	>	0000

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are unavailable on dsPIC33EPXXXGP502/MC502/MC502/MC202 and PIC24EP256GP/MC202 (28-pin) devices.

TABLE 4-43: CTMU REGISTER MAP

File	Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CTML	JCON1	033A	CTMUEN	-	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	—	—	-	—			—	—	0000
CTML	JCON2	033C	EDG1MOD	EDG1POL		EDG1	SEL<3:0>		EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL		EDG2S	EL<3:0>		_		0000
CTML	JICON	033E			ITRIM<5	5:0>			IRNG	6<1:0>	—	_		_	_	_			0000

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-44: JTAG INTERFACE REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
JDATAH	0FF0	—	_	—	—		JDATAH<27:16> xxz					xxxx						
JDATAL	0FF2						JDATAL<15:0> 001						0000					

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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4.6 Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either Data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y Data Spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

4.6.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified, and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note:	Y space Modulo Addressing EA calcula-
	tions assume word-sized data (LSb of
	every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.6.2 W ADDRESS REGISTER SELECTION

The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = 1111, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = 1111, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X Data Space when XWM is set to any value other than '1111' and the XMODEN bit is set (MODCON<15>).

The Y Address Space Pointer W register (YWM), to which Modulo Addressing is to be applied, is stored in MODCON<7:4>. Modulo Addressing is enabled for Y Data Space when YWM is set to any value other than '1111' and the YMODEN bit is set at MODCON<14>.



FIGURE 4-20: MODULO ADDRESSING OPERATION EXAMPLE

8.0 DIRECT MEMORY ACCESS (DMA)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Direct Memory Access (DMA)" (DS70348) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The DMA Controller transfers data between Peripheral Data registers and Data Space SRAM

In addition, DMA can access the entire data memory space. The Data Memory Bus Arbiter is utilized when either the CPU or DMA attempts to access SRAM, resulting in potential DMA or CPU stalls.

The DMA Controller supports 4 independent channels. Each channel can be configured for transfers to or from selected peripherals. Some of the peripherals supported by the DMA Controller include:

- ECAN[™]
- Analog-to-Digital Converter (ADC)
- Serial Peripheral Interface (SPI)
- UART
- Input Capture
- Output Compare

Refer to Table 8-1 for a complete list of supported peripherals.

FIGURE 8-1: DMA CONTROLLER MODULE



R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
ROON		ROSSLP	ROSEL	RODIV3 ⁽¹⁾	RODIV2 ⁽¹⁾	RODIV1 ⁽¹⁾	RODIV0 ⁽¹⁾		
bit 15				•		•	bit 8		
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
		<u> </u>				<u> </u>			
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'			
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown		
bit 15	ROON: Refer	ence Oscillato	Output Enab	ole bit					
Sit 10	1 = Reference 0 = Reference	e oscillator outr e oscillator outr	but is enabled	on the REFCL	.K pin ⁽²⁾				
bit 14	Unimplemen	ted: Read as '	o'						
bit 13	. 13 ROSSLP: Reference Oscillator Run in Sleep bit								
	1 = Reference	e oscillator outp	out continues	to run in Sleep					
	0 = Reference	e oscillator outp	out is disabled	l in Sleep					
bit 12	ROSEL: Refe	erence Oscillato	or Source Sel	ect bit					
	1 = Oscillator	crystal is used	as the refere	nce clock					
hit 11_8		Peference Os	cillator Divide	r hite(1)					
Dit 11-0	1111 = Refer	ence clock divi	ded by 32 76	R					
	1110 = Refer	ence clock divi	ded by 16,384	4					
	1101 = Refer	ence clock divi	ded by 8,192						
	1100 = Refer	ence clock divi	ded by 4,096						
	1011 = Refer	ence clock divi	ded by 2,048						
	1010 = Relef	ence clock divi	ded by 1,024 ded by 512						
	1000 = Refer	ence clock divi	ded by 256						
	0111 = Refer	ence clock divi	ded by 128						
	0110 = Refer	ence clock divi	ded by 64						
	0101 = Refer	ence clock divi	ded by 32						
	0100 = Refer	ence clock divi	ded by 16						
	0011 = Refer	ence clock divi	ded by 6 ded by 4						
	0001 = Refer	ence clock divi	ded by 2						
	0000 = Refer	ence clock	-						
bit 7-0	Unimplemen	ted: Read as '	כ'						

REGISTER 9-5: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

- **Note 1:** The reference oscillator output must be disabled (ROON = 0) before writing to these bits.
 - 2: This pin is remappable. See Section 11.4 "Peripheral Pin Select (PPS)" for more information.

10.2.1 SLEEP MODE

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- · Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into Standby when Sleep mode is entered by clearing the VREGS (RCON<8>) and VREGSF (RCON<11>) bits (default configuration).

If the application requires a faster wake-up time, and can accept higher current requirements, the VREGS (RCON<8>) and VREGSF (RCON<11>) bits can be set to keep the internal regulator and the Flash regulator active during Sleep mode.

10.2.2 IDLE MODE

The following occurs in Idle mode:

- The CPU stops executing instructions.
- · The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see Section 10.4 "Peripheral Module Disable").
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- · Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction or the first instruction in the Interrupt Service Routine (ISR).

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral; for example, the TSIDL bit in the Timer1 Control register (T1CON<13>).

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
_	—	—	_	—	PWM3MD ⁽¹⁾	PWM2MD ⁽¹⁾	PWM1MD ⁽¹⁾
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—		_		_		
bit 7							bit 0
Legend:							
R = Readab	ole bit	W = Writable	bit	U = Unimplen	nented bit, read	l as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-11	Unimplemen	ted: Read as '	0'				
bit 10	PWM3MD: P	WM3 Module D)isable bit ⁽¹⁾				
	1 = PWM3 mo	odule is disable	ed				
	0 = PWM3 mo	odule is enable	d				
bit 9	PWM2MD: P	WM2 Module D	isable bit ⁽¹⁾				
	1 = PWM2 mo	odule is disable	ed				
	0 = PWM2 mc	odule is enable	d				
bit 8	PWM1MD: P	WM1 Module D	isable bit ⁽¹⁾				
	1 = PWM1 mo	odule is disable	ed				
	0 = PWM1 mo	odule is enable	d				
bit 7-0	Unimplemen	ted: Read as '	0'				

REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

Note 1: This bit is available on dsPIC33EPXXXMC50X/20X and PIC24EPXXXMC20X devices only.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	—	—	—	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				U1RXR<6:0	>		
bit 7							bit 0
-							

REGISTER 11-10: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 Unimplemented: Read as '0' bit 6-0 U1RXR<6:0>: Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121

REGISTER 11-11: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_		_	—	_	—	_
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				U2RXR<6:0>	>		
bit 7							bit 0
Legend:							

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15-7 Unimplemented: Read as '0'

^{0000000 =} Input tied to Vss



FIGURE 13-3: TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)

3: Timery is a Type C timer (y = 3 and 5).

Timerx/y Resources 13.1

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/
	wwwproducts/Devices.aspx?d
	DocName=en555464

KEY RESOURCES 13.1.1

- "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- · Software Libraries
- · Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 16-7: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)

bit 7-	6	DTC<1:0>: Dead-Time Control bits
		11 = Dead-Time Compensation mode
		10 = Dead-time function is disabled
		01 = Negative dead time is actively applied for Complementary Output mode
		00 = Positive dead time is actively applied for all output modes
bit 5		DTCP: Dead-Time Compensation Polarity bit ⁽³⁾
		When Set to '1':
		If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened. If DTCMPx = 1, PWMxH is shortened and PWMxL is lengthened.
		When Set to '0':
		If $DTCMPx = 0$, $PWMxH$ is shortened and $PWMxL$ is lengthened.
		If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened.
bit 4		Unimplemented: Read as '0'
bit 3		MTBS: Master Time Base Select bit
		 1 = PWM generator uses the secondary master time base for synchronization and as the clock source for the PWM generation logic (if secondary time base is available)
		0 = PWM generator uses the primary master time base for synchronization and as the clock source for the PWM generation logic
bit 2		CAM: Center-Aligned Mode Enable bit ^(2,4)
		1 = Center-Aligned mode is enabled
		0 = Edge-Aligned mode is enabled
bit 1		XPRES: External PWMx Reset Control bit ⁽⁵⁾
		 1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
		0 = External pins do not affect PWMx time base
bit 0		IUE: Immediate Update Enable bit ⁽²⁾
		1 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are immediate
		 Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are synchronized to the PWMx period boundary
Note	1:	Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
	2:	These bits should not be changed after the PWMx is enabled (PTEN = 1).
	3:	DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.
	4:	The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.

5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

					-						
R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0				
CON	COE ⁽²⁾	CPOL			OPMODE	CEVT	COUT				
bit 15							bit 8				
R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0				
EVPOL1	EVPOL0	<u> </u>	CREF ⁽¹⁾			CCH1 ⁽¹⁾	CCH0 ⁽¹⁾				
bit 7							bit 0				
Legend:											
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, read	as '0'					
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown				
L:1 4 F			F achle 6:4								
DIL 15	1 = Op amp/c	ip/Comparator									
	1 = Op amp/o 0 = Op amp/o	comparator is d	isabled								
bit 14	COE: Compa	arator Output E	nable bit ⁽²⁾								
	1 = Compara	tor output is pr	esent on the C	xOUT pin							
	0 = Compara	tor output is int	ernal only								
bit 13	CPOL: Comp	CPOL: Comparator Output Polarity Select bit									
	1 = Compara	tor output is inv	/erted								
	0 = Compara	tor output is no	t inverted								
bit 12-11	Unimplemen	nted: Read as '	0'								
bit 10	OPMODE: O	PMODE: Op Amp/Comparator Operation Mode Select bit									
	1 = Circuit op	perates as an o	p amp								
bit Q	CEVT: Comp	arator Event bi	Hiparator H								
bit 9	UEVI: Comparator event according to the EVPOL <1:05 settings occurred; disables future triggers and $1 = 0$										
	interrupt	s until the bit is	cleared				e inggers and				
	0 = Compara	ator event did n	ot occur								
bit 8	COUT: Comp	parator Output I	bit								
	When CPOL	= 0 (non-invert	ed polarity):								
	1 = VIN + > VI	N-									
	U = VIN + < VI	= 1 (invorted p	olarity):								
	1 = VIN + < VI	<u> </u>	olanty).								
	0 = VIN+ > VI	N-									
Note 1: Inn	uts that are sele	ected and not a	vailable will be	tied to Vss. S	ee the " Pin Dia	grams" section	n for available				

REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2 OR 3)

- **Note 1:** Inputs that are selected and not available will be tied to Vss. See the "**Pin Diagrams**" section for available inputs for each package.
 - **2:** This output is not available when OPMODE (CMxCON<10>) = 1.

REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2 OR 3) (CONTINUED)

bit 7-6	EVPOL<1:0>: Trigger/Event/Interrupt Polarity Select bits
	 11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0) 10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
	If CPOL = 1 (inverted polarity): Low-to-high transition of the comparator output.
	If CPOL = 0 (non-inverted polarity): High-to-low transition of the comparator output.
	01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity-selected comparator output (while CEVT = 0)
	If CPOL = 1 (inverted polarity): High-to-low transition of the comparator output.
	If CPOL = 0 (non-inverted polarity): Low-to-high transition of the comparator output
	00 = Trigger/event/interrupt generation is disabled
bit 5	Unimplemented: Read as '0'
bit 4	CREF: Comparator Reference Select bit (VIN+ input) ⁽¹⁾
	 1 = VIN+ input connects to internal CVREFIN voltage⁽²⁾ 0 = VIN+ input connects to CxIN1+ pin
bit 3-2	Unimplemented: Read as '0'
bit 1-0	CCH<1:0>: Op Amp/Comparator Channel Select bits ⁽¹⁾
	 11 = Unimplemented 10 = Unimplemented 01 = Inverting input of the comparator connects to the CxIN2- pin⁽²⁾ 00 = Inverting input of the op amp/comparator connects to the CxIN1- pin

- **Note 1:** Inputs that are selected and not available will be tied to Vss. See the "**Pin Diagrams**" section for available inputs for each package.
 - 2: This output is not available when OPMODE (CMxCON<10>) = 1.

DC CH	ARACTE	RISTICS	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Symbol	Characteristic	Min. Typ. Max. Units Conditions						
	VIL	Input Low Voltage							
DI10		Any I/O Pin and MCLR	Vss	—	0.2 VDD	V			
DI18		I/O Pins with SDAx, SCLx	Vss	_	0.3 VDD	V	SMBus disabled		
DI19		I/O Pins with SDAx, SCLx	Vss	—	0.8	V	SMBus enabled		
	Vih	Input High Voltage							
DI20		I/O Pins Not 5V Tolerant	0.8 VDD	—	Vdd	V	(Note 3)		
		I/O Pins 5V Tolerant and MCLR	0.8 VDD	—	5.5	V	(Note 3)		
		I/O Pins with SDAx, SCLx	0.8 VDD	_	5.5	V	SMBus disabled		
		I/O Pins with SDAx, SCLx	2.1	—	5.5	V	SMBus enabled		
	ICNPU	Change Notification Pull-up Current							
DI30			150	250	550	μA	VDD = 3.3V, VPIN = VSS		
	ICNPD	Change Notification Pull-Down Current ⁽⁴⁾							
DI31			20	50	100	μA	VDD = 3.3V, VPIN = VDD		

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 2: Negative current is defined as current sourced by the pin.
- 3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 4: VIL source < (VSS 0.3). Characterized but not tested.

5: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

- 6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

DC CHARACTERISTICS			$\begin{tabular}{ l l l l l l l l l l l l l l l l l l l$					
Param No.	Symbol	Characteristic	Min. Typ. ⁽¹⁾ Max. Units Conditions					
		Program Flash Memory						
D130	Eр	Cell Endurance	10,000		_	E/W	-40°C to +125°C	
D131	Vpr	VDD for Read	3.0		3.6	V		
D132b	VPEW	VDD for Self-Timed Write	3.0		3.6	V		
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C	
D135	IDDP	Supply Current during Programming ⁽²⁾	—	10	—	mA		
D136	IPEAK	Instantaneous Peak Current During Start-up	_	_	150	mA		
D137a	Тре	Page Erase Time	17.7	—	22.9	ms	TPE = 146893 FRC cycles, Ta = +85°C (See Note 3)	
D137b	Тре	Page Erase Time	17.5	_	23.1	ms	TPE = 146893 FRC cycles, TA = +125°C (See Note 3)	
D138a	Tww	Word Write Cycle Time	41.7	_	53.8	μs	Tww = 346 FRC cycles, TA = +85°C (See Note 3)	
D138b	Tww	Word Write Cycle Time	41.2	—	54.4	μs	Tww = 346 FRC cycles, Ta = +125°C (See Note 3)	

TABLE 30-14: DC CHARACTERISTICS: PROGRAM MEMORY

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: Parameter characterized but not tested in manufacturing.

3: Other conditions: FRC = 7.37 MHz, TUN<5:0> = 011111 (for Minimum), TUN<5:0> = 100000 (for Maximum). This parameter depends on the FRC accuracy (see Table 30-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). For complete details on calculating the Minimum and Maximum time, see Section 5.3 "Programming Operations".



AC CHARACTERISTICS			Standard Ope (unless other) Operating tem	rating Co wise state perature	pnditions: 3.0V to 3.6V ed) $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended			
Param No.	Symb	Characteristic	Min.	Тур. ⁽¹⁾	Max.	Units	Conditions	
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	_	60	MHz	EC	
		Oscillator Crystal Frequency	3.5 10	—	10 25	MHz MHz	XT HS	
OS20	Tosc	Tosc = 1/Fosc	8.33	—	DC	ns	+125°C	
		Tosc = 1/Fosc	7.14	—	DC	ns	+85°C	
OS25	TCY	Instruction Cycle Time ⁽²⁾	16.67	—	DC	ns	+125°C	
		Instruction Cycle Time ⁽²⁾	14.28	—	DC	ns	+85°C	
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.45 x Tosc	—	0.55 x Tosc	ns	EC	
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC	
OS40	TckR	CLKO Rise Time ^(3,4)	—	5.2	—	ns		
OS41	TckF	CLKO Fall Time ^(3,4)	—	5.2	—	ns		
OS42	Gм	External Oscillator Transconductance ⁽⁴⁾	—	12	—	mA/V	HS, VDD = 3.3V, TA = +25°C	
			—	6	—	mA/V	XT, VDD = 3.3V, TA = +25°C	

TABLE 30-17: EXTERNAL CLOCK TIMING REQUIREMENTS

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- 2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Minimum" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Maximum" cycle time limit is "DC" (no clock) for all devices.
- 3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.
- 4: This parameter is characterized, but not tested in manufacturing.

TABLE 30-39:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)TIMING REQUIREMENTS

АС СНА	ARACTERIS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param.	Symbol	Characteristic ⁽¹⁾	Min. Typ. ⁽²⁾ Max. Units Conditions				Conditions
SP70	FscP	Maximum SCK2 Input Frequency			15	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—		—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—		—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—		—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—		_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30		_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120		_	ns	
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	_	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	_	_	ns	(Note 4)

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

рс сн	ARACTERIS	STICS	Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)(1)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial						
					-40°C ≤ TA	.≤+125°	C for Extended		
Param No. Symbol Characteristic		Min.	Тур. ⁽²⁾	Max.	Units	Conditions			
Compa	rator AC Ch	naracteristics							
CM10	Tresp	Response Time ⁽³⁾	_	19	_	ns	V+ input step of 100 mV, V- input held at VDD/2		
CM11	Тмс2о∨	Comparator Mode Change to Output Valid	10 μs						
Compa	Comparator DC Characteristics								
CM30	VOFFSET	Comparator Offset Voltage	—	±10	40	mV			
CM31	VHYST	Input Hysteresis Voltage ⁽³⁾	_	30	—	mV			
CM32	Trise/ Tfall	Comparator Output Rise/ Fall Time ⁽³⁾	—	20	—	ns	1 pF load capacitance on input		
CM33	Vgain	Open-Loop Voltage Gain ⁽³⁾	—	90	—	db			
CM34	VICM	Input Common-Mode Voltage	AVss	—	AVdd	V			
Op Am	p AC Chara	cteristics							
CM20	SR	Slew Rate ⁽³⁾		9		V/µs	10 pF load		
CM21a	Рм	Phase Margin (Configuration A) ^(3,4)	_	55	—	Degree	G = 100V/V; 10 pF load		
CM21b	Рм	Phase Margin (Configuration B) ^(3,5)	—	40	_	Degree	G = 100V/V; 10 pF load		
CM22	Gм	Gain Margin ⁽³⁾	—	20	—	db	G = 100V/V; 10 pF load		
CM23a	GBW	Gain Bandwidth (Configuration A) ^(3,4)	_	10	—	MHz	10 pF load		
CM23b	Gвw	Gain Bandwidth (Configuration B) ^(3,5)	—	6	_	MHz	10 pF load		

TABLE 30-53: OP AMP/COMPARATOR SPECIFICATIONS

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

- 2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
- 3: Parameter is characterized but not tested in manufacturing.
- 4: See Figure 25-6 for configuration information.
- 5: See Figure 25-7 for configuration information.
- 6: Resistances can vary by ±10% between op amps.

33.1 Package Marking Information (Continued)



28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	N	ILLIMETER	S	
Dimension	MIN	NOM	MAX	
Contact Pitch E			1.27 BSC	
Contact Pad Spacing	С		9.40	
Contact Pad Width (X28)	Х			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads		7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-187C Sheet 1 of 2

Revision C (December 2011)

This revision includes typographical and formatting changes throughout the data sheet text.

In addition, where applicable, new sections were added to each peripheral chapter that provide information and links to related resources, as well as helpful tips. For examples, see Section 20.1 "UART Helpful Tips" and Section 3.6 "CPU Resources". All occurrences of TLA were updated to VTLA throughout the document, with the exception of the pin diagrams (updated diagrams were not available at time of publication).

A new chapter, Section 31.0 "DC and AC Device Characteristics Graphs", was added.

All other major changes are referenced by their respective section in Table A-2.

Section Name	Update Description
"16-bit Microcontrollers and Digital Signal Controllers (up to 256-Kbyte Flash and 32-Kbyte SRAM) with High- Speed PWM, Op amps, and Advanced Analog"	The content on the first page of this section was extensively reworked to provide the reader with the key features and functionality of this device family in an "at-a-glance" format.
Section 1.0 "Device Overview"	Updated the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X Block Diagram (see Figure 1-1), which now contains a CPU block and a reference to the CPU diagram. Updated the description and Note references in the Pinout I/O Descriptions for these pins: C1IN2- C2IN2- C3IN2- OA1OUT OA2OUT and OA3OUT (see Table 1-1)
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers"	Updated the Recommended Minimum Connection diagram (see Figure 2-1).
Section 3.0 "CPU"	Updated the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X CPU Block Diagram (see Figure 3-1). Updated the Status register definition in the Programmer's Model (see Figure 3-2).
Section 4.0 "Memory Organization"	Updated the Data Memory Maps (see Figure 4-6 and Figure 4-11). Removed the DCB<1:0> bits from the OC1CON2, OC2CON2, OC3CON2, and OC4CON2 registers in the Output Compare 1 Through Output Compare 4 Register Map (see Table 4-10). Added the TRIG1 and TRGCON1 registers to the PWM Generator 1 Register Map (see Table 4-13). Added the TRIG2 and TRGCON2 registers to the PWM Generator 2 Register Map (see Table 4-14). Added the TRIG3 and TRGCON3 registers to the PWM Generator 3 Register Map (see Table 4-15). Updated the second note in Section 4.7.1 "Bit-Reversed Addressing Implementation".
Section 8.0 "Direct Memory Access (DMA)"	Updated the DMA Controller diagram (see Figure 8-1).
Section 14.0 "Input Capture"	Updated the bit values for the ICx clock source of the ICTSEL<12:10> bits in the ICxCON1 register (see Register 14-1).
Section 15.0 "Output Compare"	Updated the bit values for the OCx clock source of the OCTSEL<2:0> bits in the OCxCON1 register (see Register 15-1). Removed the DCB<1:0> bits from the Output Compare x Control Register 2 (see Register 15-2).

TABLE A-2: MAJOR SECTION UPDATES