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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc506-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc506-i-pt</a>

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name <sup>(4)</sup>	Pin Type	Buffer Type	PPS	Description
U2CTS	I	ST	No	UART2 Clear-To-Send.
U2RTS	O	—	No	UART2 Ready-To-Send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
BCLK2	O	ST	No	UART2 IrDA <sup>®</sup> baud clock output.
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	No	SPI1 data in.
SDO1	O	—	No	SPI1 data out.
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS <sup>(5)</sup>	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.
C1RX <sup>(2)</sup>	I	ST	Yes	ECAN1 bus receive pin.
C1TX <sup>(2)</sup>	O	—	Yes	ECAN1 bus transmit pin.
FLT1 <sup>(1)</sup> , FLT2 <sup>(1)</sup>	I	ST	Yes	PWM Fault Inputs 1 and 2.
FLT3 <sup>(1)</sup> , FLT4 <sup>(1)</sup>	I	ST	No	PWM Fault Inputs 3 and 4.
FLT32 <sup>(1,3)</sup>	I	ST	No	PWM Fault Input 32 (Class B Fault).
DTCMP1-DTCMP3 <sup>(1)</sup>	I	ST	Yes	PWM Dead-Time Compensation Inputs 1 through 3.
PWM1L-PWM3L <sup>(1)</sup>	O	—	No	PWM Low Outputs 1 through 3.
PWM1H-PWM3H <sup>(1)</sup>	O	—	No	PWM High Outputs 1 through 3.
SYNCI1 <sup>(1)</sup>	I	ST	Yes	PWM Synchronization Input 1.
SYNCO1 <sup>(1)</sup>	O	—	Yes	PWM Synchronization Output 1.
INDX1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Index1 pulse input.
HOME1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Home1 pulse input.
QEA1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Phase A input in QE11 mode. Auxiliary timer external clock/gate input in Timer mode.
QEB1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Phase B input in QE11 mode. Auxiliary timer external clock/gate input in Timer mode.
CNTCMP1 <sup>(1)</sup>	O	—	Yes	Quadrature Encoder Compare Output 1.

**Legend:** CMOS = CMOS compatible input or output      Analog = Analog input      P = Power  
ST = Schmitt Trigger input with CMOS levels      O = Output      I = Input  
PPS = Peripheral Pin Select      TTL = TTL input buffer

- Note 1:** This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- 2:** This pin is available on dsPIC33EPXXXGP/MC50X devices only.
- 3:** This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 “High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”** for more information.
- 4:** Not all pins are available in all packages variants. See the **“Pin Diagrams”** section for pin availability.
- 5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

### 3.6 CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

<b>Note:</b> In the event you are not able to access the product page using the link above, enter this URL in your browser: <a href="http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464">http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464</a>
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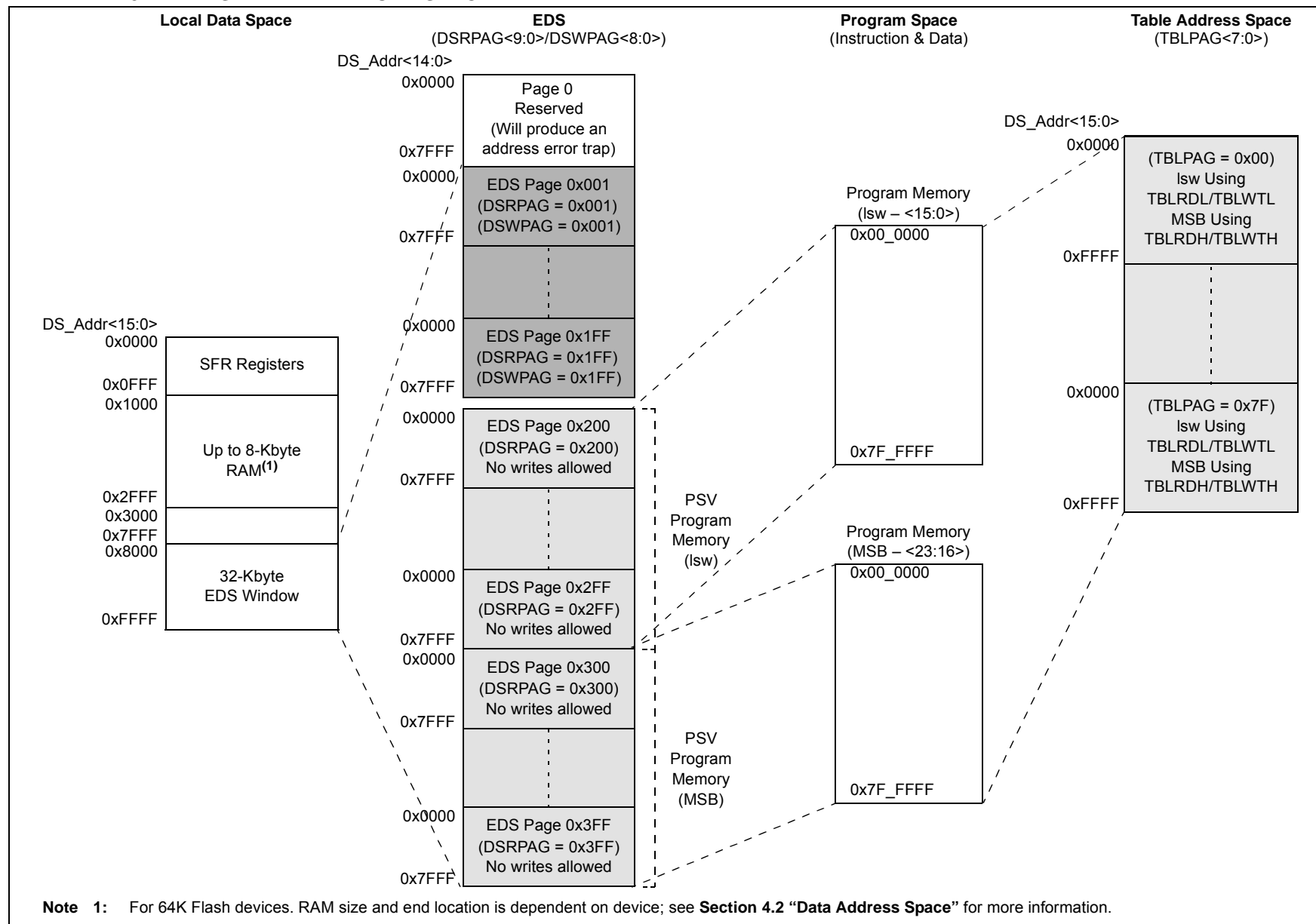
#### 3.6.1 KEY RESOURCES

- “**CPU**” (DS70359) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

**TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMIF	M12C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	QE11IF	PSEMIF	—	—	—	—	—	—	M12C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	CTMUIF	—	—	—	—	—	—	C1TXIF	—	—	CRCIF	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDITF	PTGSTEIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMIE	M12C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	QE11IE	PSEMIE	—	—	—	—	—	—	M12C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	—	C1TXIE	—	—	CRCIE	U2EIE	U1EIE	—	0000
IEC5	082A	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IE	0000
IEC7	082E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDITIE	PTGSTIEIE	—	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	M12C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	C1IP<2:0>			—	C1RXIP<2:0>			—	SPI2IP<2:0>			—	SPI2EIP<2:0>			4444
IPC9	0852	—	—	—	—	—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			0444
IPC12	0858	—	—	—	—	—	M12C2IP<2:0>			—	SI2C2IP<2:0>			—	—	—	—	0440
IPC14	085C	—	—	—	—	—	QE11IP<2:0>			—	PSEMIP<2:0>			—	—	—	—	0440
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC17	0862	—	—	—	—	—	C1TXIP<2:0>			—	—	—	—	—	—	—	—	0400
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP<2:0>			—	—	—	—	0040

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**EXAMPLE 4-3: PAGED DATA MEMORY SPACE**

**REGISTER 8-9: DSADRH: DMA MOST RECENT RAM HIGH ADDRESS REGISTER**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<23:16>							
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **DSADR<23:16>:** Most Recent DMA Address Accessed by DMA bits

**REGISTER 8-10: DSADRL: DMA MOST RECENT RAM LOW ADDRESS REGISTER**

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<7:0>							
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **DSADR<15:0>:** Most Recent DMA Address Accessed by DMA bits

**REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	PPST3	PPST2	PPST1	PPST0
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-4      **Unimplemented:** Read as '0'bit 3      **PPST3:** DMA Channel 3 Ping-Pong Mode Status Flag bit

1 = DMASTB3 register is selected

0 = DMASTA3 register is selected

bit 2      **PPST2:** DMA Channel 2 Ping-Pong Mode Status Flag bit

1 = DMASTB2 register is selected

0 = DMASTA2 register is selected

bit 1      **PPST1:** DMA Channel 1 Ping-Pong Mode Status Flag bit

1 = DMASTB1 register is selected

0 = DMASTA1 register is selected

bit 0      **PPST0:** DMA Channel 0 Ping-Pong Mode Status Flag bit

1 = DMASTB0 register is selected

0 = DMASTA0 register is selected

**REGISTER 11-8: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14**  
**(dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	QEB1R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	QEA1R<6:0>						
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **QEB1R<6:0>:** Assign B (QEB) to the Corresponding RPN Pin bits  
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **QEA1R<6:0>:** Assign A (QEA) to the Corresponding RPN Pin bits  
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

**REGISTER 11-22: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP43R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP42R<5:0>					
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-14      **Unimplemented:** Read as '0'  
bit 13-8      **RP43R<5:0>:** Peripheral Output Function is Assigned to RP43 Output Pin bits  
(see Table 11-3 for peripheral function numbers)  
bit 7-6      **Unimplemented:** Read as '0'  
bit 5-0      **RP42R<5:0>:** Peripheral Output Function is Assigned to RP42 Output Pin bits  
(see Table 11-3 for peripheral function numbers)

**REGISTER 11-23: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP55R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP54R<5:0>					
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-14      **Unimplemented:** Read as '0'  
bit 13-8      **RP55R<5:0>:** Peripheral Output Function is Assigned to RP55 Output Pin bits  
(see Table 11-3 for peripheral function numbers)  
bit 7-6      **Unimplemented:** Read as '0'  
bit 5-0      **RP54R<5:0>:** Peripheral Output Function is Assigned to RP54 Output Pin bits  
(see Table 11-3 for peripheral function numbers)

**REGISTER 16-12: TRGCONx: PWMx TRIGGER CONTROL REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
TRGDIV<3:0>				—	—	—	—
bit 15				bit 8			

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TRGSTRT<5:0> <sup>(1)</sup>					
bit 7		bit 0					

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **TRGDIV<3:0>**: Trigger # Output Divider bits

1111 = Trigger output for every 16th trigger event  
 1110 = Trigger output for every 15th trigger event  
 1101 = Trigger output for every 14th trigger event  
 1100 = Trigger output for every 13th trigger event  
 1011 = Trigger output for every 12th trigger event  
 1010 = Trigger output for every 11th trigger event  
 1001 = Trigger output for every 10th trigger event  
 1000 = Trigger output for every 9th trigger event  
 0111 = Trigger output for every 8th trigger event  
 0110 = Trigger output for every 7th trigger event  
 0101 = Trigger output for every 6th trigger event  
 0100 = Trigger output for every 5th trigger event  
 0011 = Trigger output for every 4th trigger event  
 0010 = Trigger output for every 3rd trigger event  
 0001 = Trigger output for every 2nd trigger event  
 0000 = Trigger output for every trigger event

bit 11-6 **Unimplemented**: Read as '0'

bit 5-0 **TRGSTRT<5:0>**: Trigger Postscaler Start Enable Select bits<sup>(1)</sup>

111111 = Waits 63 PWM cycles before generating the first trigger event after the module is enabled  
 •  
 •  
 •  
 000010 = Waits 2 PWM cycles before generating the first trigger event after the module is enabled  
 000001 = Waits 1 PWM cycle before generating the first trigger event after the module is enabled  
 000000 = Waits 0 PWM cycles before generating the first trigger event after the module is enabled

**Note 1:** The secondary PWM generator cannot generate PWMx trigger interrupts.

**REGISTER 16-13: IOCONx: PWMx I/O CONTROL REGISTER<sup>(2)</sup>**

R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PENH	PENL	POLH	POLL	PMOD1 <sup>(1)</sup>	PMOD0 <sup>(1)</sup>	OVRENH	OVRENL
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC
bit 7						bit 0	

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15            **PENH:** PWMxH Output Pin Ownership bit  
1 = PWMx module controls PWMxH pin  
0 = GPIO module controls PWMxH pin
- bit 14            **PENL:** PWMxL Output Pin Ownership bit  
1 = PWMx module controls PWMxL pin  
0 = GPIO module controls PWMxL pin
- bit 13            **POLH:** PWMxH Output Pin Polarity bit  
1 = PWMxH pin is active-low  
0 = PWMxH pin is active-high
- bit 12            **POLL:** PWMxL Output Pin Polarity bit  
1 = PWMxL pin is active-low  
0 = PWMxL pin is active-high
- bit 11-10        **PMOD<1:0>:** PWMx # I/O Pin Mode bits<sup>(1)</sup>  
11 = Reserved; do not use  
10 = PWMx I/O pin pair is in the Push-Pull Output mode  
01 = PWMx I/O pin pair is in the Redundant Output mode  
00 = PWMx I/O pin pair is in the Complementary Output mode
- bit 9            **OVRENH:** Override Enable for PWMxH Pin bit  
1 = OVRDAT<1> controls output on PWMxH pin  
0 = PWMx generator controls PWMxH pin
- bit 8            **OVRENL:** Override Enable for PWMxL Pin bit  
1 = OVRDAT<0> controls output on PWMxL pin  
0 = PWMx generator controls PWMxL pin
- bit 7-6          **OVRDAT<1:0>:** Data for PWMxH, PWMxL Pins if Override is Enabled bits  
If OVRRENH = 1, PWMxH is driven to the state specified by OVRDAT<1>.  
If OVRRENL = 1, PWMxL is driven to the state specified by OVRDAT<0>.
- bit 5-4          **FLTDAT<1:0>:** Data for PWMxH and PWMxL Pins if FLTMOD is Enabled bits  
If Fault is active, PWMxH is driven to the state specified by FLTDAT<1>.  
If Fault is active, PWMxL is driven to the state specified by FLTDAT<0>.
- bit 3-2          **CLDAT<1:0>:** Data for PWMxH and PWMxL Pins if CLMOD is Enabled bits  
If current-limit is active, PWMxH is driven to the state specified by CLDAT<1>.  
If current-limit is active, PWMxL is driven to the state specified by CLDAT<0>.

- Note 1:** These bits should not be changed after the PWMx module is enabled (PTEN = 1).  
**Note 2:** If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

**REGISTER 16-17: LEBDLYx: PWMx LEADING-EDGE BLANKING DELAY REGISTER**

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	LEB<11:8>			
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LEB<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12      **Unimplemented:** Read as '0'

bit 11-0      **LEB<11:0>:** Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits

**REGISTER 17-3: QE1STAT: QE1 STATUS REGISTER**

U-0	U-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0
—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN
bit 15						bit 8	

HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0
PCIIRQ <sup>(1)</sup>	PCIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN
bit 7						bit 0	

<b>Legend:</b>	HS = Hardware Settable bit	C = Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **PCHEQIRQ:** Position Counter Greater Than or Equal Compare Status bit  
 1 = POS1CNT ≥ QE1GEC  
 0 = POS1CNT < QE1GEC
- bit 12 **PCHEQIEN:** Position Counter Greater Than or Equal Compare Interrupt Enable bit  
 1 = Interrupt is enabled  
 0 = Interrupt is disabled
- bit 11 **PCLEQIRQ:** Position Counter Less Than or Equal Compare Status bit  
 1 = POS1CNT ≤ QE1LEC  
 0 = POS1CNT > QE1LEC
- bit 10 **PCLEQIEN:** Position Counter Less Than or Equal Compare Interrupt Enable bit  
 1 = Interrupt is enabled  
 0 = Interrupt is disabled
- bit 9 **POSOVIRQ:** Position Counter Overflow Status bit  
 1 = Overflow has occurred  
 0 = No overflow has occurred
- bit 8 **POSOVIEN:** Position Counter Overflow Interrupt Enable bit  
 1 = Interrupt is enabled  
 0 = Interrupt is disabled
- bit 7 **PCIIRQ:** Position Counter (Homing) Initialization Process Complete Status bit<sup>(1)</sup>  
 1 = POS1CNT was reinitialized  
 0 = POS1CNT was not reinitialized
- bit 6 **PCIEN:** Position Counter (Homing) Initialization Process Complete interrupt Enable bit  
 1 = Interrupt is enabled  
 0 = Interrupt is disabled
- bit 5 **VELOVIRQ:** Velocity Counter Overflow Status bit  
 1 = Overflow has occurred  
 0 = No overflow has not occurred
- bit 4 **VELOVIEN:** Velocity Counter Overflow Interrupt Enable bit  
 1 = Interrupt is enabled  
 0 = Interrupt is disabled
- bit 3 **HOMIRQ:** Status Flag for Home Event Status bit  
 1 = Home event has occurred  
 0 = No Home event has occurred

**Note 1:** This status bit is only applicable to PIMOD<2:0> modes, '011' and '100'.

**REGISTER 17-17: INT1TMRH: INTERVAL 1 TIMER HIGH WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTTMR<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTTMR<23:16>							
bit 7				bit 0			

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-0                      **INTTMR<31:16>**: High Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

**REGISTER 17-18: INT1TMRL: INTERVAL 1 TIMER LOW WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTTMR<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTTMR<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-0                      **INTTMR<15:0>**: Low Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

## 20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**UART**” (DS70582) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices contains two UART modules.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the UxCTS and UxRTS pins, and also includes an IrDA® encoder and decoder.

**Note:** Hardware flow control using  $\overline{\text{UxRTS}}$  and  $\overline{\text{UxCTS}}$  is not available on all pin count devices. See the “**Pin Diagrams**” section for availability.

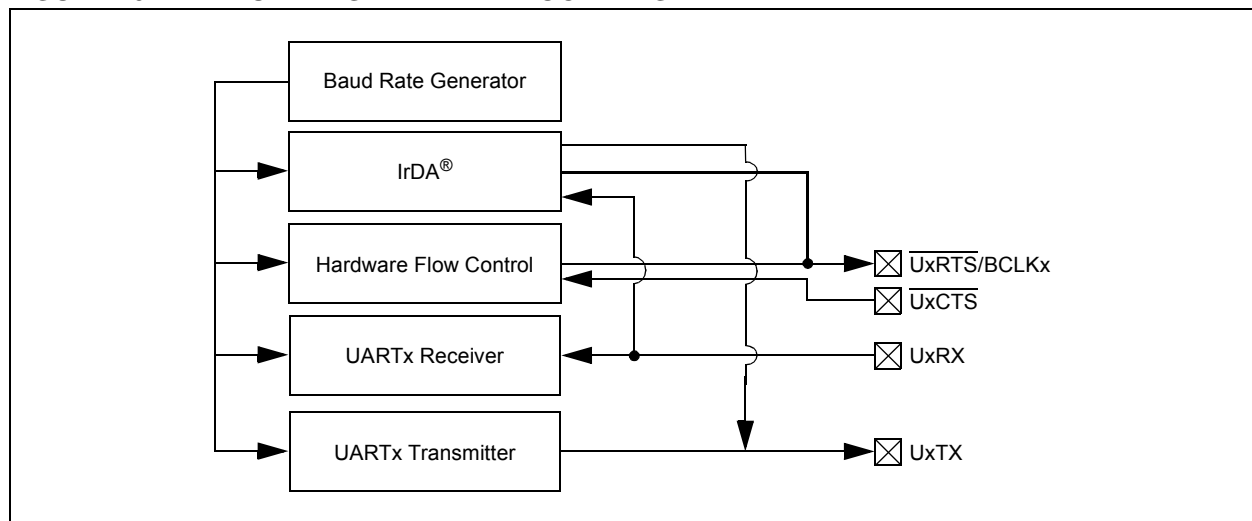
The primary features of the UARTx module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with  $\overline{\text{UxCTS}}$  and  $\overline{\text{UxRTS}}$  Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 4.375 Mbps to 67 bps at 16x mode at 70 MIPS
- Baud Rates Ranging from 17.5 Mbps to 267 bps at 4x mode at 70 MIPS
- 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- Transmit and Receive Interrupts
- A Separate Interrupt for all UARTx Error Conditions
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Support for Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UARTx module is shown in Figure 20-1. The UARTx module consists of these key hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

**FIGURE 20-1: UARTx SIMPLIFIED BLOCK DIAGRAM**



**REGISTER 21-22: CxRXFUL1: ECANx RECEIVE BUFFER FULL REGISTER 1**

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0
bit 7							bit 0

<b>Legend:</b>	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0      **RXFUL<15:0>:** Receive Buffer n Full bits  
                  1 = Buffer is full (set by module)  
                  0 = Buffer is empty (cleared by user software)

**REGISTER 21-23: CxRXFUL2: ECANx RECEIVE BUFFER FULL REGISTER 2**

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16
bit 7							bit 0

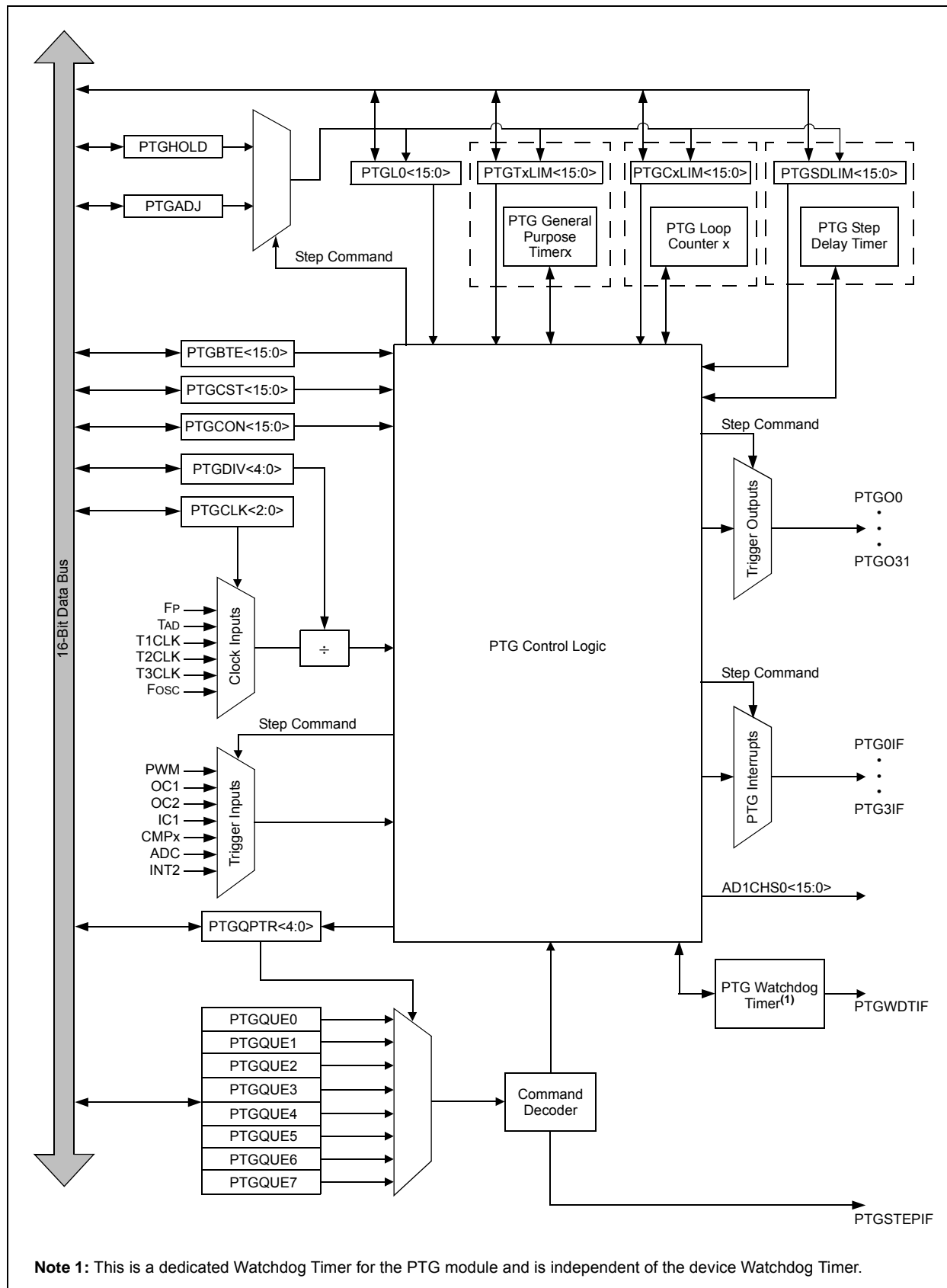
<b>Legend:</b>	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0      **RXFUL<31:16>:** Receive Buffer n Full bits  
                  1 = Buffer is full (set by module)  
                  0 = Buffer is empty (cleared by user software)

**REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2 (CONTINUED)**

- bit 1      **BUFM:** Buffer Fill Mode Select bit  
1 = Starts the buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on next interrupt  
0 = Always starts filling the buffer from the start address.
- bit 0      **ALTS:** Alternate Input Sample Mode Select bit  
1 = Uses channel input selects for Sample MUXA on first sample and Sample MUXB on next sample  
0 = Always uses channel input selects for Sample MUXA

FIGURE 24-1: PTG BLOCK DIAGRAM



**REGISTER 24-4: PTGT0LIM: PTG TIMER0 LIMIT REGISTER<sup>(1)</sup>**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT0LIM<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT0LIM<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PTGT0LIM<15:0>**: PTG Timer0 Limit Register bits  
General Purpose Timer0 Limit register (effective only with a PTGT0 Step command).

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**REGISTER 24-5: PTGT1LIM: PTG TIMER1 LIMIT REGISTER<sup>(1)</sup>**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PTGT1LIM<15:0>**: PTG Timer1 Limit Register bits  
General Purpose Timer1 Limit register (effective only with a PTGT1 Step command).

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

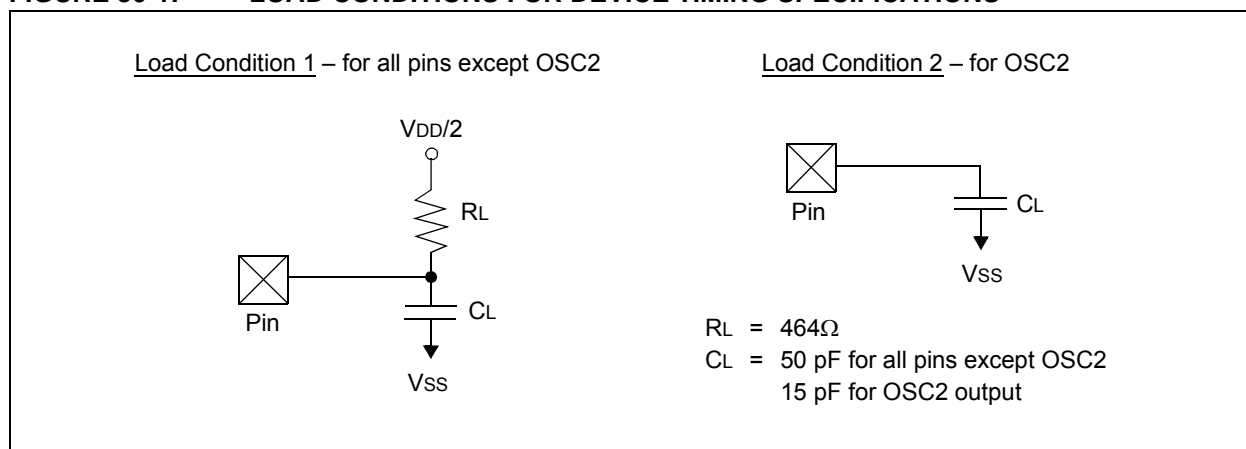
## 30.2 AC Characteristics and Timing Parameters

This section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X AC characteristics and timing parameters.

**TABLE 30-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC**

<b>AC CHARACTERISTICS</b>	<b>Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)</b>
	Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended Operating voltage $V_{DD}$ range as described in <b>Section 30.1 “DC Characteristics”</b> .

**FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**

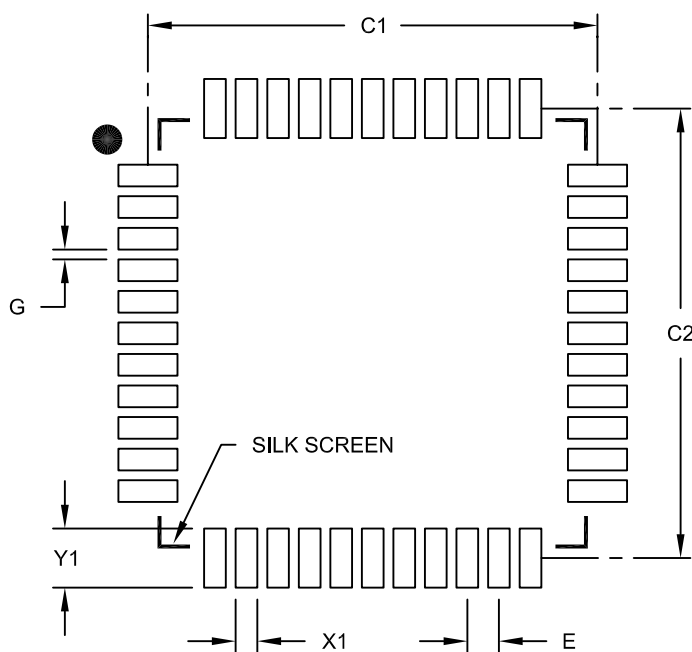


**TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS**

Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO50	Cosco	OSC2 Pin	—	—	15	pF	In XT and HS modes, when external clock is used to drive OSC1
DO56	Cio	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I <sup>2</sup> C™ mode

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B