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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24К х 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512mc506t-i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams (Continued)



Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the dsPIC33EP64MC506 product page of the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

> In addition to parameters, features and other documentation, the resulting page provides links to the related family reference manual sections.

- "Introduction" (DS70573)
- "CPU" (DS70359)
- "Data Memory" (DS70595)
- "Program Memory" (DS70613)
- "Flash Programming" (DS70609)
- "Interrupts" (DS70600)
- "Oscillator" (DS70580)
- "Reset" (DS70602)
- "Watchdog Timer and Power-Saving Modes" (DS70615)
- "I/O Ports" (DS70598)
- "Timers" (DS70362)
- "Input Capture" (DS70352)
- "Output Compare" (DS70358)
- "High-Speed PWM" (DS70645)
- "Quadrature Encoder Interface (QEI)" (DS70601)
- "Analog-to-Digital Converter (ADC)" (DS70621)
- "UART" (DS70582)
- "Serial Peripheral Interface (SPI)" (DS70569)
- "Inter-Integrated Circuit (I²C[™])" (DS70330)
- "Enhanced Controller Area Network (ECAN™)" (DS70353)
- "Direct Memory Access (DMA)" (DS70348)
- "CodeGuard™ Security" (DS70634)
- "Programming and Diagnostics" (DS70608)
- "Op Amp/Comparator" (DS70357)
- "Programmable Cyclic Redundancy Check (CRC)" (DS70346)
- "Device Configuration" (DS70618)
- "Peripheral Trigger Generator (PTG)" (DS70669)
- "Charge Time Measurement Unit (CTMU)" (DS70661)

3.7 CPU Control Registers

R/W-0) R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
0A ⁽¹⁾	OB ⁽¹⁾	SA ^(1,4)	SB ^(1,4)	OAB ⁽¹⁾	SAB ⁽¹⁾	DA ⁽¹⁾	DC
bit 15							bit 8
R/W-0 ⁽²	R/W-0 ^(2,3)	R/W-0 ^(2,3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2	IPL1	IPL0	RA	N	OV	Z	С
bit 7							bit 0
Legend:		C = Clearable	bit				
R = Reada	able bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value	e at POR	'1'= Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	OA: Accumu	lator A Overflow	v Status bit ⁽¹⁾				
	1 = Accumula	ator A has over	flowed				
	0 = Accumula	ator A has not c	verflowed				
bit 14	OB: Accumu	lator B Overflov	v Status bit ⁽¹⁾				
	1 = Accumula	ator B has over	flowed				
hit 13		lator A Saturatio	n 'Sticky' Sta	tue hit(1,4)			
DIL 15	$1 = \Delta c cumula$	ator A is saturat	ed or has her	n saturated at	some time		
	0 = Accumula	ator A is not sat	urated		Some time		
bit 12	SB: Accumu	lator B Saturatio	on 'Sticky' Sta	tus bit ^(1,4)			
	1 = Accumula	ator B is satura	ed or has bee	en saturated at	some time		
	0 = Accumula	ator B is not sat	urated				
bit 11	OAB: OA (OB Combined A	ccumulator O	verflow Status	bit ⁽¹⁾		
	1 = Accumula	ators A or B have	ve overflowed				
	0 = Neither A	Accumulators A	or B have ove	erflowed	(1)		
bit 10	SAB: SA S	B Combined A	cumulator 'Si	icky Status bit		1	
	1 = Accumula 0 = Neither A	ators A or B are	or B are satur	nave been sat	urated at some	time	
hit 9		Active hit(1)		alou			
bit 0	1 = DO loop is	s in progress					
	0 = DO loop is	s not in progres	S				
bit 8	DC: MCU AL	U Half Carry/Bo	orrow bit				
	1 = A carry-o	out from the 4th	low-order bit (for byte-sized o	data) or 8th low-	order bit (for wo	ord-sized data)
	of the re	sult occurred					
	0 = No carry	-out from the 4	th low-order t	bit (for byte-siz	ed data) or 8th	low-order bit (1	for word-sized
	uala) U						
Note 1:	This bit is availabl	e on dsPIC33E	PXXXMC20X	/50X and dsPl	C33EPXXXGP	50X devices on	ly.
2:	The IPL<2:0> bits	are concatenat	ed with the IF	PL<3> bit (COR	RCON<3>) to fo	rm the CPU Inte	errupt Priority
	Level. The value I IPL< $3 > = 1$.	n parentheses i	naicates the I	PL, IT IPL<3> =	= ⊥. User interru	ipts are disable	a wnen

REGISTER 3-1: SR: CPU STATUS REGISTER

- 3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- **4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP/MC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Program Memory" (DS70613) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

4.1 Program Address Space

The program address memory space of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in Section 4.8 "Interfacing Program and Data Memory Spaces".

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to read Device ID sections of the configuration memory space.

The program memory maps, which are presented by device family and memory size, are shown in Figure 4-1 through Figure 4-5.

FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X AND PIC24EP32GP/MC20X DEVICES



4.2.5 X AND Y DATA SPACES

The dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X core has two Data Spaces, X and Y. These Data Spaces can be considered either separate (for some DSP instructions) or as one unified linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X Data Space is used by all instructions and supports all addressing modes. X Data Space has separate read and write data buses. The X read data bus is the read data path for all instructions that view Data Space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y Data Space is used in concert with the X Data Space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY. N and MSC) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X Data Space. Modulo Addressing and Bit-Reversed Addressing are not present in PIC24EPXXXGP/MC20X devices.

All data memory writes, including in DSP instructions, view Data Space as combined X and Y address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

4.3 Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

4.3.1 KEY RESOURCES

- "Program Memory" (DS70613) in the "dsPIC33/ PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

4.4.1 PAGED MEMORY SCHEME

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre-modified and post-modified Effective Addresses (EA). The upper half of the base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Read Page register (DSRPAG) or the 9-bit Write Page register (DSWPAG), to form an Extended Data Space (EDS) address or Program Space Visibility (PSV) address. The Data Space Page registers are located in the SFR space.

Construction of the EDS address is shown in Example 4-1. When DSRPAG<9> = 0 and the base address bit, EA<15> = 1, the DSRPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit EDS read address. Similarly, when base address bit, EA<15> = 1, DSWPAG<8:0> are concatenated onto EA<14:0> to form the 24-bit EDS write address.





4.8 Interfacing Program and Data Memory Spaces

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X architecture uses a 24-bit-wide Program Space (PS) and a 16-bit-wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the architecture of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices provides two methods by which Program Space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the Program Space
- Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

TABLE 4-65: PROGRAM SPACE ADDRESS CONSTRUCTION

	Access	Program Space Address						
Access Type	Space	<23>	<22:16>	<15>	<14:1>	<0>		
Instruction Access	User	0	0 PC<22:1>					
(Code Execution)		0xx xxxx xxxx xxxx xxxx xxx0						
TBLRD/TBLWT	User	TBLPAG<7:0> Data EA<15:0>						
(Byte/Word Read/Write)		0	xxx xxxx	xxxx xxx	x xxxx xxxx			
	Configuration	TB	LPAG<7:0>		Data EA<15:0>			
		1	XXX XXXX	XXXX XX	xx xxxx xxxx			

FIGURE 4-22: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR ⁽¹⁾	OVBERR ⁽¹⁾	COVAERR ⁽¹⁾	COVBERR ⁽¹⁾	OVATE ⁽¹⁾	OVBTE ⁽¹⁾	COVTE ⁽¹⁾
bit 15							bit 8
r							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR ⁽¹) DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0
[
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpleme	ented bit, read a	as '0'	
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is clear	red	x = Bit is unk	nown
bit 15	NSTDIS: Inte	errupt Nesting	Disable bit				
	\perp = Interrupt	nesting is disa	ibled				
bit 14	OVAFRR: A	ccumulator A (Overflow Trap F	lag bit(1)			
2	1 = Trap was	s caused by ov	erflow of Accur	nulator A			
	0 = Trap was	s not caused b	y overflow of A	ccumulator A			
bit 13	OVBERR: A	ccumulator B (Overflow Trap F	lag bit ⁽¹⁾			
	1 = Trap was	s caused by ow	erflow of Accur	nulator B			
	0 = Irap was	s not caused b	y overflow of A	ccumulator B	(1)		
bit 12	COVAERR:	Accumulator A	Catastrophic (Jverflow Trap FI	ag bit("		
	1 = Trap was 0 = Trap was	s not caused by ca	v catastrophic over	overflow of Accu	mulator A		
bit 11	COVBERR:	Accumulator E	Catastrophic (Overflow Trap Fl	ag bit ⁽¹⁾		
	1 = Trap was	s caused by ca	tastrophic over	flow of Accumul	ator B		
	0 = Trap was	s not caused b	y catastrophic o	overflow of Accu	mulator B		
bit 10	OVATE: Acc	umulator A Ov	erflow Trap En	able bit ⁽¹⁾			
	1 = Trap ove	rflow of Accun	nulator A				
hit 0			orflow Tran En	able bit(1)			
DIL 9	1 = Tran ove	rflow of Accun	nulator B				
	0 = Trap is d	isabled					
bit 8	COVTE: Cat	astrophic Ove	rflow Trap Enat	ole bit ⁽¹⁾			
	1 = Trap on o	catastrophic ov	erflow of Accu	mulator A or B is	s enabled		
	0 = Trap is d	isabled					
bit 7	SFTACERR:	Shift Accumu	lator Error Statu	us bit ⁽¹⁾			
	1 = Math erro	or trap was ca or trap was po	used by an inva t caused by an	alid accumulator	shift ator shift		
bit 6		ivide-hv-Zero	Error Status bit				
bit o	1 = Math erro	or trap was ca	used by a divide	e-bv-zero			
	0 = Math erro	or trap was no	t caused by a d	ivide-by-zero			
bit 5	DMACERR:	DMAC Trap F	lag bit				
	1 = DMAC tr	ap has occurre	ed				
	0 = DMAC tr	ap has not occ	curred				
Note 1: The	ese bits are ava	ailable on dsPl	C33EPXXXMC	20X/50X and de	PIC33EPXXX	GP50X devices	s only.

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

9.3 Oscillator Control Registers

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER⁽¹⁾

11-0	R-0	R-0	R-0	U-O	R/W-v	R/W-v	R/W-v
	COSC2	COSC1	COSCO	_	NOSC2 ⁽²⁾	NOSC1 ⁽²⁾	NOSCO ⁽²⁾
bit 15							bit 8
R/W-0	R/W-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
CLKLOC	CK IOLOCK	LOCK		CF ⁽³⁾		—	OSWEN
bit 7							bit 0
			(
Legend:	- h l - h :4	y = Value set	from Configur	ation bits on P	'OR	(0)	
		vv = vvritable	DIL	0 = 0	mented bit, read	as u	
-n = value	alpor	I = BILIS Set		0 = BIUS CIE	ared		IOWN
bit 15	Unimplemen	ted: Read as '	0'				
bit 14-12	COSC<2:0>:	Current Oscilla	ator Selection	bits (read-only	')		
	111 = Fast R(C Oscillator (F	RC) with Divid	le-by-n	,		
	110 = Fast R	C Oscillator (F	RC) with Divid	le-by-16			
	101 = Low-Po	ower RC Oscill	ator (LPRC)				
	011 = Primary	v Oscillator (X	r, HS, EC) wit	h PLL			
	010 = Primary	y Oscillator (X	ſ, HS, EC)				
	001 = Fast R 000 = Fast R	C Oscillator (F C Oscillator (F	RC) with Divid RC)	le-by-N and PL	L (FRCPLL)		
bit 11	Unimplemen	ted: Read as '	0'				
bit 10-8	NOSC<2:0>:	New Oscillator	Selection bits	_S (2)			
	111 = Fast R	C Oscillator (F	RC) with Divid	le-by-n			
	110 = Fast R	C Oscillator (F	RC) with Divic	le-by-16			
	101 - Low-PC 100 = Reserv	ed					
	011 = Primary	y Oscillator (X	r, HS, EC) wit	h PLL			
	010 = Primary	y Oscillator (X	r, HS, EC)				
	001 = Fast R0 000 = Fast R0	C Oscillator (FI	RC) with Divid RC)	Ie-by-N and PL	L (FRCPLL)		
bit 7	CLKLOCK: C	lock Lock Ena	ble bit				
	1 = If (FCKS	M0 = 1), then c	lock and PLL	configurations	are locked; if (F	CKSM0 = 0), t	hen clock and
	0 = Clock and	d PLL selection	ns are not lock	ked, configurat	ions may be mo	dified	
bit 6	IOLOCK: I/O	Lock Enable b	it				
	1 = I/O lock is	active					
	0 = I/O lock is	not active	/ I I \				
bit 5	LOCK: PLL L	ock Status bit	(read-only)	ant un tincaria	a atiafia d		
	 1 = indicates 0 = Indicates 	that PLL is in	t of lock, start	-up timer is -up timer is in	progress or PLL	is disabled	
Note 1:	Writes to this regis	ter require an e erence Manual	unlock sequer " (available fro	nce. Refer to " om the Microch	Oscillator" (DS ip web site) for	70580) in the <i>"</i> o details.	dsPIC33/
2:	Direct clock switch This applies to cloc	es between an ck switches in o	y primary osci either direction	llator mode wit	h PLL and FRC ances, the appli	PLL mode are r cation must sw	not permitted. itch to FRC
	moue as a transitio	nai Clock Sour		IE IWO PLL IIIO	u c s.		

3: This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.

12.2 Timer1 Control Register

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0		
TON ⁽¹⁾	—	TSIDL	—	_	—	—	—		
bit 15							bit 8		
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0		
	TGATE	TCKPS1	TCKPS0	_	TSYNC ⁽¹⁾	TCS ⁽¹⁾	—		
bit 7							bit 0		
Legend:									
R = Readab	ole bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'			
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own		
		(1)							
bit 15	TON: Timer1	On bit ⁽¹⁾							
	1 = Starts 16-	bit Limer1 bit Timer1							
bit 1/	Unimplement	ted: Pead as '	ı'						
bit 13		1 Stop in Idle N	/ode hit						
DIC 15	1 = Discontinu	i stop in lae k	eration when a	device enters l	dle mode				
	0 = Continues	module opera	tion in Idle mo	ode					
bit 12-7	Unimplement	ted: Read as ')'						
bit 6	TGATE: Time	. TGATE: Timer1 Gated Time Accumulation Enable bit							
	When TCS =	<u>1:</u> prod							
	When TCS =	0. 0.							
	1 = Gated tim	<u>e</u> accumulatior	n is enabled						
	0 = Gated tim	e accumulatior	n is disabled						
bit 5-4	TCKPS<1:0>	: Timer1 Input	Clock Prescal	e Select bits					
	11 = 1:256								
	10 = 1:64 01 = 1:8								
	01 = 1.0 00 = 1.1								
bit 3	Unimplement	ted: Read as ')'						
bit 2	TSYNC: Time	er1 External Clo	ock Input Sync	chronization Se	elect bit ⁽¹⁾				
	When TCS =	1:							
	1 = Synchroni	izes external cl	ock input						
	0 = Does not	synchronize ex	ternal clock in	nput					
	This bit is jand	<u>ored</u> .							
bit 1	TCS: Timer1 (Clock Source S	Select bit ⁽¹⁾						
	1 = External c	lock is from pir	n, T1CK (on th	ne rising edge)					
	0 = Internal cl	ock (FP)		5 5-7					
bit 0	Unimplement	ted: Read as ')'						
Note 1: \	When Timer1 is en attempts by user so	abled in Exterr oftware to write	al Synchrono to the TMR1	us Counter mo register are ig	ode (TCS = 1, T nored.	SYNC = 1, TO	N = 1), any		

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

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R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	_	_
bit 15	1		1		1		bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	BCH(")	BCL	BPHH	BPHL	BPLH	BPLL
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	PHR: PWMxH	Rising Edge	Trigger Enabl	e bit			
	\perp = Rising edg 0 = Leading-E	ge of PyvivixH v Edge Blanking i	anores risina	edge of PWM	anking counter kH		
bit 14	PHF: PWMxH	Falling Edge	Trigger Enabl	e bit			
	1 = Falling ed	ge of PWMxH	will trigger Le	ading-Edge Bla	anking counter		
	0 = Leading-E	Edge Blanking i	gnores falling	g edge of PWM	хH		
bit 13	PLR: PWMxL	. Rising Edge T	rigger Enable	e bit oding Edgo Blo	nking countor		
	0 = Leading-E	Edge Blanking i	gnores rising	edge of PWM	kL		
bit 12	PLF: PWMxL	Falling Edge T	rigger Enable	e bit			
	1 = Falling ed	ge of PWMxL	will trigger Le	ading-Edge Bla	anking counter		
	0 = Leading-E	Edge Blanking i	gnores falling	g edge of PWM	xL		
bit 11	1 = Leading-F	-ault Input Lea Edge Blanking i	ding-Edge Bla	anking Enable	bit		
	0 = Leading-E	Edge Blanking i	s not applied	to selected Fa	ult input		
bit 10	CLLEBEN: C	urrent-Limit Le	ading-Edge E	Blanking Enable	e bit		
	1 = Leading-E	Edge Blanking i	s applied to s	selected curren	t-limit input		
hit 0.6	0 = Leading-E	tode Blanking I	s not applied	to selected cul	rrent-limit input		
bit 5	BCH Blankin	a in Selected F	J Blanking Sign	al High Enable	hit(1)		
bit 5	1 = State blan	kina (of curren	t-limit and/or	Fault input sigr	nals) when seled	ted blanking s	ianal is hiah
	0 = No blankii	ng when select	ed blanking s	signal is high	,	5	0 0
bit 4	BCL: Blanking	g in Selected B	lanking Signa	al Low Enable I	bit ⁽¹⁾		
	1 = State blan	iking (of curren	t-limit and/or	Fault input sigr	nals) when seled	cted blanking s	ignal is low
bit 3	BPHH: Blanki	ing in PWMxH	High Enable	hit			
bit o	1 = State blan	iking (of curren	t-limit and/or	Fault input sigr	nals) when PWN	/IxH output is h	igh
	0 = No blanki	ng when PWM	xH output is h	nigh			-
bit 2	BPHL: Blanki	ng in PWMxH	Low Enable b	pit			
	1 = State blan 0 = No blankii	nking (of curren ng when PWM	t-limit and/or xH output is le	Fault input sigr ow	nals) when PWN	IxH output is lo	W
bit 1	BPLH: Blanki	ng in PWMxL I	High Enable b	oit			
	1 = State blan 0 = No blankii	nking (of curren ng when PWM	t-limit and/or xL output is h	Fault input sigr igh	nals) when PWN	/IxL output is hi	igh
bit 0	BPLL: Blanki	ng in PWMxL L	ow Enable b	it			
	1 = State blan	king (of curren	t-limit and/or	Fault input sigr	nals) when PWN	IxL output is lo	W
	v = i N o diankii		x∟ output is io	JVV			

REGISTER 16-16: LEBCONX: PWMx LEADING-EDGE BLANKING CONTROL REGISTER

Note 1: The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

17.1 QEI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

17.1.1 KEY RESOURCES

- "Quadrature Encoder Interface" (DS70601) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	_	_	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0
bit 15							bit 8
U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
	ICODE6	ICODE5	ICODE4	ICODE3	ICODE2	ICODE1	ICODE0
bit 7			1	1	I	1	bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own
bit 15-13	Unimplemen	ted: Read as '	0'				
bit 12-8	FILHIT<4:0>:	Filter Hit Num	ber bits				
	10000-1111	1 = Reserved					
	01111 = Filte	r 15					
	•						
	•						
	•						
	00001 = Filte 00000 = Filte	r 1 r 0					
bit 7	Unimplemen	ted: Read as '	0'				
bit 6-0	ICODE<6:0>:	: Interrupt Flag	Code bits				
	1000101-11	11111 = Rese	rved				
	1000100 = F	IFO almost full	interrupt				
	1000011 = R 1000010 = W	ake-up interru	pt				
	1000001 = E	rror interrupt					
	1000000 = N	o interrupt					
	•						
	•						
	•						
	0010000-01	11111 = Kese B15 buffer inte	rved				
	•		nupt				
	•						
	•						
	0001001 = R	B9 buffer inter	rupt				
	0001000 = R	B8 buffer inter	rupt				
	0000111 = T	RB7 buffer inte	rrupt				
	0000110 = 1	RB5 buffer inte	errupt				
	0000100 = T	RB4 buffer inte	errupt				
	0000011 = T	RB3 buffer inte	rrupt				
	0000010 = T	RB2 buffer inte	rrupt				
	0000001 = T	RB1 buffer inte	errupt				
			πupι				

REGISTER 21-3: CxVEC: ECANx INTERRUPT CODE REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
DMABS2	DMABS1	DMABS0	—	_	_	_	—
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FSA4	FSA3	FSA2	FSA1	FSA0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	bit	U = Unimple	mented bit, read	d as '0'	
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15-13 bit 12-5 bit 4-0	ie at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown DMABS 2:0>: DMA Buffer Size bits 111 = Reserved 10 = 32 buffers in RAM 101 = 24 buffers in RAM 100 = 16 buffers in RAM 100 = 16 buffers in RAM 011 = 12 buffers in RAM 010 = 8 buffers in RAM 001 = 6 buffers in RAM 000 = 4 buffers in RAM 000 = 4 buffers in RAM 000 = 4 buffers in RAM Unimplemented: Read as '0' FSA 4:0>: FIFO Area Starts with Buffer bits 1111 = Read Buffer RB31 1110 = Read Buffer RB30 . . </td						

REGISTER 21-4: CxFCTRL: ECANx FIFO CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0		—
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15	EDG1MOD: E	Edge 1 Edge Sa	ampling Mode	Selection bit			
	1 = Edge 1 is	edge-sensitive	9				
h:+ 4 4		s level-sensitive					
DIT 14	EDG1POL: E	dge 1 Polarity	Select Dit	dao roopopoo			
	1 = Edge 1 is $0 = Edge 1$ is	s programmed f	or a positive e	edae response			
bit 13-10	EDG1SEL<3:	:0>: Edae 1 So	urce Select bits	3			
	1xxx = Rese	rved					
	01xx = Reser	rved					
	0011 = CTED)1 pin					
	00010 = CTEL	module					
	0000 = Timer	1 module					
bit 9	EDG2STAT: E	Edge 2 Status b	it				
	Indicates the	status of Edge	2 and can be v	vritten to contro	ol the edge sou	rce.	
	1 = Edge 2h	as occurred	J				
hit Q] ;+				
DILO	EDGISIAI: E	status of Edge	il 1 and can be y	written to contro	the edge sou	rce	
	1 = Edge 1 h	as occurred			i the edge sou	ice.	
	0 = Edge 1 h	as not occurred	t				
bit 7	EDG2MOD: E	Edge 2 Edge Sa	ampling Mode	Selection bit			
	1 = Edge 2 is	edge-sensitive	9				
	0 = Edge 2 is	s level-sensitive					
bit 6	EDG2POL: E	dge 2 Polarity	Select bit				
	1 = Edge 2 Is 0 = Edge 2 is	s programmed i	or a positive e	age response			
bit 5-2	EDG2SEL<3:	:0>: Edge 2 So	urce Select bits	8			
	1111 = Reser	rved		-			
	01xx = Reser	rved					
	0100 = CMP1	1 module					
	0011 = CIEL 0010 = CTFF	o∠ pin)1 pin					
	0001 = OC1	module					
	0000 = IC1 m	nodule					
bit 1-0	Unimplemen	ted: Read as ')'				

REGISTER 22-2: CTMUCON2: CTMU CONTROL REGISTER 2

24.4 Step Commands and Format

TABLE 24-1: PTG STEP COMMAND FORMAT

Step Command Byte:						
STE	Px<7:0>					
CMD<3:0>	OPTION<3:0>					
bit 7 bit	4 bit 3 bit 0					

bit 7-4	CMD<3:0>	Step Command	Command Description		
	0000	PTGCTRL	Execute control command as described by OPTION<3:0>.		
	0001	PTGADD	Add contents of PTGADJ register to target register as described by OPTION<3:0>.		
		PTGCOPY	Copy contents of PTGHOLD register to target register as described by OPTION<3:0>.		
	001x	PTGSTRB	Copy the value contained in CMD<0>:OPTION<3:0> to the CH0SA<4:0> bits (AD1CHS0<4:0>).		
	0100	PTGWHI	Wait for a low-to-high edge input from the selected PTG trigger input as described by OPTION<3:0>.		
	0101	PTGWLO	Wait for a high-to-low edge input from the selected PTG trigger input as described by OPTION<3:0>.		
	0110	Reserved	Reserved.		
	0111	PTGIRQ	Generate individual interrupt request as described by OPTION3<:0>.		
	100x	PTGTRIG	Generate individual trigger output as described by < <cmd<0>:OPTION<3:0>>.</cmd<0>		
	101x	PTGJMP	Copy the value indicated in < <cmd<0>:OPTION<3:0>> to the Queue Pointer (PTGQPTR) and jump to that Step queue.</cmd<0>		
	110x	PTGJMPC0	PTGC0 = PTGC0LIM: Increment the Queue Pointer (PTGQPTR).		
			$PTGC0 \neq PTGC0LIM$: Increment Counter 0 (PTGC0) and copy the value indicated in < <cmd<0>:OPTION<3:0>> to the Queue Pointer (PTGQPTR), and jump to that Step queue</cmd<0>		
	111x	PTGJMPC1	PTGC1 = PTGC1LIM: Increment the Queue Pointer (PTGQPTR).		
			$PTGC1 \neq PTGC1LIM$: Increment Counter 1 (PTGC1) and copy the value indicated in < <cmd<0>:OPTION<3:0>> to the Queue Pointer (PTGQPTR), and jump to that Step queue.</cmd<0>		

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 24-2 for the trigger output descriptions.

3: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER

U-0	-0 U-0 U-0 U-0 R/W-0		R/W-0	R/W-0	R/W-0	RW-0	
—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0
bit 15							bit 8

| R/W-0 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SELSRCB3 | SELSRCB2 | SELSRCB1 | SELSRCB0 | SELSRCA3 | SELSRCA2 | SELSRCA1 | SELSRCA0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 Unimplemented: Read as '0'

bit 11-8	SELSRCC<3:0>: Mask C Input Select bits
	1111 = FLT4
	1110 = FLT2
	1101 = PTGO19
	1100 = PTGO18
	1011 = Reserved
	1010 = Reserved
	1001 = Reserved
	1000 = Reserved
	0111 = Reserved
	0110 = Reserved
	0101 = PWM3H
	0100 = PWM3L
	0011 = PWM2H
	0010 = PWM2L
	0000 = PVVIVITL
· · · .	
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0111 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1000 = Reserved 1000 = Reserved 0111 = Reserved 0111 = Reserved 0110 = Reserved 0110 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3I
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1000 = Reserved 0111 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0101 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2I
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1000 = Reserved 0101 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0101 = Reserved 0111 = Reserved 0111 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H 0000 = PWM1L

AC CHARA	CTERISTICS		$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	СКЕ	СКР	SMP	
15 MHz	Table 30-33		_	0,1	0,1	0,1	
9 MHz	—	Table 30-34	—	1	0,1	1	
9 MHz	—	Table 30-35	—	0	0,1	1	
15 MHz	—	—	Table 30-36	1	0	0	
11 MHz	—	—	Table 30-37	1	1	0	
15 MHz		_	Table 30-38	0	1	0	
11 MHz	_	_	Table 30-39	0	0	0	

TABLE 30-33: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY

FIGURE 30-14: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS



DC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)(1)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial							
					-40°C ≤ TA	.≤+125°	C for Extended		
Param No. Symbol Characteristic			Min.	Тур. ⁽²⁾	Max.	Units	Conditions		
Comparator AC Characteristics									
CM10	Tresp	Response Time ⁽³⁾	_	19	_	ns	V+ input step of 100 mV, V- input held at VDD/2		
CM11	Тмс2о∨	Comparator Mode Change to Output Valid		_	10	μs			
Compa	rator DC Ch	naracteristics							
CM30	VOFFSET	Comparator Offset Voltage	—	±10	40	mV			
CM31	VHYST	Input Hysteresis Voltage ⁽³⁾	_	30	—	mV			
CM32	Trise/ Tfall	Comparator Output Rise/ Fall Time ⁽³⁾	—	20	—	ns	1 pF load capacitance on input		
CM33	Vgain	Open-Loop Voltage Gain ⁽³⁾	—	90	—	db			
CM34	VICM	Input Common-Mode Voltage	AVss	—	AVdd	V			
Op Am	p AC Chara	cteristics							
CM20	SR	Slew Rate ⁽³⁾		9		V/µs	10 pF load		
CM21a	Рм	Phase Margin (Configuration A) ^(3,4)	_	55	—	Degree	G = 100V/V; 10 pF load		
CM21b	Рм	Phase Margin (Configuration B) ^(3,5)	—	40	_	Degree	G = 100V/V; 10 pF load		
CM22	Gм	Gain Margin ⁽³⁾	—	20	—	db	G = 100V/V; 10 pF load		
CM23a	GBW	Gain Bandwidth (Configuration A) ^(3,4)	_	10	—	MHz	10 pF load		
CM23b	Gвw	Gain Bandwidth (Configuration B) ^(3,5)	—	6	_	MHz	10 pF load		

TABLE 30-53: OP AMP/COMPARATOR SPECIFICATIONS

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

- 2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
- 3: Parameter is characterized but not tested in manufacturing.
- 4: See Figure 25-6 for configuration information.
- 5: See Figure 25-7 for configuration information.
- 6: Resistances can vary by ±10% between op amps.

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions:3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$					
Param No.	Min.	Тур.	Max.	Units	Conditions			
CTMU Curr	rent Source	9						
CTMUI1	IOUT1	Base Range ⁽¹⁾	0.29	_	0.77	μA	CTMUICON<9:8> = 01	
CTMUI2	IOUT2	10x Range ⁽¹⁾	3.85	—	7.7	μA	CTMUICON<9:8> = 10	
CTMUI3	IOUT3	100x Range ⁽¹⁾	38.5	—	77	μA	CTMUICON<9:8> = 11	
CTMUI4	IOUT4	1000x Range ⁽¹⁾	385	—	770	μA	CTMUICON<9:8> = 00	
CTMUFV1 VF		Temperature Diode Forward Voltage ^(1,2)	_	0.598		V	TA = +25°C, CTMUICON<9:8> = 01	
			-	0.658		V	TA = +25°C, CTMUICON<9:8> = 10	
			-	0.721		V	TA = +25°C, CTMUICON<9:8> = 11	
CTMUFV2	VFVR	Temperature Diode Rate of	_	-1.92	_	mV/ºC	CTMUICON<9:8> = 01	
		Change ^(1,2,3)	_	-1.74	_	mV/ºC	CTMUICON<9:8> = 10	
			_	-1.56	_	mV/ºC	CTMUICON<9:8> = 11	

TABLE 30-56: CTMU CURRENT SOURCE SPECIFICATIONS

Note 1: Nominal value at center point of current trim range (CTMUICON<15:10> = 000000).

2: Parameters are characterized but not tested in manufacturing.

3: Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC configured for 10-bit mode
- ADC module configured for conversion speed of 500 ksps
- All PMDx bits are cleared (PMDx = 0)
- Executing a while(1) statement
- · Device operating from the FRC with no PLL