What is "Embedded - Microcontrollers"?
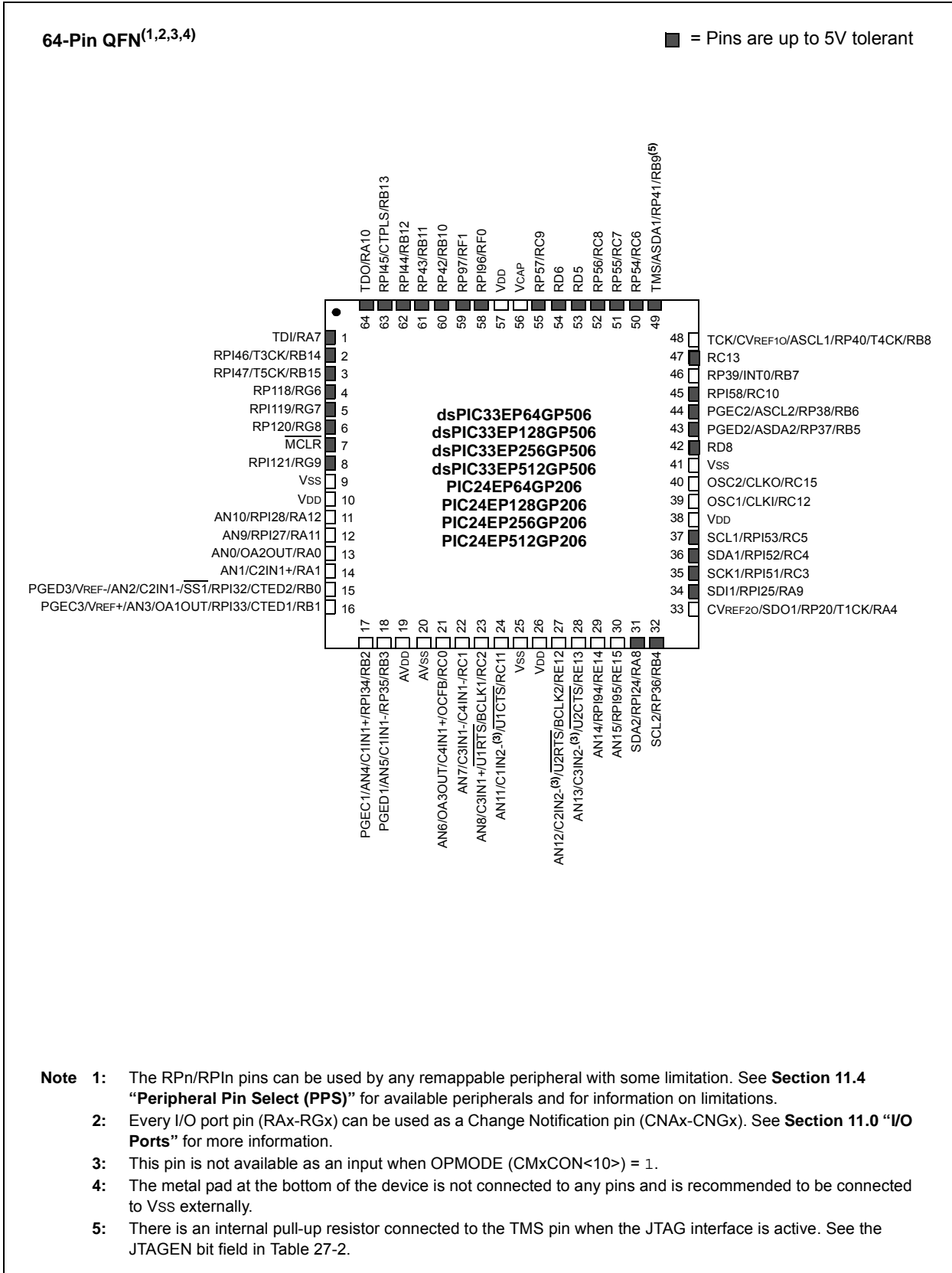
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64gp502-i-sp

Pin Diagrams (Continued)

64-Pin QFN[1,2,3,4]

■ = Pins are up to 5V tolerant

Top pins (64–49):
64 TDO/RA10
63 RPI45/CTPLS/RB13
62 RPI44/RB12
61 RP43/RB11
60 RP42/RB10
59 RP97/RF1
58 RPI96/RF0
57 VDD
56 VCAP
55 RP57/RC9
54 RD6
53 RD5
52 RP56/RC8
51 RP55/RC7
50 RP54/RC6
49 TMS/ASDA1/RP41/RB9[5]

Left pins (1–16):
1 TDI/RA7
2 RPI46/T3CK/RB14
3 RPI47/T5CK/RB15
4 RP118/RG6
5 RPI119/RG7
6 RP120/RG8
7 MCLR
8 RPI121/RG9
9 VSS
10 VDD
11 AN10/RPI28/RA12
12 AN9/RPI27/RA11
13 AN0/OA2OUT/RA0
14 AN1/C2IN1+/RA1
15 PGED3/VREF-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0
16 PGEC3/VREF+/AN3/OA1OUT/RPI33/CTED1/RB1

Device names (center):
dsPIC33EP64GP506
dsPIC33EP128GP506
dsPIC33EP256GP506
dsPIC33EP512GP506
PIC24EP64GP206
PIC24EP128GP206
PIC24EP256GP206
PIC24EP512GP206

Right pins (48–33):
48 TCK/CVREF1O/ASCL1/RP40/T4CK/RB8
47 RC13
46 RP39/INT0/RB7
45 RPI58/RC10
44 PGEC2/ASCL2/RP38/RB6
43 PGED2/ASDA2/RP37/RB5
42 RD8
41 VSS
40 OSC2/CLKO/RC15
39 OSC1/CLKI/RC12
38 VDD
37 SCL1/RPI53/RC5
36 SDA1/RPI52/RC4
35 SCK1/RPI51/RC3
34 SDI1/RPI25/RA9
33 CVREF2O/SDO1/RP20/T1CK/RA4

Bottom pins (17–32):
17 PGEC1/AN4/C1IN1+/RPI34/RB2
18 PGED1/AN5/C1IN1-/RP35/RB3
19 AVDD
20 AVSS
21 AN6/OA3OUT/C4IN1+/RC0
22 AN7/C3IN1-/C4IN1-/RC1
23 AN8/C3IN1+/U1RTS/BCLK1/RC2
24 AN11/C1IN2-/U1CTS/RC11
25 VSS
26 VDD
27 AN12/C2IN2-/U2RTS/BCLK2/RE12
28 AN13/C3IN2-/U2CTS/RE13
29 AN14/RPI94/RE14
30 AN15/RPI95/RE15
31 SDA2/RPI24/RA8
32 SCL2/RP36/RB4

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: This pin is not available as an input when OPMODE (CMxCON<10>) = 1.

4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

5: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-6).

Program memory addresses are always word-aligned on the lower word and addresses are incremented, or decremented by two, during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices reserve the addresses between 0x000000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address, 0x000000, of Flash memory, with the actual address for the start of code at address, 0x000002, of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in **Section 7.1 "Interrupt Vector Table"**.

FIGURE 4-6: PROGRAM MEMORY ORGANIZATION
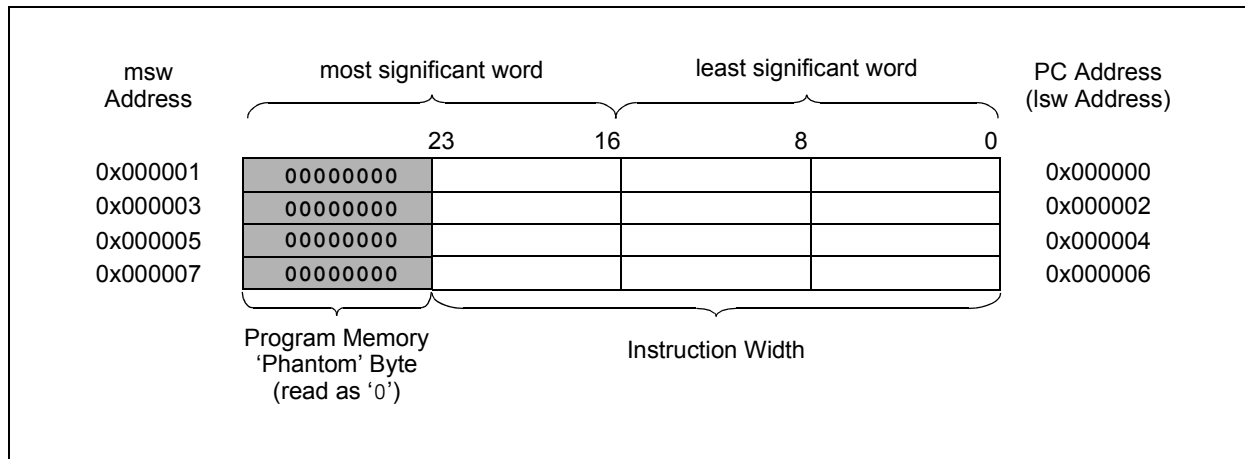
4.4 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000								W0 (WREG)									xxxx
W1	0002								W1									xxxx
W2	0004								W2									xxxx
W3	0006								W3									xxxx
W4	0008								W4									xxxx
W5	000A								W5									xxxx
W6	000C								W6									xxxx
W7	000E								W7									xxxx
W8	0010								W8									xxxx
W9	0012								W9									xxxx
W10	0014								W10									xxxx
W11	0016								W11									xxxx
W12	0018								W12									xxxx
W13	001A								W13									xxxx
W14	001C								W14									xxxx
W15	001E								W15									xxxx
SPLIM	0020								SPLIM									0000
ACCAL	0022								ACCAL									0000
ACCAH	0024								ACCAH									0000
ACCAU	0026			Sign Extension of ACCA<39>								ACCAU						0000
ACCBL	0028								ACCBL									0000
ACCBH	002A								ACCBH									0000
ACCBU	002C			Sign Extension of ACCB<39>								ACCBU						0000
PCL	002E								PCL<15:0>								—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	PCH<6:0>							0000
DSRPAG	0032	—	—	—	—	—	—	DSRPAG<9:0>										0001
DSWPAG	0034	—	—	—	—	—	—	—	DSWPAG<8:0>									0001
RCOUNT	0036								RCOUNT<15:0>									0000
DCOUNT	0038								DCOUNT<15:0>									0000
DOSTARTL	003A								DOSTARTL<15:1>								—	0000
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DOSTARTH<5:0>						0000
DOENDL	003E								DOENDL<15:1>								—	0000
DOENDH	0040	—	—	—	—	—	—	—	—	—	—	DOENDH<5:0>						0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	DMA3IF	—	—	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	QEI1IF	PSEMIF	—	—	—	—	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	CTMUIF	—	—	—	—	—	—	—	—	—	CRCIF	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	DMA3IE	—	—	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	QEI1IE	PSEMIE	—	—	—	—	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	—	—	—	—	CRCIE	U2EIE	U1EIE	—	0000
IEC5	082A	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IE	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	—	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	—	—	—	—	—	—	—	—	SPI2IP<2:0>			—	SPI2EIP<2:0>			0044
IPC9	0852	—	—	—	—	—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			0444
IPC12	0858	—	—	—	—	—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	—	—	—	0440
IPC14	085C	—	—	—	—	—	QEI1IP<2:0>			—	PSEMIP<2:0>			—	—	—	—	0440
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP<2:0>			—	—	—	—	0040
IPC23	086E	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC24	0870	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IP<2:0>			4004

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 10-3:   PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	—	—	—	—	CMPMD	—	—
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
CRCMD	—	—	—	—	—	I2C2MD	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11   **Unimplemented:** Read as '0'

bit 10   **CMPMD:** Comparator Module Disable bit
1 = Comparator module is disabled
0 = Comparator module is enabled

bit 9-8   **Unimplemented:** Read as '0'

bit 7   **CRCMD:** CRC Module Disable bit
1 = CRC module is disabled
0 = CRC module is enabled

bit 6-2   **Unimplemented:** Read as '0'

bit 1   **I2C2MD:** I2C2 Module Disable bit
1 = I2C2 module is disabled
0 = I2C2 module is enabled

bit 0   **Unimplemented:** Read as '0'

REGISTER 10-4:   PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
—	—	—	—	REFOMD	CTMUMD	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4   **Unimplemented:** Read as '0'

bit 3   **REFOMD:** Reference Clock Module Disable bit
1 = Reference clock module is disabled
0 = Reference clock module is enabled

bit 2   **CTMUMD:** CTMU Module Disable bit
1 = CTMU module is disabled
0 = CTMU module is enabled

bit 1-0   **Unimplemented:** Read as '0'

FIGURE 13-3: **TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)**

Note 1: The ADC trigger is available on the TMR3:TMR2 andTMR5:TMR4 32-bit timer pairs.
2: Timerx is a Type B timer (x = 2 and 4).
3: Timery is a Type C timer (y = 3 and 5).
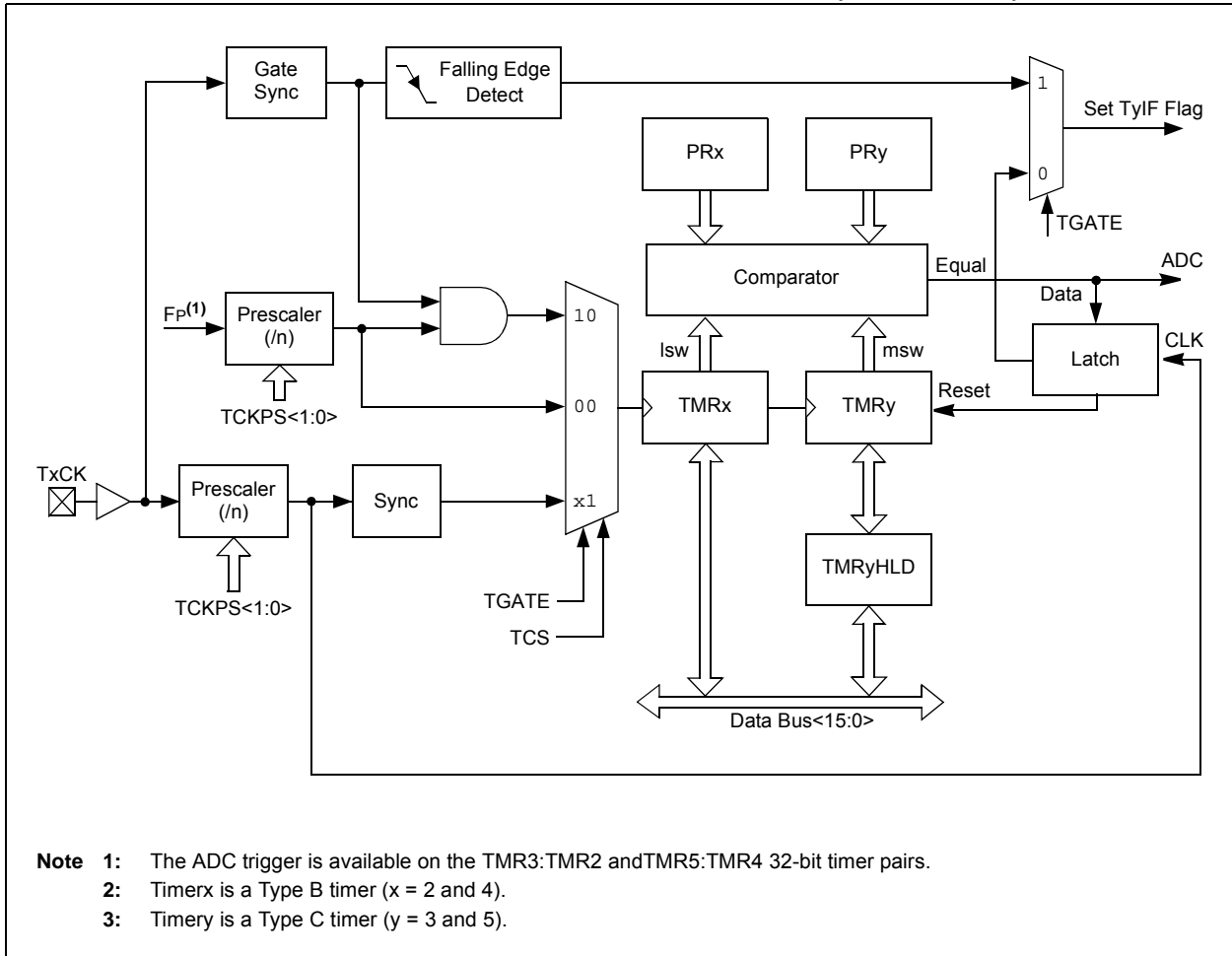
13.1 Timerx/y Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

13.1.1 KEY RESOURCES

- **"Timers"** (DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

16.2 PWM Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

> **Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

16.2.1   KEY RESOURCES

- **"High-Speed PWM"** (DS70645) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

16.3 PWMx Control Registers

REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU[1]	SYNCPOL[1]	SYNCOEN[1]
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN[1]	SYNCSRC2[1]	SYNCSRC1[1]	SYNCSRC0[1]	SEVTPS3[1]	SEVTPS2[1]	SEVTPS1[1]	SEVTPS0[1]
bit 7							bit 0

Legend:		HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PTEN:** PWMx Module Enable bit
1 = PWMx module is enabled
0 = PWMx module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **PTSIDL:** PWMx Time Base Stop in Idle Mode bit
1 = PWMx time base halts in CPU Idle mode
0 = PWMx time base runs in CPU Idle mode

bit 12 **SESTAT:** Special Event Interrupt Status bit
1 = Special event interrupt is pending
0 = Special event interrupt is not pending

bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Special event interrupt is enabled
0 = Special event interrupt is disabled

bit 10 **EIPU:** Enable Immediate Period Updates bit[1]
1 = Active Period register is updated immediately
0 = Active Period register updates occur on PWMx cycle boundaries

bit 9 **SYNCPOL:** Synchronize Input and Output Polarity bit[1]
1 = SYNCI1/SYNCO1 polarity is inverted (active-low)
0 = SYNCI1/SYNCO1 is active-high

bit 8 **SYNCOEN:** Primary Time Base Sync Enable bit[1]
1 = SYNCO1 output is enabled
0 = SYNCO1 output is disabled

bit 7 **SYNCEN:** External Time Base Synchronization Enable bit[1]
1 = External synchronization of primary time base is enabled
0 = External synchronization of primary time base is disabled

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.

2: See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for information on this selection.

REGISTER 20-2:   UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5   **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)

1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
0 = Address Detect mode is disabled

bit 4   **RIDLE:** Receiver Idle bit (read-only)

1 = Receiver is Idle
0 = Receiver is active

bit 3   **PERR:** Parity Error Status bit (read-only)

1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected

bit 2   **FERR:** Framing Error Status bit (read-only)

1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected

bit 1   **OERR:** Receive Buffer Overrun Error Status bit (clear/read-only)

1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed; clearing a previously set OERR bit ($1 \rightarrow 0$ transition) resets the receiver buffer and the UxRSR to the empty state

bit 0   **URXDA:** UARTx Receive Buffer Data Available bit (read-only)

1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

Note 1:   Refer to the **"UART"** (DS70582) section in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for transmit operation.

REGISTER 21-8: CxEC: ECANx TRANSMIT/RECEIVE ERROR COUNT REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			TERRCNT<7:0>				
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			RERRCNT<7:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **TERRCNT<7:0>:** Transmit Error Count bits

bit 7-0 **RERRCNT<7:0>:** Receive Error Count bits

REGISTER 21-9: CxCFG1: ECANx BAUD RATE CONFIGURATION REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-6 **SJW<1:0>:** Synchronization Jump Width bits

11 = Length is 4 x TQ
10 = Length is 3 x TQ
01 = Length is 2 x TQ
00 = Length is 1 x TQ

bit 5-0 **BRP<5:0>:** Baud Rate Prescaler bits

11 1111 = TQ = 2 x 64 x 1/FCAN
•
•
•
00 0010 = TQ = 2 x 3 x 1/FCAN
00 0001 = TQ = 2 x 2 x 1/FCAN
00 0000 = TQ = 2 x 1 x 1/FCAN

REGISTER 24-4: PTGT0LIM: PTG TIMER0 LIMIT REGISTER[1]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT0LIM<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT0LIM<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGT0LIM<15:0>:** PTG Timer0 Limit Register bits

General Purpose Timer0 Limit register (effective only with a `PTGT0` Step command).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = `1` and PTGSTRT = `1`).

REGISTER 24-5: PTGT1LIM: PTG TIMER1 LIMIT REGISTER[1]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGT1LIM<15:0>:** PTG Timer1 Limit Register bits

General Purpose Timer1 Limit register (effective only with a `PTGT1` Step command).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = `1` and PTGSTRT = `1`).

REGISTER 26-2: CRCCON2: CRC CONTROL REGISTER 2

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DWIDTH4	DWIDTH3	DWIDTH2	DWIDTH1	DWIDTH0
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	PLEN4	PLEN3	PLEN2	PLEN1	PLEN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **DWIDTH<4:0>:** Data Width Select bits

These bits set the width of the data word (DWIDTH<4:0> + 1).

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **PLEN<4:0>:** Polynomial Length Select bits

These bits set the length of the polynomial (Polynomial Length = PLEN<4:0> + 1).

TABLE 27-2:   CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Description
WDTPRE	Watchdog Timer Prescaler bit `1` = 1:128 `0` = 1:32
WDTPOST<3:0>	Watchdog Timer Postscaler bits `1111` = 1:32,768 `1110` = 1:16,384 • • • `0001` = 1:2 `0000` = 1:1
WDTWIN<1:0>	Watchdog Window Select bits `11` = WDT window is 25% of WDT period `10` = WDT window is 37.5% of WDT period `01` = WDT window is 50% of WDT period `00` = WDT window is 75% of WDT period
ALTI2C1	Alternate I2C1 pin `1` = I2C1 is mapped to the SDA1/SCL1 pins `0` = I2C1 is mapped to the ASDA1/ASCL1 pins
ALTI2C2	Alternate I2C2 pin `1` = I2C2 is mapped to the SDA2/SCL2 pins `0` = I2C2 is mapped to the ASDA2/ASCL2 pins
JTAGEN[2]	JTAG Enable bit `1` = JTAG is enabled `0` = JTAG is disabled
ICS<1:0>	ICD Communication Channel Select bits `11` = Communicate on PGEC1 and PGED1 `10` = Communicate on PGEC2 and PGED2 `01` = Communicate on PGEC3 and PGED3 `00` = Reserved, do not use

Note 1:   This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

2:   When JTAGEN = `1`, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = `1`. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

TABLE 28-2:   INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles[2]	Status Flags Affected
46	MOV	MOV	f,Wn	Move f to Wn	1	1	None
		MOV	f	Move f to f	1	1	None
		MOV	f,WREG	Move f to WREG	1	1	None
		MOV	#lit16,Wn	Move 16-bit literal to Wn	1	1	None
		MOV.b	#lit8,Wn	Move 8-bit literal to Wn	1	1	None
		MOV	Wn,f	Move Wn to f	1	1	None
		MOV	Wso,Wdo	Move Ws to Wd	1	1	None
		MOV	WREG,f	Move WREG to f	1	1	None
		MOV.D	Wns,Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D	Ws,Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
47	MOVPAG	MOVPAG	#lit10,DSRPAG	Move 10-bit literal to DSRPAG	1	1	None
		MOVPAG	#lit9,DSWPAG	Move 9-bit literal to DSWPAG	1	1	None
		MOVPAG	#lit8,TBLPAG	Move 8-bit literal to TBLPAG	1	1	None
		MOVPAG	Ws,DSRPAG	Move Ws<9:0> to DSRPAG	1	1	None
		MOVPAG	Ws,DSWPAG	Move Ws<8:0> to DSWPAG	1	1	None
		MOVPAG	Ws,TBLPAG	Move Ws<7:0> to TBLPAG	1	1	None
48	MOVSAC	MOVSAC	Acc,Wx,Wxd,Wy,Wyd,AWB[1]	Prefetch and store accumulator	1	1	None
49	MPY	MPY	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd[1]	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		MPY	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd[1]	Square Wm to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
50	MPY.N	MPY.N	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd[1]	-(Multiply Wm by Wn) to Accumulator	1	1	None
51	MSC	MSC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd,AWB[1]	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB, SA,SB,SAB

Note 1:   These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

     2:   Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 30-7:   DC CHARACTERISTICS: IDLE CURRENT (I$_{IDLE}$)

DC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C $\leq$ T$_A$ $\leq$ +85°C for Industrial -40°C $\leq$ T$_A$ $\leq$ +125°C for Extended		
Parameter No.	Typ.	Max.	Units	Conditions		
Idle Current (I$_{IDLE}$)[1]						
DC40d	3	8	mA	-40°C	3.3V	10 MIPS
DC40a	3	8	mA	+25°C		
DC40b	3	8	mA	+85°C		
DC40c	3	8	mA	+125°C		
DC42d	6	12	mA	-40°C	3.3V	20 MIPS
DC42a	6	12	mA	+25°C		
DC42b	6	12	mA	+85°C		
DC42c	6	12	mA	+125°C		
DC44d	11	18	mA	-40°C	3.3V	40 MIPS
DC44a	11	18	mA	+25°C		
DC44b	11	18	mA	+85°C		
DC44c	11	18	mA	+125°C		
DC45d	17	27	mA	-40°C	3.3V	60 MIPS
DC45a	17	27	mA	+25°C		
DC45b	17	27	mA	+85°C		
DC45c	17	27	mA	+125°C		
DC46d	20	35	mA	-40°C	3.3V	70 MIPS
DC46a	20	35	mA	+25°C		
DC46b	20	35	mA	+85°C		

Note 1:   Base Idle current (I$_{IDLE}$) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to V$_{SS}$
- $\overline{MCLR}$ = V$_{DD}$, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

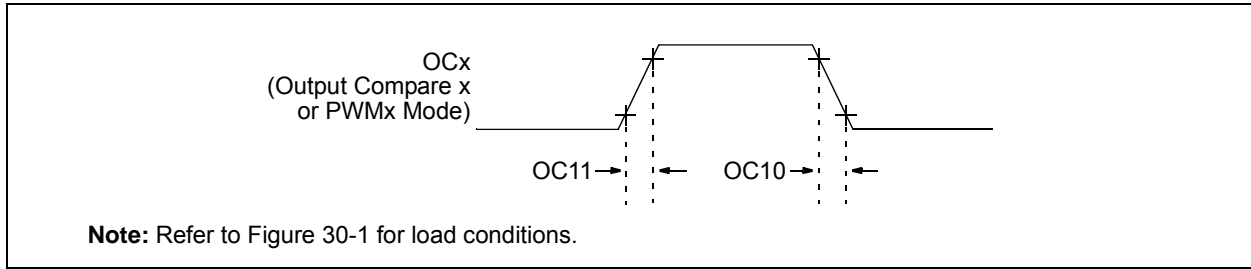**FIGURE 30-7:** **OUTPUT COMPARE x MODULE (OCx) TIMING CHARACTERISTICS**

OCx
(Output Compare x
or PWMx Mode)

OC11→ OC10→

Note: Refer to Figure 30-1 for load conditions.

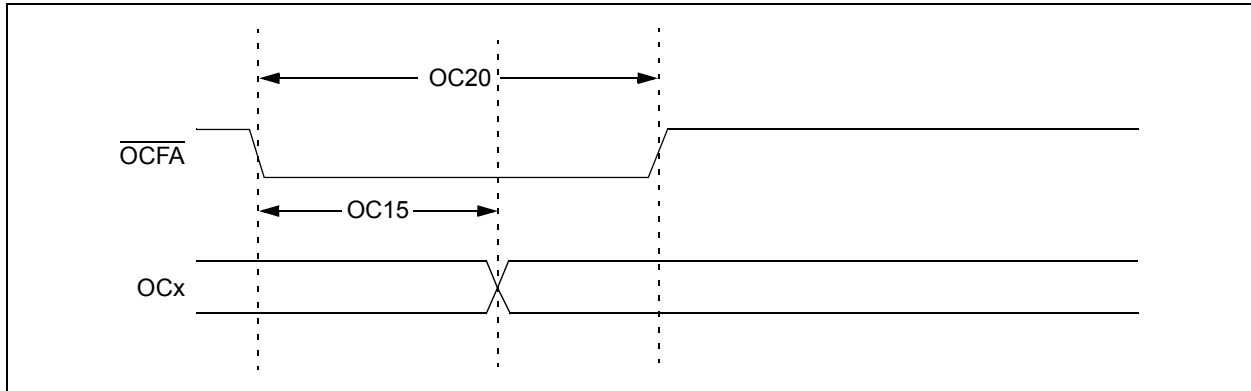**TABLE 30-27:** **OUTPUT COMPARE x MODULE TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic[1]	Min.	Typ.	Max.	Units	Conditions
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See Parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter DO31

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-8: **OCx/PWMx MODULE TIMING CHARACTERISTICS**

OCFA

OCx

OC20

OC15

TABLE 30-28: **OCx/PWMx MODE TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic[1]	Min.	Typ.	Max.	Units	Conditions
OC15	TFD	Fault Input to PWMx I/O Change	—	—	TCY + 20	ns	
OC20	TFLT	Fault Input Pulse Width	TCY + 20	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 30-38: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C $\leq$ TA $\leq$ +85°C for Industrial -40°C $\leq$ TA $\leq$ +125°C for Extended				
Param.	Symbol	Characteristic[1]	Min.	Typ.[2]	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	—	—	Lesser of FP or 11	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS2}$ ↑ to SDO2 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	$\overline{SS2}$ ↑ after SCK2 Edge	1.5 TCY + 40	—	—	ns	(Note 4)
SP60	TssL2doV	SDO2 Data Output Valid after $\overline{SS2}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

FIGURE 30-23: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1)
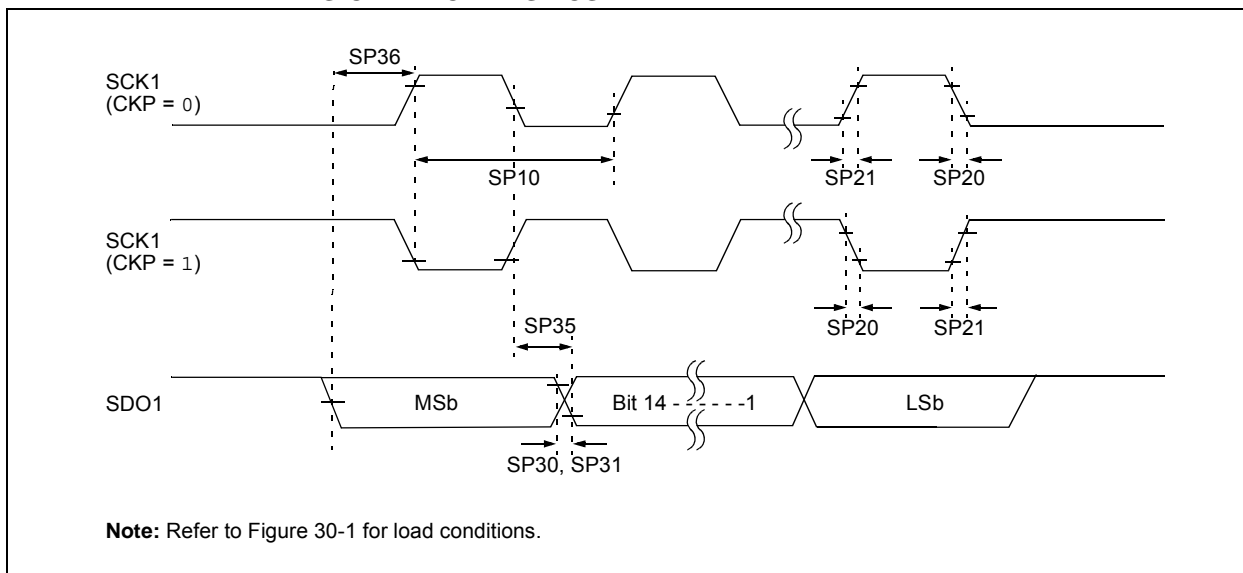TIMING CHARACTERISTICS

Note: Refer to Figure 30-1 for load conditions.

TABLE 30-42: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic[1]	Min.	Typ.[2]	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	—	—	15	MHz	(Note 3)
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdiV2scH, TdiV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.
2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.
4: Assumes 50 pF load on all SPI1 pins.

NOTES:

Revision F (November 2012)

Removed "Preliminary" from data sheet footer.

Revision G (March 2013)

This revision includes the following global changes:

- changes "$\overline{\text{FLTx}}$" pin function to "FLTx" on all occurrences
- adds **Section 31.0 "High-Temperature Electrical Characteristics"** for high-temperature (+150°C) data

This revision also includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-5.

TABLE A-5: MAJOR SECTION UPDATES

Section Name	Update Description
Cover Section	• Changes internal oscillator specification to 1.0% • Changes I/O sink/source values to 12 mA or 6 mA • Corrects 44-pin VTLA pin diagram (pin 32 now shows as 5V tolerant)
Section 4.0 "Memory Organization"	• Deletes references to Configuration Shadow registers • Corrects the spelling of the JTAGIP and PTGWDTIP bits throughout • Corrects the Reset value of all IOCON registers as C000h • Adds footnote to Table 4-42 to indicate the absence of Comparator 3 in 28-pin devices
Section 6.0 "Resets"	• Removes references to cold and warm Resets, and clarifies the initial configuration of the device clock source on all Resets
Section 7.0 "Interrupt Controller"	• Corrects the definition of GIE as "Global Interrupt Enable" (not "General")
Section 9.0 "Oscillator Configuration"	• Clarifies the behavior of the CF bit when cleared in software • Removes POR behavior footnotes from all control registers • Corrects the tuning range of the TUN<5:0> bits in Register 9-4 to an overall range ±1.5%
Section 13.0 "Timer2/3 and Timer4/5"	• Clarifies the presence of the ADC Trigger in 16-bit Timer3 and Timer5, as well as the 32-bit timers
Section 15.0 "Output Compare"	• Corrects the first trigger source for SYNCSEL<4:0> (OCxCON2<4:0>) as OCxRS match
Section 16.0 "High-Speed PWM Module"	• Clarifies the source of the PWM interrupts in Figure 16-1 • Corrects the Reset states of IOCONx<15:14> in Register 16-13 as '11'
Section 17.0 "Quadrature Encoder Interface (QEI) Module"	• Clarifies the operation of the IMV<1:0> bits (QEICON<9:8>) with updated text and additional notes • Corrects the first prescaler value for QFVDIV<2:0> (QEI1OC<13:11>), now 1:128
Section 23.0 "10-Bit/12-Bit Analog-to-Digital Converter (ADC)"	• Adds note to Figure 23-1 that Op Amp 3 is not available in 28-pin devices • Changes "sample clock" to "sample trigger" in AD1CON1 (Register 23-1) • Clarifies footnotes on op amp usage in Registers 23-5 and 23-6
Section 25.0 "Op Amp/ Comparator Module"	• Adds Note text to indicate that Comparator 3 is unavailable in 28-pin devices • Splits Figure 25-1 into two figures for clearer presentation (Figure 25-1 for Op amp/Comparators 1 through 3, Figure 25-2 for Comparator 4). Subsequent figures are renumbered accordingly. • Corrects reference description in xxxxx (now (AVDD+AVSS)/2) • Changes CMSTAT<15> in Register 25-1 to "PSIDL"
Section 27.0 "Special Features"	• Corrects the addresses of all Configuration bytes for 512 Kbyte devices