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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64gp503t-e-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5	IPL<2:0>: CPU Interrupt Priority Level Status bits ^(2,3) 111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled 110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12) 011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10) 001 = CPU Interrupt Priority Level is 1 (9) 000 = CPU Interrupt Priority Level is 0 (8)
bit 4	RA: REPEAT Loop Active bit 1 = REPEAT loop in progress 0 = REPEAT loop not in progress
bit 3	N: MCU ALU Negative bit 1 = Result was negative 0 = Result was non-negative (zero or positive)
bit 2	 OV: MCU ALU Overflow bit This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state. 1 = Overflow occurred for signed arithmetic (in this arithmetic operation) 0 = No overflow occurred
bit 1	 Z: MCU ALU Zero bit 1 = An operation that affects the Z bit has set it at some time in the past 0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)
bit 0	C: MCU ALU Carry/Borrow bit 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred
Note 1: 2:	This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only. The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority

- Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
 3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- 4: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				IC2R<6:0>			
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				IC1R<6:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit				U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	Unimplemen	ted: Read as '	0'				
bit 14-8	IC2R<6:0>: A (see Table 11	Assign Input Ca -2 for input pin	pture 2 (IC2) selection nur	to the Correspondent	onding RPn P	in bits	
	1111001 = I r	nput tied to RPI	121				
	•						
	0000001 = lr	nput tied to CM	P1				
	nl = 0000000	nput tied to Vss	;				
bit 7	Unimplemen	ted: Read as '	0'				
bit 6-0	IC1R<6:0>: A (see Table 11	Assign Input Ca -2 for input pin	pture 1 (IC1) selection nur	to the Correspondence	onding RPn P	in bits	
	1111001 = I r	nput tied to RPI	121				
	•						
	•						
	0000001 = lr	nput tied to CM	P1				
	0000000 = Ir	nput tied to Vss	;				

REGISTER 11-4: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

NOTES:

13.0 TIMER2/3 AND TIMER4/5

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70362) of the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter
- They also support these features:
- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (32-bit timer pairs, and Timer3 and Timer5 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, and T4CON, T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. T3CON and T5CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw); Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

Note: For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

Note: Only Timer2, 3, 4 and 5 can trigger a DMA data transfer.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
QCAPEN	FLTREN	QFDIV2	QFDIV1	QFDIV0	OUTFNC1	OUTFNC0	SWPAB					
bit 15					• •		bit 8					
R/W-0	R/W-0	R/W-0	R/W-0	R-x	R-x	R-x	R-x					
HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA					
bit 7							bit 0					
Legend:	a hit	\// - \//ritabla	h it	II – Unimploy	monted bit read	4 a.a. (0)						
n - Value at		vv = vvii(able	DIL	$0^{\circ} = 0$	nented bit, read	v – Ritic unkn						
		1 - Dit 13 36t			areu							
bit 15	OCAPEN: OF	-I Position Cou	nter Input Cap	ture Enable bit								
	1 = Index ma	tch event trigge	ers a position c	apture event								
	0 = Index ma	tch event does	not trigger a p	osition capture	event							
bit 14	FLTREN: QE	Ax/QEBx/INDX	x/HOMEx Digi	ital Filter Enabl	e bit							
	1 = Input pin	digital filter is e digital filter is d	nabled isabled (bypas	eed)								
hit 13_11			NDXv/HOMEv	Digital Input Fi	ilter Clock Divid	a Salact hits						
511 15-11	111 = 1:128 (clock divide		Digital Input I								
	110 = 1:64 clock divide											
	101 = 1:32 clock divide											
	100 = 1.16 cm 011 = 1:8 clo	011 = 1:8 clock divide										
	010 = 1:4 clo	010 = 1:4 clock divide										
	001 = 1:2 clock divide											
hit 10₋9			Output Functi	ion Mode Sele	rt hits							
bit 10 5	11 = The CTN	1 = The CTNCMPx in goes high when QEI11 EC > POS1CNT > QEI1GEC										
	10 = The CTM	NCMPx pin goe	s high when P	$OS1CNT \leq QE$	EIILEC							
	01 = The CTNCMPx pin goes high when POS1CNT \geq QEI1GEC											
hit 8	SWPAB: Swa	s uisabled an OEA and OE	B Inputs hit									
bit 0	1 = QEAx and	d QEBx are swa	apped prior to	quadrature de	coder logic							
	0 = QEAx and	0 = QEAx and QEBx are not swapped										
bit 7	HOMPOL: HO	OMEx Input Po	larity Select bit	t								
	1 = Input is in	iverted										
hit 6		ot inverted Vy Input Dolori	ty Soloot bit									
DILO	1 = Input is in	verted	ly Select bit									
	0 = Input is no	0 = Input is not inverted										
bit 5	QEBPOL: QE	EBx Input Polar	ity Select bit									
	1 = Input is ir	nverted										
L:1 4		ot inverted	:									
DIT 4		EAX Input Polar	ity Select bit									
	1 = 10000000000000000000000000000000000	not inverted										
bit 3	HOME: Statu	s of HOMEx In	out Pin After P	olarity Control								
	1 = Pin is at I	logic '1'		-								
	0 = Pin is at	logic '0'										

REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER

REGISTER 17-4: POSICNTH: POSITION COUNTER 1 HIGH WORD REGISTER

-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown
R = Readable bit W = Writable bit			bit	U = Unimpler	mented bit, rea	d as '0'	
Legend:							
bit 7							bit 0
			POSCN	IT<23:16>			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
bit 15							bit 8
			POSCN	IT<31:24>			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

bit 15-0 **POSCNT<31:16>:** High Word Used to Form 32-Bit Position Counter Register (POS1CNT) bits

REGISTER 17-5: POS1CNTL: POSITION COUNTER 1 LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
POSCNT<15:8>								
bit 15							bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			POSCN	NT<7:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 POSCNT<15:0>: Low Word Used to Form 32-Bit Position Counter Register (POS1CNT) bits

REGISTER 17-6: POS1HLD: POSITION COUNTER 1 HOLD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			POSH	LD<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			POSH	ILD<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'			
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			

bit 15-0 **POSHLD<15:0>:** Hold Register for Reading and Writing POS1CNTH bits

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REGISTER 17-17: INT1TMRH: INTERVAL 1 TIMER HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
INTTMR<31:24>										
bit 15 bit 8										
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
			INTTM	R<23:16>						
bit 7							bit 0			
Legend:										
R = Readable b	bit	W = Writable bi	it	U = Unimplemented bit, read as '0'						
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown						

bit 15-0 INTTMR<31:16>: High Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

REGISTER 17-18: INT1TMRL: INTERVAL 1 TIMER LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTTM	1R<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INTT	/IR<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable b	ble bit U = Unimplemented bit, read as '0'				
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			

bit 15-0 INTTMR<15:0>: Low Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

18.1 SPI Helpful Tips

- 1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
 - a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on SSx.
 - b) If FRMPOL = 0, use a pull-up resistor on $\frac{1}{SSx}$.

Note:	This	insures	that	the	first	fra	ame
	transmission a		after	initializ	ation	is	not
	shifted						

- 2. In Non-Framed 3-Wire mode, (i.e., not using SSx from a master):
 - a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on SSx.
 - b) If CKP = 0, always place a pull-down resistor on SSx.
 - **Note:** This will insure that during power-up and initialization the master/slave will not lose Sync due to an errant SCKx transition that would cause the slave to accumulate data shift errors for both transmit and receive appearing as corrupted data.
- FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the SSx pin, which indicates the start of a data frame.
 - Note: Not all third-party devices support Frame mode timing. Refer to the SPIx specifications in Section 30.0 "Electrical Characteristics" for details.
- In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPIx data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

18.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

18.2.1 KEY RESOURCES

- "Serial Peripheral Interface (SPI)" (DS70569) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

19.2 I²C Control Registers

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	_	I2CSIDL	SCLREL	IPMIEN ⁽¹⁾	A10M	DISSLW	SMEN
bit 15					•		bit 8
R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0
Legend:		HC = Hardware	Clearable bit				
R = Readable	e bit	W = Writable bit	t	U = Unimpler	mented bit, rea	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
bit 15	12CEN: 12Cx	Enable bit					
	1 = Enables t	he I2Cx module a	and configures	the SDAx and	SCLx pins as	serial port pins	;
h it 4.4			all I-C ···· pins a	are controlled	by port function	15	
DIL 14		ted: Read as 0	da hit				
DIE 13	1 - Discontinu	x Stop in Idle Mo	de bli ation whon dow	ico ontore an l	dlo modo		
	0 = Continues	s module operation	on in Idle mode		die mode		
bit 12	SCLREL: SC	Lx Release Cont	rol bit (when or	perating as I ² C	slave)		
	1 = Releases	SCLx clock		U	,		
	0 = Holds SC	Lx clock low (cloo	ck stretch)				
	$\frac{\text{If STREN} = 1}{\text{Distance}}$	<u>:</u>			· · · · · · · · · · · · · · · · · · ·		
	Bit is R/W (i.e	., software can w	rite '0' to initiate o data byte tra	e stretch and w	rite '1' to relea	se clock). Harc	dware is clear
	address byte	reception. Hardw	are is clear at	the end of eve	ry slave data b	yte reception.	l every slave
	If STREN = 0	<u>:</u>			-		
	Bit is R/S (i.e.	, software can on	ly write '1' to re	elease clock). I	Hardware is cle	ar at the begin	ning of every
	slave data by		Hardware is cle	ar at the end o	of every slave a	address byte re	eception.
bit 11	IPMIEN: Intel	ligent Peripheral	Management I	nterface (IPMI)) Enable bit		
	1 = IPMI mod 0 = IPMI mod	e is enabled, all a		Acknowledged	I		
bit 10	A10M: 10-Bit	Slave Address b	it				
	1 = I2CxADD	is a 10-bit slave	address				
	0 = I2CxADD	is a 7-bit slave a	ddress				
bit 9	DISSLW: Disa	able Slew Rate C	Control bit				
	1 = Slew rate 0 = Slew rate	control is disable control is enable	ed d				
bit 8	SMEN: SMBL	us Input Levels bi	t				
	1 = Enables I 0 = Disables \$	/O pin thresholds SMBus input thre	compliant with sholds	SMBus speci	fication		
bit 7	GCEN: Gene	ral Call Enable bi	it (when operat	ing as I ² C slav	re)		
	1 = Enables in 0 = General c	terrupt when a ge all address disab	neral call addre	ss is received ir	12CxRSR (mo	dule is enabled	for reception)

Note 1: When performing master operations, ensure that the IPMIEN bit is set to '0'.

REGISTER 20-1: UXMODE: UARTX MODE REGISTER (CONTINUED)

bit 5	ABAUD: Auto-Baud Enable bit
	 1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion 0 = Baud rate measurement is disabled or completed
bit 4	URXINV: UARTx Receive Polarity Inversion bit
	1 = UxRX Idle state is '0' 0 = UxRX Idle state is '1'
bit 3	BRGH: High Baud Rate Enable bit
	 1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode) 0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
bit 2-1	PDSEL<1:0>: Parity and Data Selection bits
	 11 = 9-bit data, no parity 10 = 8-bit data, odd parity 01 = 8-bit data, even parity 00 = 8-bit data, no parity
bit 0	STSEL: Stop Bit Selection bit
	1 = Two Stop bits 0 = One Stop bit
Note 1:	Refer to the " UART " (DS70582) section in the <i>"dsPIC33/PIC24 Family Reference Manual"</i> for information on enabling the UARTx module for receive or transmit operation.

- 2: This feature is only available for the 16x BRG mode (BRGH = 0).
- 3: This feature is only available on 44-pin and 64-pin devices.
- 4: This feature is only available on 64-pin devices.

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R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1	
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN ⁽¹⁾	UTXBF	TRMT	
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0	
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	
bit 7				-			bit 0	
Legend: HC = Hardwar		e Clearable bit	C = Clearable	e bit				
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'				

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

		0 – Onimplemented bit, rea	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15,13 UTXISEL<1:0>: UARTx Transmission Interrupt Mode Selection bits

- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 UTXINV: UARTx Transmit Polarity Inversion bit
 - If IREN = 0: 1 = UxTX Idle state is '0'
 - 0 = UxTX Idle state is '1'
 - If IREN = 1:
 - 1 = IrDA encoded, UxTX Idle state is '1'
 - 0 = IrDA encoded, UxTX Idle state is '0'
- bit 12 Unimplemented: Read as '0'
- bit 11 UTXBRK: UARTx Transmit Break bit
 - 1 = Sends Sync Break on next transmission Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
 - 0 = Sync Break transmission is disabled or completed
- **UTXEN:** UARTx Transmit Enable bit⁽¹⁾ bit 10 1 = Transmit is enabled, UxTX pin is controlled by UARTx
 - 0 = Transmit is disabled, any pending transmission is aborted and buffer is reset; UxTX pin is controlled by the PORT
- bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
 - 1 = Transmit buffer is full
 - 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
 - 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
 - 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
- bit 7-6 URXISEL<1:0>: UARTx Receive Interrupt Mode Selection bits
 - 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
 - 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
 - 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters
- Note 1: Refer to the "UART" (DS70582) section in the "dsPIC33/PIC24 Family Reference Manual" for information on enabling the UARTx module for transmit operation.

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R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1
bit 15				·	- -	·	bit 8
U-x	U-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
_	—	—	RB0	DLC3	DLC2	DLC1	DLC0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set	t	'0' = Bit is cleared x = Bit is unknown			nown
bit 15-10	EID<5:0>: E>	ktended Identifi	er bits				
bit 9	RTR: Remote	e Transmission	Request bit				
	When IDE =	<u>1:</u>					
	1 = Message	will request re	mote transmis	ssion			
		lessage					
	<u>When IDE = (</u> The RTR bit i	<u>0:</u> is ignored					
hit 9	BB1 : Boson	od Dit 1					
DILO	Llear must so	t this hit to '0'	oor CAN proto				
DIT 7-5	Unimplemen	ted: Read as	0				
bit 4	RB0: Reserve	ed Bit 0					
	User must se	t this bit to '0' p	per CAN proto	COI.			

BUFFER 21-3: ECAN™ MESSAGE BUFFER WORD 2

bit 3-0 DLC<3:0>: Data Length Code bits

BUFFER 21-4: ECAN[™] MESSAGE BUFFER WORD 3

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			B	/te 1			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			B	/te 0			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'			
-n = Value at POR '1' = Bit is s		'1' = Bit is set		'0' = Bit is cleared x = Bit is unkno			nown

bit 15-8 Byte 1<15:8>: ECAN Message Byte 1 bits

bit 7-0 Byte 0<7:0>: ECAN Message Byte 0 bits

23.4 ADC Control Registers

REGISTER 23-1: AD1CON1: ADC1 CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM1	FORM0
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC, HS	R/C-0, HC, HS
SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE ⁽³⁾
bit 7						-	bit 0
Legend:		HC = Hardwa	re Clearable bit	HS = Hardwa	re Settable bit	C = Clearable bi	t
R = Readab	le bit	W = Writable I	bit	U = Unimpler	nented bit, read	d as '0'	
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unknow	vn
bit 15	ADON: ADO	C1 Operating N	lode bit				
	1 = ADC mo	odule is operati	ng				
	0 = ADC is	off					
bit 14	Unimpleme	ented: Read as	'0'				
bit 13	ADSIDL: AI	DC1 Stop in Idle	e Mode bit				
	1 = Disconti	inues module o	peration when	device enters	Idle mode		
	0 = Continu	es module ope	ration in Idle mo	ode			
bit 12	ADDMABM	: DMA Buffer E	Build Mode bit				
	1 = DMA b	uffers are writte	en in the order	of conversion	; the module p	provides an addre	ess to the DMA
	0 = DMA bi	uffers are writte	en in Scatter/Ga	ther mode: the	e module prov	ides a Scatter/Ga	ther address to
	the DM	A channel, bas	ed on the index	of the analog	input and the	size of the DMA	ouffer.
bit 11	Unimpleme	ented: Read as	'0'				
bit 10	AD12B: AD	C1 10-Bit or 12	2-Bit Operation	Mode bit			
	1 = 12-bit, 1	-channel ADC	operation				
	0 = 10-bit, 4	-channel ADC	operation				
bit 9-8	FORM<1:0	>: Data Output	Format bits				
	For 10-Bit C	Operation:					
	11 = Signed	d fractional (Do	UT = sddd ddd	ld dd00 000	0, where $s = $.	NOT.d<9>)	
	10 = Fractions	hai (DOUT = ac	100 0000 000 = cccc cccd		where $c = N($	(<0>b TC	
	00 = Intege	r (Dout = 0000	00dd dddd	dddd)		51.u (0 ²)	
	For 12-Bit C	Deration:		,			
	11 = Signed	fractional (Do	UT = sddd ddd	ld dddd 000	0, where $s = .$	NOT.d<11>)	
	10 = Fractic	onal (Dout = do	ldd dddd ddd	ld 0000)			
	00 = Intege	r (DOUT = 0000	- ssss sada) dddd dddd	aaaa aaad, dddd)	where $s = .NC$	JI.U<112)	
		. (2001 - 0000		adduj			
Note 1: S	See Section 24	1.0 "Peripheral	l Trigger Gene	rator (PTG) M	odule" for info	ormation on this s	election.

- 2: This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- 3: Do not clear the DONE bit in software if Auto-Sample is enabled (ASAM = 1).

NOTES:

Bit Field	Description
WDTPRE	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
WDTPOST<3:0>	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • • • • • • • • • • •
WDTWIN<1:0>	Watchdog Window Select bits 11 = WDT window is 25% of WDT period 10 = WDT window is 37.5% of WDT period 01 = WDT window is 50% of WDT period 00 = WDT window is 75% of WDT period
ALTI2C1	Alternate I2C1 pin 1 = I2C1 is mapped to the SDA1/SCL1 pins 0 = I2C1 is mapped to the ASDA1/ASCL1 pins
ALTI2C2	Alternate I2C2 pin 1 = I2C2 is mapped to the SDA2/SCL2 pins 0 = I2C2 is mapped to the ASDA2/ASCL2 pins
JTAGEN ⁽²⁾	JTAG Enable bit 1 = JTAG is enabled 0 = JTAG is disabled
ICS<1:0>	ICD Communication Channel Select bits 11 = Communicate on PGEC1 and PGED1 10 = Communicate on PGEC2 and PGED2 01 = Communicate on PGEC3 and PGED3 00 = Reserved, do not use

TABLE 27-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

2: When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
53	NEG	NEG Acc ⁽¹⁾		Negate Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		NEG	f	$f = \overline{f} + 1$	1	1	C,DC,N,OV,Z
		NEG	f,WREG	WREG = \overline{f} + 1	1	1	C,DC,N,OV,Z
		NEG	Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
54	NOP	NOP		No Operation	1	1	None
		NOPR		No Operation	1	1	None
55	POP	POP	f	Pop f from Top-of-Stack (TOS)	1	1	None
		POP	Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
		POP.D	Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)	1	2	None
		POP.S		Pop Shadow Registers	1	1	All
56	PUSH	PUSH	f	Push f to Top-of-Stack (TOS)	1	1	None
		PUSH	Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
		PUSH.D	Wns	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None
		PUSH.S		Push Shadow Registers	1	1	None
57	PWRSAV	PWRSAV	#lit1	Go into Sleep or Idle mode	1	1	WDTO,Sleep
58	RCALL	RCALL	Expr	Relative Call	1	4	SFA
		RCALL	Wn	Computed Call	1	4	SFA
59	REPEAT	REPEAT	#lit15	Repeat Next Instruction lit15 + 1 times	1	1	None
		REPEAT	Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
60	RESET	RESET		Software device Reset	1	1	None
61	RETFIE	RETFIE		Return from interrupt	1	6 (5)	SFA
62	RETLW	RETLW	#lit10,Wn	Return with literal in Wn	1	6 (5)	SFA
63	RETURN	RETURN		Return from Subroutine	1	6 (5)	SFA
64	RLC	RLC	f	f = Rotate Left through Carry f	1	1	C,N,Z
		RLC	f,WREG	WREG = Rotate Left through Carry f	1	1	C,N,Z
		RLC	Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C,N,Z
65	RLNC	RLNC	f	f = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	f,WREG	WREG = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N,Z
66	RRC	RRC	f	f = Rotate Right through Carry f	1	1	C,N,Z
		RRC	f,WREG	WREG = Rotate Right through Carry f	1	1	C,N,Z
		RRC	Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C,N,Z
67	RRNC	RRNC	f	f = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	f,WREG	WREG = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	Ws,Wd	Wd = Rotate Right (No Carry) Ws	1	1	N,Z
68	SAC	SAC	Acc,#Slit4,Wdo()	Store Accumulator	1	1	None
		SAC.R	Acc,#Slit4,Wdo\''	Store Rounded Accumulator	1	1	None
69	SE	SE	Ws,Wnd	Wnd = sign-extended Ws	1	1	C,N,Z
10	SEIM	SEIM	I		1	1	None
		SEIM	WREG		1	1	None
71	SFTAC	SETM	ws Acc,Wn ⁽¹⁾	Arithmetic Shift Accumulator by (Wn)	1	1	OA,OB,OAB,
		SFTAC	Acc,#Slit6 ⁽¹⁾	Arithmetic Shift Accumulator by Slit6	1	1	OA,OB,OAB,

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

31.0 HIGH-TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between -40° C to $+150^{\circ}$ C are identical to those shown in **Section 30.0** "**Electrical Characteristics**" for operation between -40° C to $+125^{\circ}$ C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter DC10 in **Section 30.0 "Electrical Characteristics"** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X high-temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias ⁽²⁾	40°C to +150°C
Storage temperature	65°C to +160°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to Vss ⁽³⁾	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when VDD < 3.0V ⁽³⁾	-0.3V to 3.6V
Voltage on any 5V tolerant pin with respect to Vss when $VDD \ge 3.0V^{(3)}$	-0.3V to 5.5V
Maximum current out of Vss pin	60 mA
Maximum current into VDD pin ⁽⁴⁾	60 mA
Maximum junction temperature	+155°C
Maximum current sourced/sunk by any 4x I/O pin	
Maximum current sourced/sunk by any 8x I/O pin	
Maximum current sunk by all ports combined	
Maximum current sourced by all ports combined ⁽⁴⁾	70 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.
 - 2: AEC-Q100 reliability testing for devices intended to operate at +150°C is 1,000 hours. Any design in which the total operating time from +125°C to +150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.
 - 3: Refer to the "Pin Diagrams" section for 5V tolerant pins.
 - 4: Maximum allowable current is a function of device maximum power dissipation (see Table 31-2).

33.2 Package Details

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES	
Dimensio	n Limits	MIN	NOM	MAX
Number of Pins	Ν		28	
Pitch	е		.100 BSC	
Top to Seating Plane	А	-	-	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	С	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	_	_	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-187C Sheet 1 of 2

APPENDIX A: REVISION HISTORY

Revision A (April 2011)

This is the initial released version of the document.

Revision B (July 2011)

This revision includes minor typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-1.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Digital Signal Controllers and Microcontrollers"	Changed all pin diagrams references of VLAP to TLA.
Section 4.0 "Memory Organization"	Updated the All Resets values for CLKDIV and PLLFBD in the System Control Register Map (see Table 4-35).
Section 5.0 "Flash Program Memory"	Updated "one word" to "two words" in the first paragraph of Section 5.2 "RTSP Operation" .
Section 9.0 "Oscillator Configuration"	Updated the PLL Block Diagram (see Figure 9-2). Updated the Oscillator Mode, Fast RC Oscillator (FRC) with divide-by-N and PLL (FRCPLL), by changing (FRCDIVN + PLL) to (FRCPLL).
	Changed (FRCDIVN + PLL) to (FRCPLL) for COSC<2:0> = 001 and NOSC<2:0> = 001 in the Oscillator Control Register (see Register 9-1).
	Changed the POR value from 0 to 1 for the DOZE<1:0> bits, from 1 to 0 for the FRCDIV<0> bit, and from 0 to 1 for the PLLPOST<0> bit; Updated the default definitions for the DOZE<2:0> and FRCDIV<2:0> bits and updated all bit definitions for the PLLPOST<1:0> bits in the Clock Divisor Register (see Register 9-2).
	Changed the POR value from 0 to 1 for the PLLDIV<5:4> bits and updated the default definitions for all PLLDIV<8:0> bits in the PLL Feedback Division Register (see Register 9-2).
Section 22.0 "Charge Time Measurement Unit (CTMU)"	Updated the bit definitions for the IRNG<1:0> bits in the CTMU Current Control Register (see Register 22-3).
Section 25.0 "Op amp/ Comparator Module"	Updated the voltage reference block diagrams (see Figure 25-1 and Figure 25-2).