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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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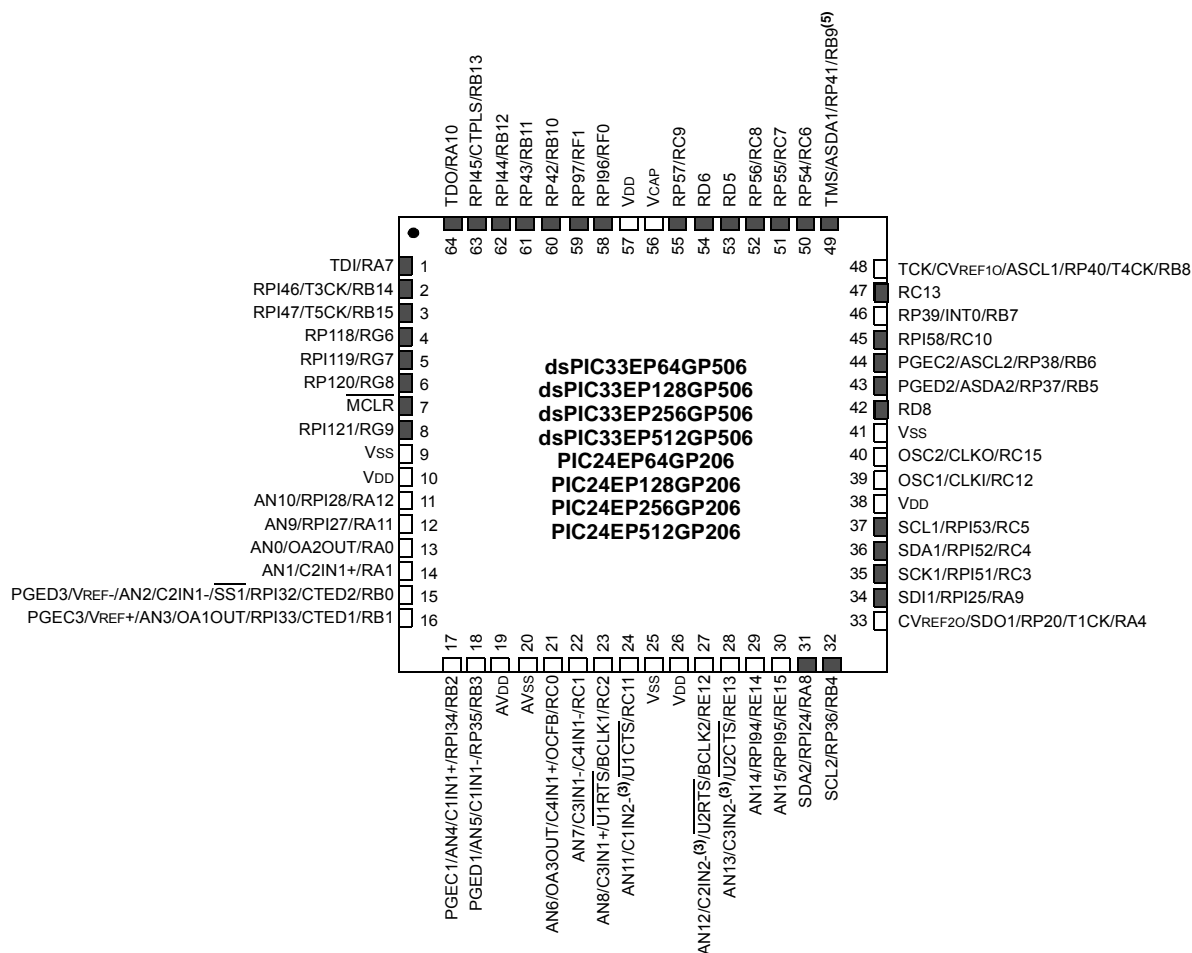
Details

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64gp506t-e-pt

Pin Diagrams (Continued)

64-Pin QFN^(1,2,3,4)

■ = Pins are up to 5V tolerant



- Note 1:** The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** This pin is not available as an input when OPMODE (CMxCON<10>) = 1.
- Note 4:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
- Note 5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to $3 \text{ MHz} < F_{IN} < 5.5 \text{ MHz}$ to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start-up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLFBD, to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between Vss and unused pins, and drive the output to logic low.

2.9 Application Examples

- Induction heating
- Uninterruptable Power Supplies (UPS)
- DC/AC inverters
- Compressor motor control
- Washing machine 3-phase motor control
- BLDC motor control
- Automotive HVAC, cooling fans, fuel pumps
- Stepper motor control
- Audio and fluid sensor monitoring
- Camera lens focus and stability control
- Speech (playback, hands-free kits, answering machines, VoIP)
- Consumer audio
- Industrial and building control (security systems and access control)
- Barcode reading
- Networking: LAN switches, gateways
- Data storage device management
- Smart cards and smart card readers

Examples of typical application connections are shown in Figure 2-4 through Figure 2-8.

FIGURE 2-4: BOOST CONVERTER IMPLEMENTATION

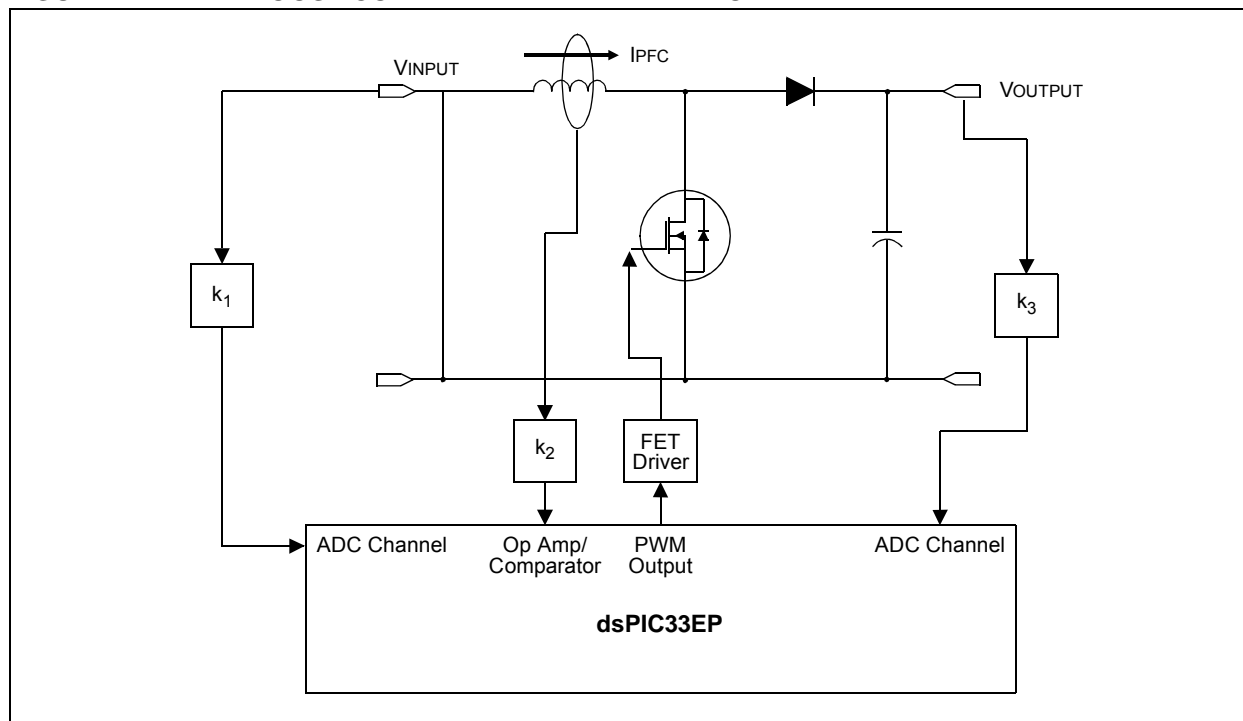
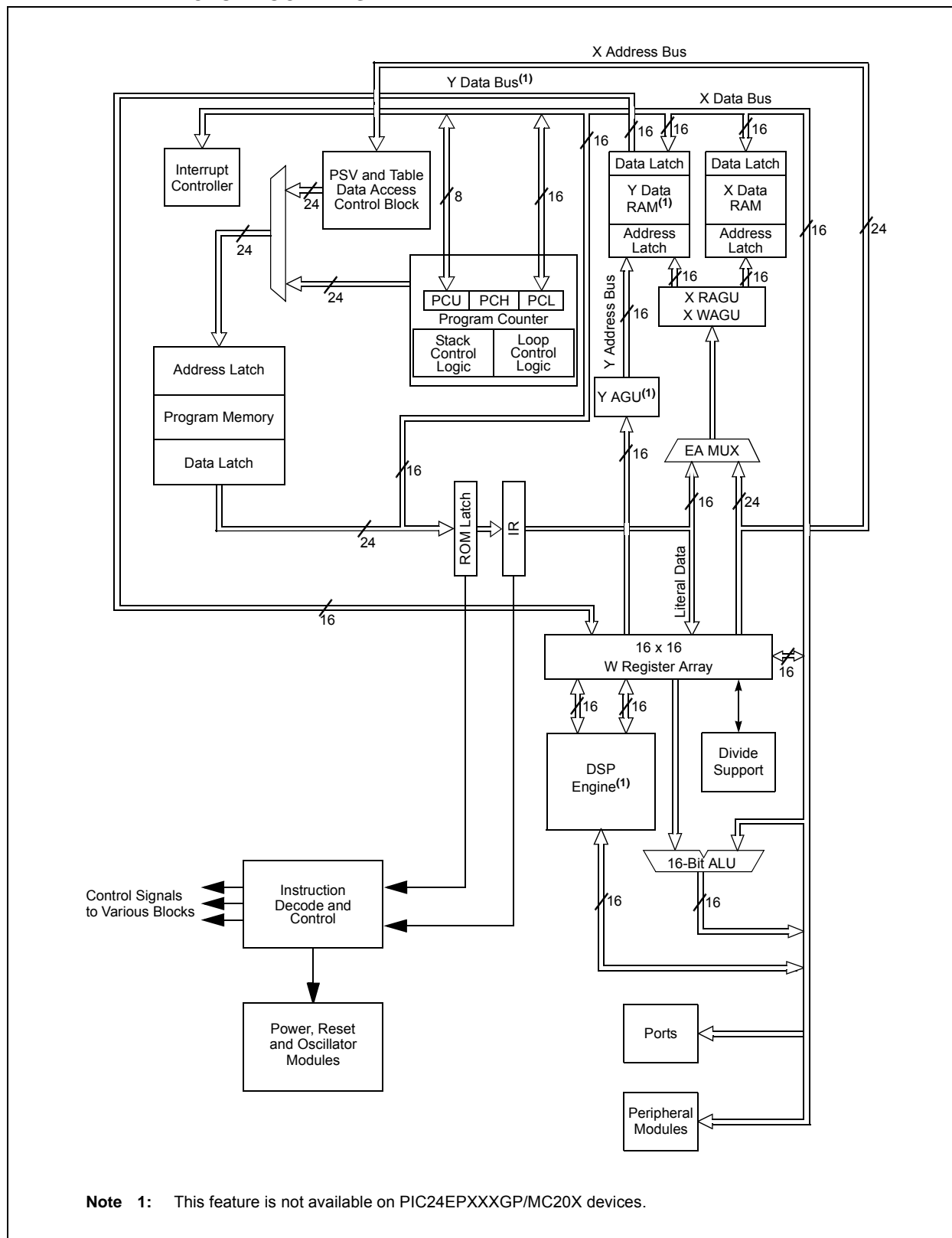


FIGURE 3-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X CPU BLOCK DIAGRAM



4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Program Memory**” (DS70613) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

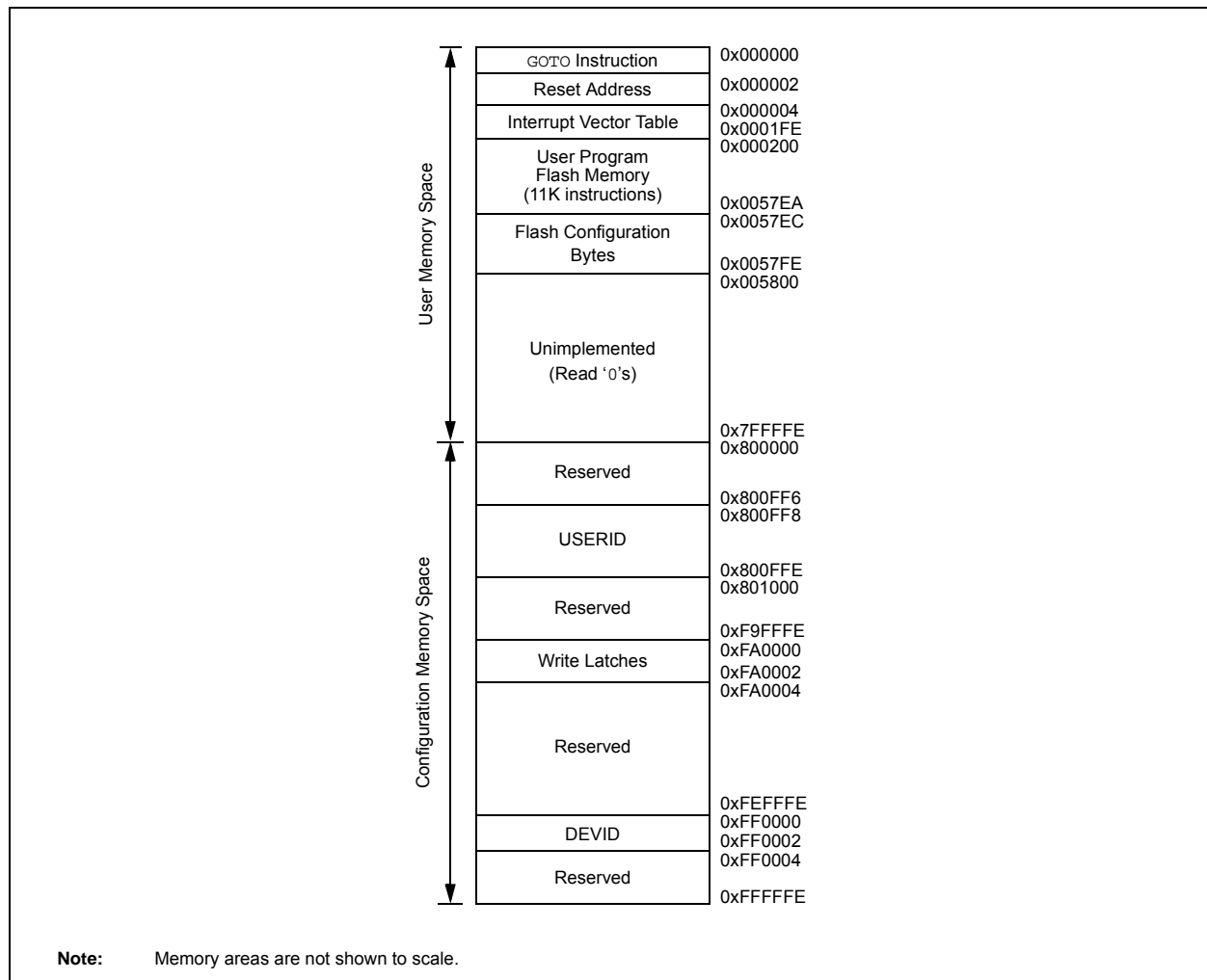
4.1 Program Address Space

The program address memory space of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in **Section 4.8 “Interfacing Program and Data Memory Spaces”**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to read Device ID sections of the configuration memory space.

The program memory maps, which are presented by device family and memory size, are shown in Figure 4-1 through Figure 4-5.

FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X AND PIC24EP32GP/MC20X DEVICES



4.4 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXMC20X/50X AND dsPIC33EPXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
W0	0000	W0 (WREG)																	xxxx
W1	0002	W1																	xxxx
W2	0004	W2																	xxxx
W3	0006	W3																	xxxx
W4	0008	W4																	xxxx
W5	000A	W5																	xxxx
W6	000C	W6																	xxxx
W7	000E	W7																	xxxx
W8	0010	W8																	xxxx
W9	0012	W9																	xxxx
W10	0014	W10																	xxxx
W11	0016	W11																	xxxx
W12	0018	W12																	xxxx
W13	001A	W13																	xxxx
W14	001C	W14																	xxxx
W15	001E	W15																	xxxx
SPLIM	0020	SPLIM																	0000
ACCAL	0022	ACCAL																	0000
ACCAH	0024	ACCAH																	0000
ACCAU	0026	Sign Extension of ACCA<39>										ACCAU							0000
ACCBH	0028	ACCBH																	0000
ACCBH	002A	ACCBH																	0000
ACCBU	002C	Sign Extension of ACCB<39>										ACCBU							0000
PCL	002E	PCL<15:0>																—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	PCH<6:0>							0000	
DSRPAG	0032	—	—	—	—	—	—	DSRPAG<9:0>										0001	
DSWPAG	0034	—	—	—	—	—	—	—	DSWPAG<8:0>										0001
RCOUNT	0036	RCOUNT<15:0>																	0000
DCOUNT	0038	DCOUNT<15:0>																	0000
DOSTARTL	003A	DOSTARTL<15:1>																—	0000
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DOSTARTH<5:0>						0000	
DOENDL	003E	DOENDL<15:1>																—	0000
DOENDH	0040	—	—	—	—	—	—	—	—	—	—	DOENDH<5:0>						0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-49: PORTD REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	0E30	—	—	—	—	—	—	—	TRISD8	—	TRISD6	TRISD5	—	—	—	—	—	0160
PORTD	0E32	—	—	—	—	—	—	—	RD8	—	RD6	RD5	—	—	—	—	—	xxxx
LATD	0E34	—	—	—	—	—	—	—	LATD8	—	LATD6	LATD5	—	—	—	—	—	xxxx
ODCD	0E36	—	—	—	—	—	—	—	ODCD8	—	ODCD6	ODCD5	—	—	—	—	—	0000
CNEND	0E38	—	—	—	—	—	—	—	CNIED8	—	CNIED6	CNIED5	—	—	—	—	—	0000
CNPUD	0E3A	—	—	—	—	—	—	—	CNPUD8	—	CNPUD6	CNPUD5	—	—	—	—	—	0000
CNPDD	0E3C	—	—	—	—	—	—	—	CNPDD8	—	CNPDD6	CNPDD5	—	—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-50: PORTE REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISE	0E40	TRISE15	TRISE14	TRISE13	TRISE12	—	—	—	—	—	—	—	—	—	—	—	—	F000
PORTE	0E42	RE15	RE14	RE13	RE12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
LATE	0E44	LATE15	LATE14	LATE13	LATE12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
ODCE	0E46	ODCE15	ODCE14	ODCE13	ODCE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNENE	0E48	CNIEE15	CNIEE14	CNIEE13	CNIEE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPUE	0E4A	CNPUE15	CNPUE14	CNPUE13	CNPUE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPDE	0E4C	CNPDE15	CNPDE14	CNPDE13	CNPDE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
ANSELE	0E4E	ANSE15	ANSE14	ANSE13	ANSE12	—	—	—	—	—	—	—	—	—	—	—	—	F000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-51: PORTF REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRISF1	TRISF0	0003
PORTF	0E52	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RF1	RF0	xxxx
LATF	0E54	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LATF1	LATF0	xxxx
ODCF	0E56	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODCF1	ODCF0	0000
CNENF	0E58	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNIEF1	CNIEF0	0000
CNPUF	0E5A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPUF1	CNPUF0	0000
CNPDF	0E5C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPDF1	CNPDF0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 8-7: DMAxPAD: DMA CHANNEL x PERIPHERAL ADDRESS REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PAD<15:0>**: Peripheral Address Register bits

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-8: DMAxCNT: DMA CHANNEL x TRANSFER COUNT REGISTER⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CNT<13:8> ⁽²⁾					
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNT<7:0> ⁽²⁾							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **CNT<13:0>**: DMA Transfer Count Register bits⁽²⁾

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

2: The number of DMA transfers = CNT<13:0> + 1.

REGISTER 11-22: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP43R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP42R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'
bit 13-8 **RP43R<5:0>:** Peripheral Output Function is Assigned to RP43 Output Pin bits
(see Table 11-3 for peripheral function numbers)
bit 7-6 **Unimplemented:** Read as '0'
bit 5-0 **RP42R<5:0>:** Peripheral Output Function is Assigned to RP42 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 11-23: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP55R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP54R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'
bit 13-8 **RP55R<5:0>:** Peripheral Output Function is Assigned to RP55 Output Pin bits
(see Table 11-3 for peripheral function numbers)
bit 7-6 **Unimplemented:** Read as '0'
bit 5-0 **RP54R<5:0>:** Peripheral Output Function is Assigned to RP54 Output Pin bits
(see Table 11-3 for peripheral function numbers)

NOTES:

REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN ⁽²⁾	CKP	MSTEN	SPRE2 ⁽³⁾	SPRE1 ⁽³⁾	SPRE0 ⁽³⁾	PPRE1 ⁽³⁾	PPRE0 ⁽³⁾
bit 7							bit 0

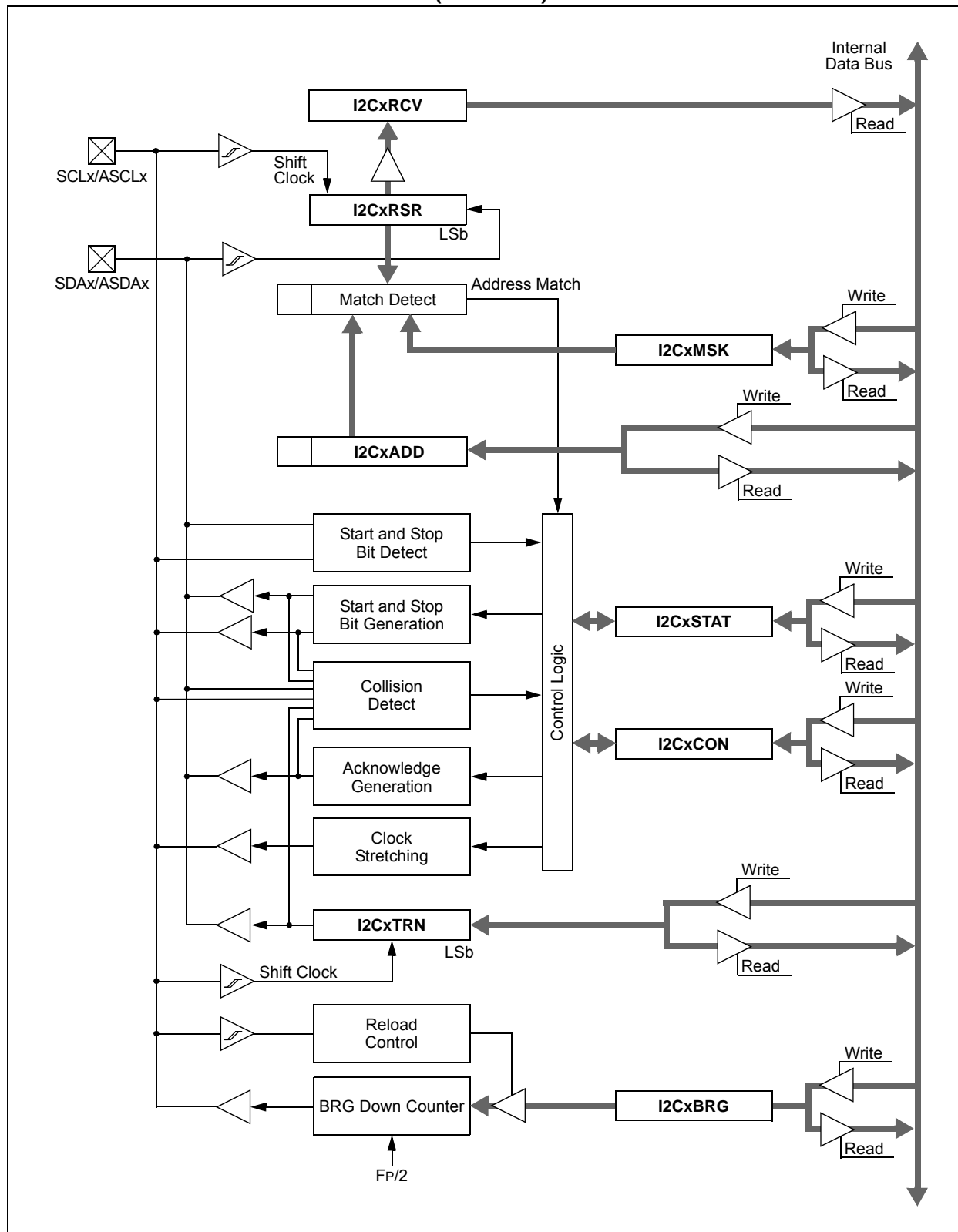
Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-13 **Unimplemented:** Read as '0'
- bit 12 **DISSCK:** Disable SCKx Pin bit (SPIx Master modes only)
 1 = Internal SPIx clock is disabled, pin functions as I/O
 0 = Internal SPIx clock is enabled
- bit 11 **DISSDO:** Disable SDOx Pin bit
 1 = SDOx pin is not used by the module; pin functions as I/O
 0 = SDOx pin is controlled by the module
- bit 10 **MODE16:** Word/Byte Communication Select bit
 1 = Communication is word-wide (16 bits)
 0 = Communication is byte-wide (8 bits)
- bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master mode:
 1 = Input data is sampled at end of data output time
 0 = Input data is sampled at middle of data output time
Slave mode:
 SMP must be cleared when SPIx is used in Slave mode.
- bit 8 **CKE:** SPIx Clock Edge Select bit⁽¹⁾
 1 = Serial output data changes on transition from active clock state to Idle clock state (refer to bit 6)
 0 = Serial output data changes on transition from Idle clock state to active clock state (refer to bit 6)
- bit 7 **SSEN:** Slave Select Enable bit (Slave mode)⁽²⁾
 1 = \overline{SSx} pin is used for Slave mode
 0 = \overline{SSx} pin is not used by the module; pin is controlled by port function
- bit 6 **CKP:** Clock Polarity Select bit
 1 = Idle state for clock is a high level; active state is a low level
 0 = Idle state for clock is a low level; active state is a high level
- bit 5 **MSTEN:** Master Mode Enable bit
 1 = Master mode
 0 = Slave mode

- Note 1:** The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
Note 2: This bit must be cleared when FRMEN = 1.
Note 3: Do not set both primary and secondary prescalers to the value of 1:1.

FIGURE 19-1: I2Cx BLOCK DIAGRAM (x = 1 OR 2)



21.2 Modes of Operation

The ECAN module can operate in one of several operation modes selected by the user. These modes include:

- Initialization mode
- Disable mode
- Normal Operation mode
- Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

21.3 ECAN Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

21.3.1 KEY RESOURCES

- **“Enhanced Controller Area Network (ECAN™)”** (DS70353) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

24.3 PTG Control Registers

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGEN	—	PTGSIDL	PTGTOGL	—	PTGSWT ⁽²⁾	PTGSSEN ⁽³⁾	PTGIVIS
bit 15				bit 8			

R/W-0	HS-0	U-0	U-0	U-0	U-0	R/W-0	
PTGSTRT	PTGWDTO	—	—	—	—	PTGITM1 ⁽¹⁾	PTGITM0 ⁽¹⁾
bit 7				bit 0			

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **PTGEN:** Module Enable bit
 1 = PTG module is enabled
 0 = PTG module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **PTGSIDL:** PTG Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12 **PTGTOGL:** PTG TRIG Output Toggle Mode bit
 1 = Toggle state of the PTGOx for each execution of the PTGTRIG command
 0 = Each execution of the PTGTRIG command will generate a single PTGOx pulse determined by the value in the PTGPWDx bits
- bit 11 **Unimplemented:** Read as '0'
- bit 10 **PTGSWT:** PTG Software Trigger bit⁽²⁾
 1 = Triggers the PTG module
 0 = No action (clearing this bit will have no effect)
- bit 9 **PTGSSEN:** PTG Enable Single-Step bit⁽³⁾
 1 = Enables Single-Step mode
 0 = Disables Single-Step mode
- bit 8 **PTGIVIS:** PTG Counter/Timer Visibility Control bit
 1 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the current values of their corresponding counter/timer registers (PTGSD, PTGCx, PTGTx)
 0 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the value previously written to those limit registers
- bit 7 **PTGSTRT:** PTG Start Sequencer bit
 1 = Starts to sequentially execute commands (Continuous mode)
 0 = Stops executing commands
- bit 6 **PTGWDTO:** PTG Watchdog Timer Time-out Status bit
 1 = PTG Watchdog Timer has timed out
 0 = PTG Watchdog Timer has not timed out.
- bit 5-2 **Unimplemented:** Read as '0'

- Note 1:** These bits apply to the PTGWHI and PTGWLO commands only.
- Note 2:** This bit is only used with the PTGCTRL step command software trigger option.
- Note 3:** Use of the PTG Single-Step mode is reserved for debugging tools only.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
52	MUL	MUL.SS Wb, Ws, Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SS Wb, Ws, Acc ⁽¹⁾	Accumulator = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU Wb, Ws, Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb, Ws, Acc ⁽¹⁾	Accumulator = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb, #lit5, Acc ⁽¹⁾	Accumulator = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.US Wb, Ws, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.US Wb, Ws, Acc ⁽¹⁾	Accumulator = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU Wb, Ws, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.UU Wb, #lit5, Acc ⁽¹⁾	Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb, Ws, Acc ⁽¹⁾	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1	None
		MULW.SS Wb, Ws, Wnd	Wnd = signed(Wb) * signed(Ws)	1	1	None
		MULW.SU Wb, Ws, Wnd	Wnd = signed(Wb) * unsigned(Ws)	1	1	None
		MULW.US Wb, Ws, Wnd	Wnd = unsigned(Wb) * signed(Ws)	1	1	None
		MULW.UU Wb, Ws, Wnd	Wnd = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb, #lit5, Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.SU Wb, #lit5, Wnd	Wnd = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb, #lit5, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb, #lit5, Wnd	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL f	W3:W2 = f * WREG	1	1	None

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 30-22: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SY00	TPU	Power-up Period	—	400	600	μs	
SY10	TOST	Oscillator Start-up Time	—	1024 TOSC	—	—	TOSC = OSC1 period
SY12	TWDT	Watchdog Timer Time-out Period	0.81	0.98	1.22	ms	WDTPRE = 0, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21 (see Table 30-20) at +85°C
			3.26	3.91	4.88	ms	WDTPRE = 1, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21 (see Table 30-20) at +85°C
SY13	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	0.68	0.72	1.2	μs	
SY20	TMCLR	MCLR Pulse Width (low)	2	—	—	μs	
SY30	TBOR	BOR Pulse Width (low)	1	—	—	μs	
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	500	900	μs	-40°C to +85°C
SY36	TVREG	Voltage Regulator Standby-to-Active mode Transition Time	—	—	30	μs	
SY37	TOSCDFRC	FRC Oscillator Start-up Delay	46	48	54	μs	
SY38	TOSCDLPRC	LPRC Oscillator Start-up Delay	—	—	70	μs	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)
TIMING CHARACTERISTICS**

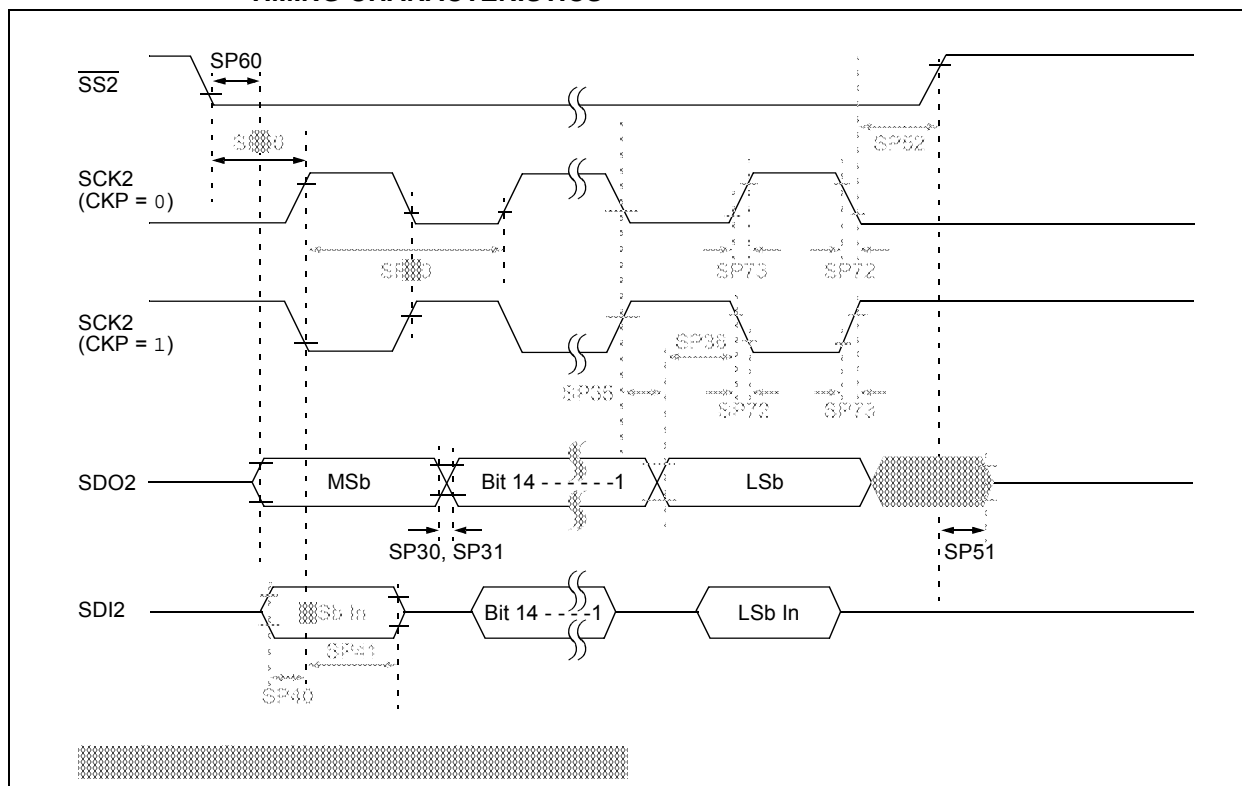
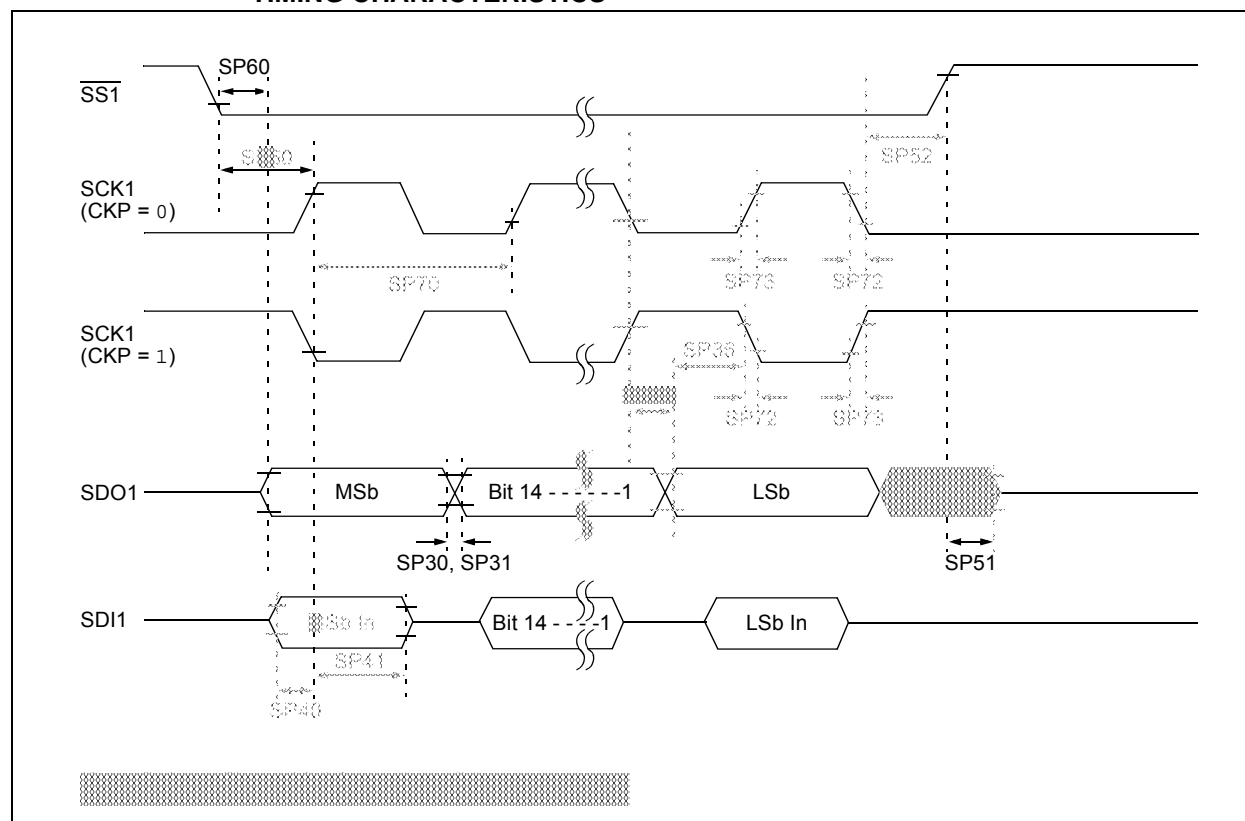


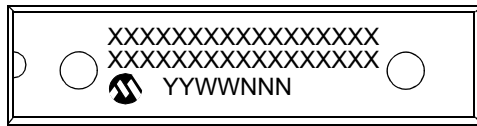
FIGURE 30-27: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)
TIMING CHARACTERISTICS



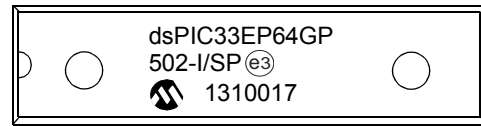
33.0 PACKAGING INFORMATION

33.1 Package Marking Information

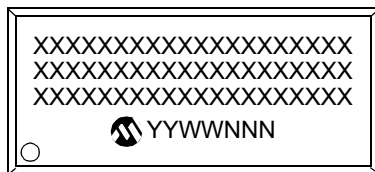
28-Lead SPDIP



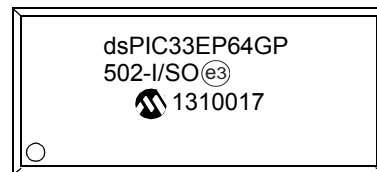
Example



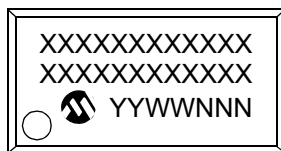
28-Lead SOIC (.300")



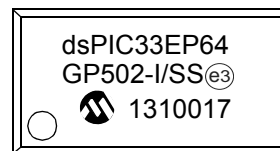
Example



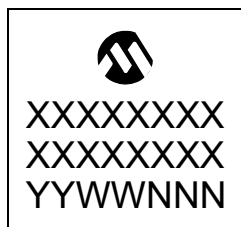
28-Lead SSOP



Example



28-Lead QFN-S (6x6x0.9 mm)



Example

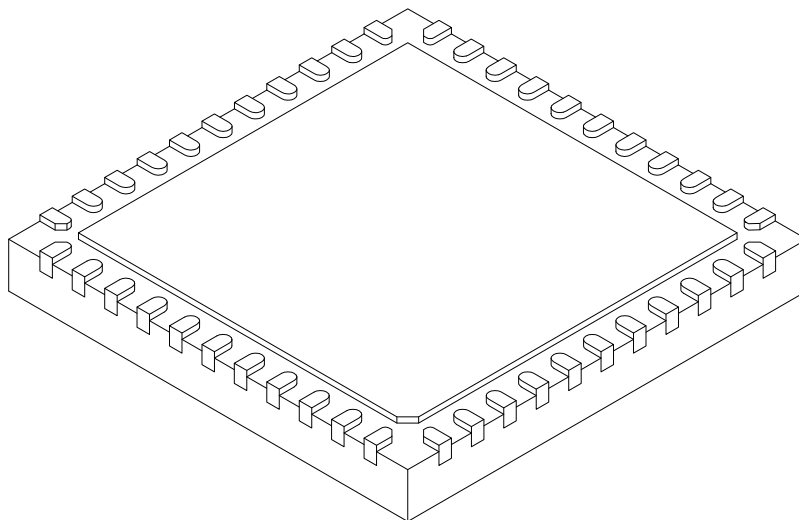


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	44		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	E	8.00 BSC		
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D	8.00 BSC		
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension. usually without tolerance. for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2

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