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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

ХF

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64mc202-e-sp

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Pin Diagrams (Continued)



REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 2	SFA: Stack Frame Active Status bit
	1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and
	DSWPAG values
	0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space
hit 1	PND: Dounding Mode Select hit(1)

- bit 1 **RND:** Rounding Mode Select bit⁽¹⁾
 - 1 = Biased (conventional) rounding is enabled
 - 0 = Unbiased (convergent) rounding is enabled

bit 0 IF: Integer or Fractional Multiplier Mode Select bit⁽¹⁾ 1 = Integer mode is enabled for DSP multiply 0 = Fractional mode is enabled for DSP multiply

- Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.
 - **2:** This bit is always read as '0'.
 - 3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC35	0886	—		JTAGIP<2:0)>	—		ICDIP<2:0	>	—	_	—	—	_	_	—	-	4400
IPC36	0888	_		PTG0IP<2:0)>	_	PT	GWDTIP<	2:0>	_	PT	GSTEPIP<2	::0>	_	_	_	_	4440
IPC37	088A	_	_	_	_	_	F	PTG3IP<2:	0>	_		PTG2IP<2:0	>	_	I	PTG1IP<2:0>		0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	_	_	_	_	_	_	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	_	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	_	—	_	—	—	_	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	_	_	_	—	_	—	_	DAE	DOOVR	—	—	—		0000
INTCON4	08C6	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	SGHT	0000
INTTREG	08C8	_	_	_	_		ILR<3:0>						VECN	IUM<7:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



EXAMPLE 4-2: EXTENDED DATA SPACE (EDS) WRITE ADDRESS GENERATION

The paged memory scheme provides access to multiple 32-Kbyte windows in the EDS and PSV memory. The Data Space Page registers, DSxPAG, in combination with the upper half of the Data Space address, can provide up to 16 Mbytes of additional address space in the EDS and 8 Mbytes (DSRPAG only) of PSV address space. The paged data memory space is shown in Example 4-3.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG. Writes to PS are not supported, so DSWPAG is dedicated to DS, including EDS only. The Data Space and EDS can be read from, and written to, using DSRPAG and DSWPAG, respectively.

10.2.1 SLEEP MODE

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- · Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into Standby when Sleep mode is entered by clearing the VREGS (RCON<8>) and VREGSF (RCON<11>) bits (default configuration).

If the application requires a faster wake-up time, and can accept higher current requirements, the VREGS (RCON<8>) and VREGSF (RCON<11>) bits can be set to keep the internal regulator and the Flash regulator active during Sleep mode.

10.2.2 IDLE MODE

The following occurs in Idle mode:

- The CPU stops executing instructions.
- · The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see Section 10.4 "Peripheral Module Disable").
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- · Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction or the first instruction in the Interrupt Service Routine (ISR).

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral; for example, the TSIDL bit in the Timer1 Control register (T1CON<13>).

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

REGISTER 11-9: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
—				HOME1R<6:0	>							
bit 15							bit 8					
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
—				INDX1R<6:0>	>							
bit 7							bit 0					
Legend:												
R = Readab	ole bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'						
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown					
bit 15	Unimpleme	ented: Read as '	0'									
bit 15 bit 14-8	HOME1R<6	5:0>: Assign QEI	0 1 HOME1 (H selection nun	OME1) to the C	Corresponding	RPn Pin bits						
	1111001 =	1111001 = Input tied to RPI121										
		Input tied to CM	D1									
	0000000 =	Input tied to Vss	;									
bit 7	Unimpleme	ented: Read as '	0'									
bit 6-0	IND1XR<6: (see Table 2	0>: Assign QEI1 I1-2 for input pin	INDEX1 (INE selection nun	0X1) to the Cor nbers)	responding R	Pn Pin bits						
	1111001 =	Input tied to RPI	121	,								
	•											
	0000001 =	Input tied to CM	P1									
	0000000 =	Input tied to Vss										

U-0	U-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0			
	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN			
bit 15							bit 8			
HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0			
PCIIRQ ⁽¹⁾	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN			
bit 7							bit 0			
Legend:		HS = Hardware Settable bit C = Clearable bit								
R = Readable	bit	W = Writable b	bit	U = Unimpler	nented bit, rea	d as '0'				
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	IOWN			
bit 15-14	Unimplemen	ted: Read as '0			01.1	.,				
DIT 13			er Greater Tha	n or Equal Con	npare Status b	It				
	0 = POS1CN	T < QEI1GEC								
bit 12	PCHEQIEN:	Position Counte	r Greater Tha	n or Equal Con	npare Interrupt	Enable bit				
	1 = Interrupt i	s enabled								
	0 = Interrupt i	s disabled								
bit 11	PCLEQIRQ:	Position Counte	r Less Than o	r Equal Compa	are Status bit					
	$1 = POS1CN^{-1}$	$T \leq QEI1LEC$								
bit 10		Position Counte	r Less Than or	r Equal Compa	re Interrupt En	able bit				
	1 = Interrupt i	s enabled								
	0 = Interrupt i	s disabled								
bit 9	POSOVIRQ:	Position Counte	er Overflow Sta	atus bit						
	1 = Overflow	has occurred								
h it 0		ow has occurred) n Overflevv linte	ann at Eachlach	.:.					
DIL 8	1 = Interrupt i	Position Counte	r Overnow Inte	errupt Enable b	nt					
	0 = Interrupt i	s disabled								
bit 7	PCIIRQ: Posi	ition Counter (H	oming) Initializ	ation Process	Complete Stat	us bit ⁽¹⁾				
	1 = POS1CN	T was reinitialize	ed							
	$0 = POS1CN^{-1}$	T was not reiniti	alized							
bit 6	PCIIEN: Posit	tion Counter (He	oming) Initializ	ation Process	Complete inter	rupt Enable bit				
	1 = Interrupt i	s enabled								
bit 5		Velocity Counte	r Overflow Sta	tus bit						
Sit O	1 = Overflow	has occurred								
	0 = No overflo	ow has not occu	irred							
bit 4	VELOVIEN: \	/elocity Counter	Overflow Inte	rrupt Enable bi	it					
	1 = Interrupt i	s enabled								
L # 0		s disabled		ua hit						
DIL 3		at has occurred	me ⊨vent Stati	us dil						
	0 = No Home	event has occure	irred							

REGISTER 17-3: QEI1STAT: QEI1 STATUS REGISTER

Note 1: This status bit is only applicable to PIMOD<2:0> modes, '011' and '100'.

REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER (CONTINUED)

- bit 1 **RBIF:** RX Buffer Interrupt Flag bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 0 **TBIF:** TX Buffer Interrupt Flag bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred

BUFFER 21-7: ECAN™ MESSAGE BUFFER WORD 6

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
	Byte 7										
bit 15							bit 8				
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
	Byte 6										
bit 7							bit 0				
Legend:											
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'											
-n = Value at POR '1' = Bit is set '			'0' = Bit is clea	ared	x = Bit is unkr	nown					

bit 15-8 Byte 7<15:8>: ECAN Message Byte 7 bits

bit 7-0 Byte 6<7:0>: ECAN Message Byte 6 bits

BUFFER 21-8: ECAN[™] MESSAGE BUFFER WORD 7

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	_	FILHIT4 ⁽¹⁾	FILHIT3 ⁽¹⁾	FILHIT2 ⁽¹⁾	FILHIT1 ⁽¹⁾	FILHITO ⁽¹⁾
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	—	_	—	_	_	—	—
bit 7							bit 0
Leaend:							

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13	Unimplemented: Read as '0'
bit 12-8	FILHIT<4:0>: Filter Hit Code bits ⁽¹⁾
	Encodes number of filter that resulted in writing this buffer.
bit 7-0	Unimplemented: Read as '0'

Note 1: Only written by module for receive buffers, unused for transmit buffers.

REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)

bit 4-0	CH0SA<4:0>: Channel 0 Positive Input Select for Sample MUXA bits ⁽¹⁾									
	11111 = Open; use this selection with CTMU capacitive and time measurement									
	11110 = Channel 0 positive input is connected to the CTMU temperature measurement diode (CTMU TEMP)									
	11101 = Reserved									
	11011 = Reserved									
	11010 = Channel 0 positive input is the output of OA3/AN6 ^(2,3)									
	11001 = Channel 0 positive input is the output of OA2/AN0 ⁽²⁾									
	11000 = Channel 0 positive input is the output of OA1/AN3 ⁽²⁾									
	10110 = Reserved									
	•									
	•									
	10000 = Reserved									
	01111 = Channel 0 positive input is $AN15^{(1,3)}$									
	01110 = Channel 0 positive input is AN14 ^(1,3)									
	•									
	•									
	00010 = Channel 0 positive input is AN2 ^(1,3)									
	00001 = Channel 0 positive input is AN0(1,3)									

- **Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.
 - 2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.
 - 3: See the "Pin Diagrams" section for the available analog channels for each device.

27.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a То comprehensive reference source. complement the information in this data sheet, refer to the related section of the "dsPIC33/PIC24 Familv Reference Manual', which is available from the Microchip web site (www.microchip.com).

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard[™] Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming[™] (ICSP[™])
- In-Circuit Emulation

27.1 Configuration Bits

In dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored in at the top of the on-chip program memory space, known as the Flash Configuration bytes. Their specific locations are shown in Table 27-1. The configuration data is automatically loaded from the Flash Configuration bytes to the proper Configuration Shadow registers during device Resets.

Note:	Configuration data is reloaded on all types
	of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration bytes for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled.

The upper 2 bytes of all Flash Configuration Words in program memory should always be '1111 1111 1111 1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '1's to these locations has no effect on device operation.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

The Configuration Flash bytes map is shown in Table 27-1.

27.5 Watchdog Timer (WDT)

For dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

27.5.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a WDT Timeout period (TWDT), as shown in Parameter SY12 in Table 30-22.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- · On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution
- Note: The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.



FIGURE 27-2: WDT BLOCK DIAGRAM

27.5.2 SLEEP AND IDLE MODES

If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes the device and code execution continues from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON<3,2>) needs to be cleared in software after the device wakes up.

27.5.3 ENABLING WDT

The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

27.5.4 WDT WINDOW

The Watchdog Timer has an optional Windowed mode, enabled by programming the WINDIS bit in the WDT Configuration register (FWDT<6>). In the Windowed mode (WINDIS = 0), the WDT should be cleared based on the settings in the programmable Watchdog Timer Window select bits (WDTWIN<1:0>).

29.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM[™] and dsPICDEM[™] demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ[®] security ICs, CAN, IrDA[®], PowerSmart battery management, SEEVAL[®] evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

29.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent[®] and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika[®]

DC CHARACTI	ERISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Parameter No.	Тур.	Max.	Units		Conditions			
Idle Current (II	dle) ⁽¹⁾							
DC40d	3	8	mA	-40°C				
DC40a	3	8	mA	+25°C	2 21/			
DC40b	3	8	mA	+85°C	3.3V	10 1011-5		
DC40c	3	8	mA	+125°C				
DC42d	6	12	mA	-40°C				
DC42a	6	12	mA	+25°C	3 3\/	20 MIPS		
DC42b	6	12	mA	+85°C	5.5 V	20 1011 3		
DC42c	6	12	mA	+125°C				
DC44d	11	18	mA	-40°C				
DC44a	11	18	mA	+25°C	3 3\/			
DC44b	11	18	mA	+85°C	5.5 V	40 1011 3		
DC44c	11	18	mA	+125°C				
DC45d	17	27	mA	-40°C				
DC45a	17	27	mA	+25°C	3 3\/	60 MIRS		
DC45b	17	27	mA	+85°C	5.5V	00 1011-3		
DC45c	17	27	mA	+125°C				
DC46d	20	35	mA	-40°C				
DC46a	20	35	mA	+25°C	3.3V	70 MIPS		
DC46b	20	35	mA	+85°C				

TABLE 30-7: DC CHARACTERISTICS: IDLE CURRENT (lidle)

Note 1: Base Idle current (IIDLE) is measured as follows:

• CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- · CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to Vss
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled



FIGURE 30-16: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS

TABLE 30-35:SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param.	Symbol	Characteristic ⁽¹⁾	Min. Typ. ⁽²⁾ Max. Units Conditions					
SP10	FscP	Maximum SCK2 Frequency		_	9	MHz	(Note 3)	
SP20	TscF	SCK2 Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)	
SP21	TscR	SCK2 Output Rise Time	—	—		ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO2 Data Output Fall Time	_			ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO2 Data Output Rise Time	—	_		ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns		
SP36	TdoV2sc, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_		ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30		_	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	_	ns		

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- **3:** The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.
- **4:** Assumes 50 pF load on all SPI2 pins.

TABLE 30-38:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param.	Symbol	Min.	Typ. ⁽²⁾	Max.	Units	Conditions		
SP70	FscP	Maximum SCK2 Input Frequency	_		Lesser of FP or 11	MHz	(Note 3)	
SP72	TscF	SCK2 Input Fall Time	—	_	—	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCK2 Input Rise Time	—	_	—	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO2 Data Output Fall Time	—		_	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO2 Data Output Rise Time	—		_	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30		—	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30		—	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30		—	ns		
SP50	TssL2scH, TssL2scL	SS2 ↓ to SCK2 ↑ or SCK2 ↓ Input	120		—	ns		
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	_	50	ns	(Note 4)	
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 TCY + 40	_	_	ns	(Note 4)	
SP60	TssL2doV	SDO2 Data Output Valid after SS2 Edge	—	-	50	ns		

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

FIGURE 30-23: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS



TABLE 30-42: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$				
Param.	Symbol	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP10	FscP	Maximum SCK1 Frequency	—		15	MHz	(Note 3)
SP20	TscF	SCK1 Output Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK1 Output Rise Time	—	—	_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdiV2scH, TdiV2scL	SDO1 Data Output Setup to First SCK1 Edge	30			ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

	30-37.									
АС СН	ARACTE	RISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)}^{(1)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$							
Param No.	Symbol	Characteristic	Min.	Conditions						
Device Supply										
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or 3.0	—	Lesser of: VDD + 0.3 or 3.6	V				
AD02	AVss	Module Vss Supply	Vss – 0.3	_	Vss + 0.3	V				
		·	Refer	ence In	puts					
AD05	Vrefh	Reference Voltage High	AVss + 2.5	—	AVdd	V	VREFH = VREF+ VREFL = VREF- (Note 1)			
AD05a			3.0	—	3.6	V	VREFH = AVDD VREFL = AVSS = 0			
AD06	VREFL	Reference Voltage Low	AVss	_	AVDD – 2.5	V	(Note 1)			
AD06a	-		0	—	0	V	VREFH = AVDD VREFL = AVSS = 0			
AD07	Vref	Absolute Reference Voltage	2.5	—	3.6	V	VREF = VREFH - VREFL			
AD08	IREF	Current Drain	_	_	10 600	μΑ μΑ	ADC off ADC on			
AD09	IAD	Operating Current ⁽²⁾	—	5	—	mA	ADC operating in 10-bit mode (Note 1)			
			—	2	—	mA	ADC operating in 12-bit mode (Note 1)			
			Ana	log Inp	out	•				
AD12	Vinh	Input Voltage Range Vinн	VINL	_	Vrefh	V	This voltage reflects Sample-and- Hold Channels 0, 1, 2 and 3 (CH0-CH3), positive input			
AD13	VINL	Input Voltage Range VINL	VREFL		AVss + 1V	V	This voltage reflects Sample-and- Hold Channels 0, 1, 2 and 3 (CH0-CH3), negative input			
AD17	Rin	Recommended Impedance of Analog Voltage Source	_		200	Ω	Impedance to achieve maximum performance of ADC			

TABLE 30-57: ADC MODULE SPECIFICATIONS

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: Parameter is characterized but not tested in manufacturing.

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS				
Dimension	n Limits	MIN	NOM	MAX		
Number of Pins	Ν	28				
Pitch	е	0.65 BSC				
Overall Height	Α	-	-	2.00		
Molded Package Thickness	A2	1.65	1.75	1.85		
Standoff	A1	0.05	-	-		
Overall Width	E	7.40	7.80	8.20		
Molded Package Width	E1	5.00	5.30	5.60		
Overall Length	D	9.90	10.20	10.50		
Foot Length	L	0.55	0.75	0.95		
Footprint		1.25 REF				
Lead Thickness	с	0.09	-	0.25		
Foot Angle	¢	0°	4°	8°		
Lead Width	b	0.22	_	0.38		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.

- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS					
Dimension	Limits	MIN	NOM	MAX		
Number of Pins	N	48				
Pitch	е	0.40 BSC				
Overall Height	Α	0.45 0.50 0.55				
Standoff	A1	0.00	0.02	0.05		
Contact Thickness	A3	0.127 REF				
Overall Width	E	6.00 BSC				
Exposed Pad Width	E2	4.45 4.60 4.7				
Overall Length	D	6.00 BSC				
Exposed Pad Length	D2	4.45	4.60	4.75		
Contact Width	b	0.15	0.20	0.25		
Contact Length	L	0.30	0.40	0.50		
Contact-to-Exposed Pad	K	0.20	-	_		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-153A Sheet 2 of 2