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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 60 MIPS |
| Connectivity | I ² C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 64KB (22K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 9x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VQFN Exposed Pad |
| Supplier Device Package | 44-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64mc204-e-ml |

2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICKit™ 3, MPLAB ICD 3, or MPLAB REAL ICE™.

For more information on MPLAB ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- "Using MPLAB® ICD 3" (poster) DS51765
- "MPLAB® ICD 3 Design Advisory" DS51764
- "MPLAB® REAL ICE™ In-Circuit Emulator User's Guide" DS51616
- "Using MPLAB® REAL ICE™ In-Circuit Emulator" (poster) DS51749

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency Primary Oscillator and a low-frequency Secondary Oscillator. For details, see **Section 9.0 "Oscillator Configuration"** for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

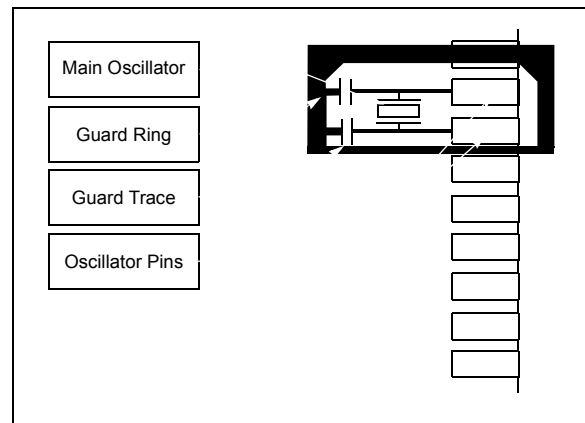


TABLE 4-52: PORTG REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|------------|
| TRISG | 0E60 | — | — | — | — | — | — | TRISG9 | TRISG8 | TRISG7 | TRISG6 | — | — | — | — | — | — | 03C0 |
| PORTG | 0E62 | — | — | — | — | — | — | RG9 | RG8 | RG7 | RG6 | — | — | — | — | — | — | xxxx |
| LATG | 0E64 | — | — | — | — | — | — | LATG9 | LATG8 | LATG7 | LATG6 | — | — | — | — | — | — | xxxx |
| ODCG | 0E66 | — | — | — | — | — | — | ODCG9 | ODCG8 | ODCG7 | ODCG6 | — | — | — | — | — | — | 0000 |
| CNENG | 0E68 | — | — | — | — | — | — | CNIEG9 | CNIEG8 | CNIEG7 | CNIEG6 | — | — | — | — | — | — | 0000 |
| CNPUG | 0E6A | — | — | — | — | — | — | CNPUG9 | CNPUG8 | CNPUG7 | CNPUG6 | — | — | — | — | — | — | 0000 |
| CNPDG | 0E6C | — | — | — | — | — | — | CNPDG9 | CNPDG8 | CNPDG7 | CNPDG6 | — | — | — | — | — | — | 0000 |

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

| | |
|-------|---|
| bit 3 | SLEEP: Wake-up from Sleep Flag bit 1 = Device has been in Sleep mode 0 = Device has not been in Sleep mode |
| bit 2 | IDLE: Wake-up from Idle Flag bit 1 = Device was in Idle mode 0 = Device was not in Idle mode |
| bit 1 | BOR: Brown-out Reset Flag bit 1 = A Brown-out Reset has occurred 0 = A Brown-out Reset has not occurred |
| bit 0 | POR: Power-on Reset Flag bit 1 = A Power-on Reset has occurred 0 = A Power-on Reset has not occurred |

- Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
- 2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

FIGURE 13-1: TYPE B TIMER BLOCK DIAGRAM (x = 2 AND 4)

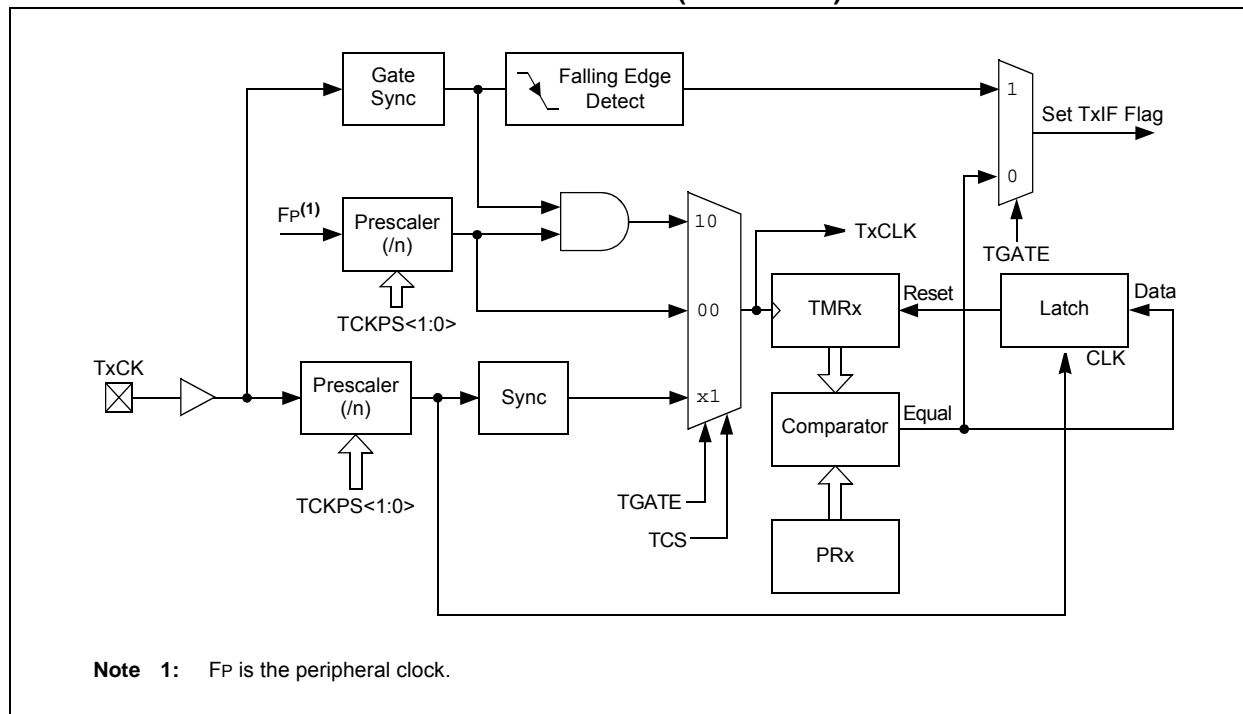
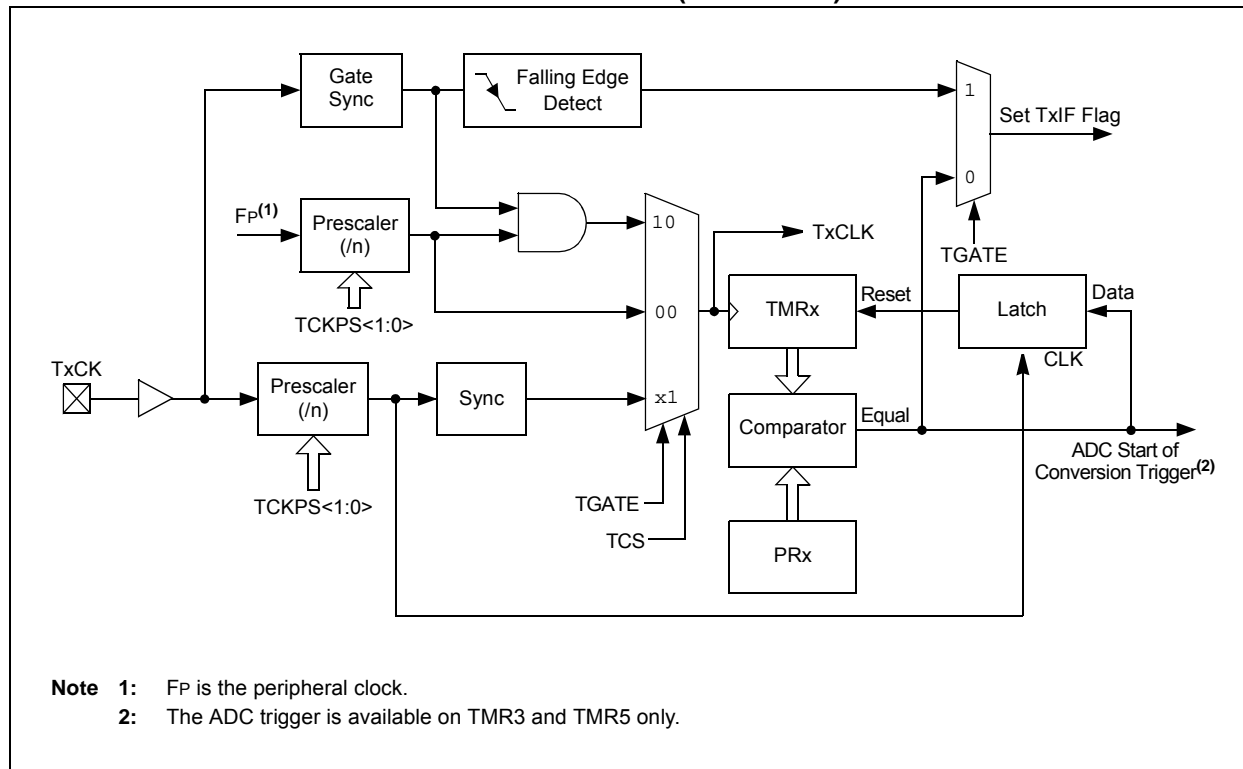


FIGURE 13-2: TYPE C TIMER BLOCK DIAGRAM (x = 3 AND 5)



REGISTER 16-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PDCx<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PDCx<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PDCx<15:0>**: PWMx Generator # Duty Cycle Value bits

REGISTER 16-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER

| | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PHASEx<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PHASEx<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PHASEx<15:0>**: PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

- Note 1:** If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation:
Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10),
PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs
- 2:** If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation:
Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10),
PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL

REGISTER 16-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER⁽¹⁾

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|----------------------|-------|
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | CLSRC4 | CLSRC3 | CLSRC2 | CLSRC1 | CLSRC0 | CLPOL ⁽²⁾ | CLMOD |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|---------|---------|---------|---------|---------|-----------------------|---------|---------|
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
| FLTSRC4 | FLTSRC3 | FLTSRC2 | FLTSRC1 | FLTSRC0 | FLTPOL ⁽²⁾ | FLTMOD1 | FLTMOD0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-10 **CLSRC<4:0>:** Current-Limit Control Signal Source Select for PWM Generator # bits

11111 = Fault 32
 11110 = Reserved
 .
 .
 .
 01100 = Reserved
 01011 = Comparator 4
 01010 = Op Amp/Comparator 3
 01001 = Op Amp/Comparator 2
 01000 = Op Amp/Comparator 1
 00111 = Reserved
 00110 = Reserved
 00101 = Reserved
 00100 = Reserved
 00011 = Fault 4
 00010 = Fault 3
 00001 = Fault 2
 00000 = Fault 1 (**default**)

bit 9 **CLPOL:** Current-Limit Polarity for PWM Generator # bit⁽²⁾

1 = The selected current-limit source is active-low
 0 = The selected current-limit source is active-high

bit 8 **CLMOD:** Current-Limit Mode Enable for PWM Generator # bit

1 = Current-Limit mode is enabled
 0 = Current-Limit mode is disabled

Note 1: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

2: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 17-15: QE1GECH: QE1 GREATER THAN OR EQUAL COMPARE HIGH WORD REGISTER

| | | | | | | | |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| QEIGEC<31:24> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| QEIGEC<23:16> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 15-0 **QEIGEC<31:16>**: High Word Used to Form 32-Bit Greater Than or Equal Compare Register (QE1GEC) bits

REGISTER 17-16: QE1GECL: QE1 GREATER THAN OR EQUAL COMPARE LOW WORD REGISTER

| | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| QEIGEC<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| QEIGEC<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 15-0 **QEIGEC<15:0>**: Low Word Used to Form 32-Bit Greater Than or Equal Compare Register (QE1GEC) bits

REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER

| | | | | | | | |
|--------|-----|------|------|------|-------|-------|-------|
| U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| — | — | TXBO | TXBP | RXBP | TXWAR | RXWAR | EWARN |
| bit 15 | | | | | | | |
| | | | | | | | |
| | | | | | | | bit 8 |

| | | | | | | | |
|-------|-------|-------|-----|--------|--------|-------|-------|
| R/C-0 | R/C-0 | R/C-0 | U-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
| IVRIF | WAKIF | ERRIF | — | FIFOIF | RBOVIF | RBIF | TBIF |
| bit 7 | | | | | | | |
| | | | | | | | |
| | | | | | | | bit 0 |

| | | | |
|-------------------|--|------------------------------------|--------------------|
| Legend: | C = Writable bit, but only '0' can be written to clear the bit | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

| | |
|-----------|--|
| bit 15-14 | Unimplemented: Read as '0' |
| bit 13 | TXBO: Transmitter in Error State Bus Off bit 1 = Transmitter is in Bus Off state 0 = Transmitter is not in Bus Off state |
| bit 12 | TXBP: Transmitter in Error State Bus Passive bit 1 = Transmitter is in Bus Passive state 0 = Transmitter is not in Bus Passive state |
| bit 11 | RXBP: Receiver in Error State Bus Passive bit 1 = Receiver is in Bus Passive state 0 = Receiver is not in Bus Passive state |
| bit 10 | TXWAR: Transmitter in Error State Warning bit 1 = Transmitter is in Error Warning state 0 = Transmitter is not in Error Warning state |
| bit 9 | RXWAR: Receiver in Error State Warning bit 1 = Receiver is in Error Warning state 0 = Receiver is not in Error Warning state |
| bit 8 | EWARN: Transmitter or Receiver in Error State Warning bit 1 = Transmitter or receiver is in Error Warning state 0 = Transmitter or receiver is not in Error Warning state |
| bit 7 | IVRIF: Invalid Message Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred |
| bit 6 | WAKIF: Bus Wake-up Activity Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred |
| bit 5 | ERRIF: Error Interrupt Flag bit (multiple sources in CxINTF<13:8>) 1 = Interrupt request has occurred 0 = Interrupt request has not occurred |
| bit 4 | Unimplemented: Read as '0' |
| bit 3 | FIFOIF: FIFO Almost Full Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred |
| bit 2 | RBOVIF: RX Buffer Overflow Interrupt Flag bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred |

REGISTER 23-5: AD1CHS123: ADC1 INPUT CHANNEL 1, 2, 3 SELECT REGISTER

| | | | | | | | |
|--------|-----|-----|-----|-----|----------|----------|---------|
| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | — | — | CH123NB1 | CH123NB0 | CH123SB |
| bit 15 | | | | | bit 8 | | |

| | | | | | | | |
|-------|-----|-----|-----|-----|----------|----------|---------|
| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | — | — | CH123NA1 | CH123NA0 | CH123SA |
| bit 7 | | | | | bit 0 | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-9 **CH123NB<1:0>:** Channel 1, 2, 3 Negative Input Select for Sample MUXB bits
In 12-bit mode (AD21B = 1), CH123NB is Unimplemented and is Read as '0':

| Value | ADC Channel | | |
|---------------------|-------------|-------|-------|
| | CH1 | CH2 | CH3 |
| 11 | AN9 | AN10 | AN11 |
| 10 ^(1,2) | OA3/AN6 | AN7 | AN8 |
| 0x | VREFL | VREFL | VREFL |

bit 8 **CH123SB:** Channel 1, 2, 3 Positive Input Select for Sample MUXB bit

In 12-bit mode (AD21B = 1), CH123SB is Unimplemented and is Read as '0':

| Value | ADC Channel | | |
|--------------------|-------------|---------|---------|
| | CH1 | CH2 | CH3 |
| 1 ⁽²⁾ | OA1/AN3 | OA2/AN0 | OA3/AN6 |
| 0 ^(1,2) | OA2/AN0 | AN1 | AN2 |

bit 7-3 **Unimplemented:** Read as '0'

bit 2-1 **CH123NA<1:0>:** Channel 1, 2, 3 Negative Input Select for Sample MUXA bits
In 12-bit mode (AD21B = 1), CH123NA is Unimplemented and is Read as '0':

| Value | ADC Channel | | |
|---------------------|-------------|-------|-------|
| | CH1 | CH2 | CH3 |
| 11 | AN9 | AN10 | AN11 |
| 10 ^(1,2) | OA3/AN6 | AN7 | AN8 |
| 0x | VREFL | VREFL | VREFL |

Note 1: AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)

bit 4-0 **CH0SA<4:0>**: Channel 0 Positive Input Select for Sample MUXA bits⁽¹⁾

11111 = Open; use this selection with CTMU capacitive and time measurement
11110 = Channel 0 positive input is connected to the CTMU temperature measurement diode (CTMU TEMP)
11101 = Reserved
11100 = Reserved
11011 = Reserved
11010 = Channel 0 positive input is the output of OA3/AN6^(2,3)
11001 = Channel 0 positive input is the output of OA2/AN0⁽²⁾
11000 = Channel 0 positive input is the output of OA1/AN3⁽²⁾
10110 = Reserved
•
•
•
10000 = Reserved
01111 = Channel 0 positive input is AN15^(1,3)
01110 = Channel 0 positive input is AN14^(1,3)
01101 = Channel 0 positive input is AN13^(1,3)
•
•
•
00010 = Channel 0 positive input is AN2^(1,3)
00001 = Channel 0 positive input is AN1^(1,3)
00000 = Channel 0 positive input is AN0^(1,3)

Note 1: AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

3: See the “Pin Diagrams” section for the available analog channels for each device.

24.3 PTG Control Registers

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER

| | | | | | | | |
|--------|-----|---------|---------|-----|-----------------------|------------------------|---------|
| R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| PTGEN | — | PTGSIDL | PTGTOGL | — | PTGSWT ⁽²⁾ | PTGSSEN ⁽³⁾ | PTGIVIS |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|---------|---------|-----|-----|-----|-----|------------------------|------------------------|
| R/W-0 | HS-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | |
| PTGSTRT | PTGWDTO | — | — | — | — | PTGITM1 ⁽¹⁾ | PTGITM0 ⁽¹⁾ |
| bit 7 | | | | | | | bit 0 |

| | | | |
|-------------------|----------------------------|------------------------------------|--------------------|
| Legend: | HS = Hardware Settable bit | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

- bit 15 **PTGEN:** Module Enable bit
1 = PTG module is enabled
0 = PTG module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **PTGSIDL:** PTG Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode
- bit 12 **PTGTOGL:** PTG TRIG Output Toggle Mode bit
1 = Toggle state of the PTGOx for each execution of the PTGTRIG command
0 = Each execution of the PTGTRIG command will generate a single PTGOx pulse determined by the value in the PTGPWDx bits
- bit 11 **Unimplemented:** Read as '0'
- bit 10 **PTGSWT:** PTG Software Trigger bit⁽²⁾
1 = Triggers the PTG module
0 = No action (clearing this bit will have no effect)
- bit 9 **PTGSSEN:** PTG Enable Single-Step bit⁽³⁾
1 = Enables Single-Step mode
0 = Disables Single-Step mode
- bit 8 **PTGIVIS:** PTG Counter/Timer Visibility Control bit
1 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the current values of their corresponding counter/timer registers (PTGSD, PTGCx, PTGTx)
0 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the value previously written to those limit registers
- bit 7 **PTGSTRT:** PTG Start Sequencer bit
1 = Starts to sequentially execute commands (Continuous mode)
0 = Stops executing commands
- bit 6 **PTGWDTO:** PTG Watchdog Timer Time-out Status bit
1 = PTG Watchdog Timer has timed out
0 = PTG Watchdog Timer has not timed out.
- bit 5-2 **Unimplemented:** Read as '0'

- Note 1:** These bits apply to the PTGWHI and PTGWLO commands only.
- Note 2:** This bit is only used with the PTGCTRL step command software trigger option.
- Note 3:** Use of the PTG Single-Step mode is reserved for debugging tools only.

REGISTER 24-4: PTGT0LIM: PTG TIMER0 LIMIT REGISTER⁽¹⁾

| | | | | | | | |
|----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PTGT0LIM<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PTGT0LIM<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PTGT0LIM<15:0>**: PTG Timer0 Limit Register bits
General Purpose Timer0 Limit register (effective only with a PTGT0 Step command).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-5: PTGT1LIM: PTG TIMER1 LIMIT REGISTER⁽¹⁾

| | | | | | | | |
|----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PTGT1LIM<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PTGT1LIM<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PTGT1LIM<15:0>**: PTG Timer1 Limit Register bits
General Purpose Timer1 Limit register (effective only with a PTGT1 Step command).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER (CONTINUED)

- bit 5 **Unimplemented:** Read as '0'
- bit 4 **CREF:** Comparator Reference Select bit (VIN+ input)⁽¹⁾
 1 = VIN+ input connects to internal CVREFIN voltage
 0 = VIN+ input connects to C4IN1+ pin
- bit 3-2 **Unimplemented:** Read as '0'
- bit 1-0 **CCH<1:0>:** Comparator Channel Select bits⁽¹⁾
 11 = VIN- input of comparator connects to OA3/AN6
 10 = VIN- input of comparator connects to OA2/AN0
 01 = VIN- input of comparator connects to OA1/AN3
 00 = VIN- input of comparator connects to C4IN1-

Note 1: Inputs that are selected and not available will be tied to Vss. See the “Pin Diagrams” section for available inputs for each package.

TABLE 27-2: CONFIGURATION BITS DESCRIPTION

| Bit Field | Description |
|------------------------|---|
| GCP | General Segment Code-Protect bit 1 = User program memory is not code-protected 0 = Code protection is enabled for the entire program memory space |
| GWRP | General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected |
| IESO | Two-Speed Oscillator Start-up Enable bit 1 = Start up device with FRC, then automatically switch to the user-selected oscillator source when ready 0 = Start up device with user-selected oscillator source |
| PWMLOCK ⁽¹⁾ | PWM Lock Enable bit 1 = Certain PWM registers may only be written after a key sequence 0 = PWM registers may be written without a key sequence |
| FNOSC<2:0> | Oscillator Selection bits 111 = Fast RC Oscillator with Divide-by-N (FRCDIVN) 110 = Fast RC Oscillator with Divide-by-16 (FRCDIV16) 101 = Low-Power RC Oscillator (LPRC) 100 = Reserved; do not use 011 = Primary Oscillator with PLL module (XT + PLL, HS + PLL, EC + PLL) 010 = Primary Oscillator (XT, HS, EC) 001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCPLL) 000 = Fast RC Oscillator (FRC) |
| FCKSM<1:0> | Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled |
| IOL1WAY | Peripheral Pin Select Configuration bit 1 = Allow only one reconfiguration 0 = Allow multiple reconfigurations |
| OSCIOFNC | OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is a general purpose digital I/O pin |
| POSCMD<1:0> | Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode |
| FWDTEN | Watchdog Timer Enable bit 1 = Watchdog Timer is always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.) 0 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register) |
| WINDIS | Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode |
| PLLKEN | PLL Lock Enable bit 1 = PLL lock is enabled 0 = PLL lock is disabled |

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

2: When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSBs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed, or an SFR register is read. In these cases, the execution takes multiple instruction cycles with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either

two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Note: For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

For more information on instructions that take more than one instruction cycle to execute, refer to **"CPU"** (DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*, particularly the **"Instruction Flow Types"** section.

TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

| Field | Description |
|---------------------|---|
| #text | Means literal defined by "text" |
| (text) | Means "content of text" |
| [text] | Means "the location addressed by text" |
| { } | Optional field or operation |
| $a \in \{b, c, d\}$ | a is selected from the set of values b, c, d |
| <n:m> | Register bit field |
| .b | Byte mode selection |
| .d | Double-Word mode selection |
| .S | Shadow register select |
| .w | Word mode selection (default) |
| Acc | One of two accumulators {A, B} |
| AWB | Accumulator write back destination address register $\in \{W13, [W13]+ = 2\}$ |
| bit4 | 4-bit bit selection field (used in word addressed instructions) $\in \{0...15\}$ |
| C, DC, N, OV, Z | MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero |
| Expr | Absolute address, label or expression (resolved by the linker) |
| f | File register address $\in \{0x0000...0x1FFF\}$ |
| lit1 | 1-bit unsigned literal $\in \{0,1\}$ |
| lit4 | 4-bit unsigned literal $\in \{0...15\}$ |
| lit5 | 5-bit unsigned literal $\in \{0...31\}$ |
| lit8 | 8-bit unsigned literal $\in \{0...255\}$ |
| lit10 | 10-bit unsigned literal $\in \{0...255\}$ for Byte mode, $\{0:1023\}$ for Word mode |
| lit14 | 14-bit unsigned literal $\in \{0...16384\}$ |
| lit16 | 16-bit unsigned literal $\in \{0...65535\}$ |
| lit23 | 23-bit unsigned literal $\in \{0...8388608\}$; LSb must be '0' |
| None | Field does not require an entry, can be blank |
| OA, OB, SA, SB | DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate |
| PC | Program Counter |
| Slit10 | 10-bit signed literal $\in \{-512...511\}$ |
| Slit16 | 16-bit signed literal $\in \{-32768...32767\}$ |
| Slit6 | 6-bit signed literal $\in \{-16...16\}$ |
| Wb | Base W register $\in \{W0...W15\}$ |
| Wd | Destination W register $\in \{Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd]\}$ |
| Wdo | Destination W register $\in \{Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb]\}$ |

TABLE 30-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | |
|--|------|------|--|------------|------|---------|
| Parameter No. | Typ. | Max. | Units | Conditions | | |
| Operating Current (IDD) ⁽¹⁾ | | | | | | |
| DC20d | 9 | 15 | mA | -40°C | 3.3V | 10 MIPS |
| DC20a | 9 | 15 | mA | +25°C | | |
| DC20b | 9 | 15 | mA | +85°C | | |
| DC20c | 9 | 15 | mA | +125°C | | |
| DC22d | 16 | 25 | mA | -40°C | 3.3V | 20 MIPS |
| DC22a | 16 | 25 | mA | +25°C | | |
| DC22b | 16 | 25 | mA | +85°C | | |
| DC22c | 16 | 25 | mA | +125°C | | |
| DC24d | 27 | 40 | mA | -40°C | 3.3V | 40 MIPS |
| DC24a | 27 | 40 | mA | +25°C | | |
| DC24b | 27 | 40 | mA | +85°C | | |
| DC24c | 27 | 40 | mA | +125°C | | |
| DC25d | 36 | 55 | mA | -40°C | 3.3V | 60 MIPS |
| DC25a | 36 | 55 | mA | +25°C | | |
| DC25b | 36 | 55 | mA | +85°C | | |
| DC25c | 36 | 55 | mA | +125°C | | |
| DC26d | 41 | 60 | mA | -40°C | 3.3V | 70 MIPS |
| DC26a | 41 | 60 | mA | +25°C | | |
| DC26b | 41 | 60 | mA | +85°C | | |

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLK0 is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}} = \text{VDD}$, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- CPU is executing `while(1){NOP();}` statement
- JTAG is disabled

TABLE 30-58: ADC MODULE SPECIFICATIONS (12-BIT MODE)

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽¹⁾ Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|-----------------------------------|--------|---|--|------|------|-------|------------------------------|
| Param No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Conditions |
| ADC Accuracy (12-Bit Mode) | | | | | | | |
| AD20a | Nr | Resolution | 12 Data Bits | | | bits | |
| AD21a | INL | Integral Nonlinearity | -2.5 | — | 2.5 | LSb | -40°C ≤ TA ≤ +85°C (Note 2) |
| | | | -5.5 | — | 5.5 | LSb | +85°C < TA ≤ +125°C (Note 2) |
| AD22a | DNL | Differential Nonlinearity | -1 | — | 1 | LSb | -40°C ≤ TA ≤ +85°C (Note 2) |
| | | | -1 | — | 1 | LSb | +85°C < TA ≤ +125°C (Note 2) |
| AD23a | GERR | Gain Error ⁽³⁾ | -10 | — | 10 | LSb | -40°C ≤ TA ≤ +85°C (Note 2) |
| | | | -10 | — | 10 | LSb | +85°C < TA ≤ +125°C (Note 2) |
| AD24a | EOFF | Offset Error | -5 | — | 5 | LSb | -40°C ≤ TA ≤ +85°C (Note 2) |
| | | | -5 | — | 5 | LSb | +85°C < TA ≤ +125°C (Note 2) |
| AD25a | — | Monotonicity | — | — | — | — | Guaranteed |
| Dynamic Performance (12-Bit Mode) | | | | | | | |
| AD30a | THD | Total Harmonic Distortion ⁽³⁾ | — | 75 | — | dB | |
| AD31a | SINAD | Signal to Noise and Distortion ⁽³⁾ | — | 68 | — | dB | |
| AD32a | SFDR | Spurious Free Dynamic Range ⁽³⁾ | — | 80 | — | dB | |
| AD33a | FNYQ | Input Signal Bandwidth ⁽³⁾ | — | 250 | — | kHz | |
| AD34a | ENOB | Effective Number of Bits ⁽³⁾ | 11.09 | 11.3 | — | bits | |

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

3: Parameters are characterized but not tested in manufacturing.

FIGURE 32-5: TYPICAL I_{PD} CURRENT @ $V_{DD} = 3.3V$

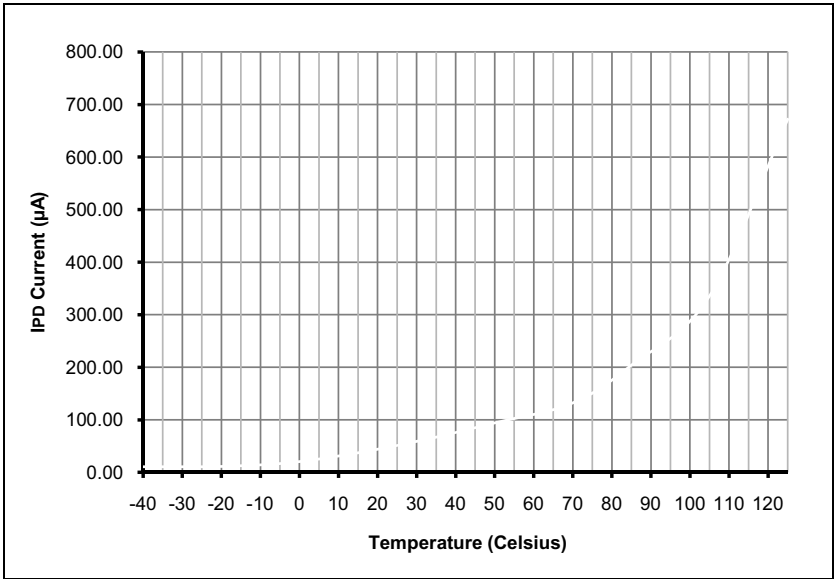


FIGURE 32-6: TYPICAL/MAXIMUM I_{DD} CURRENT @ $V_{DD} = 3.3V$

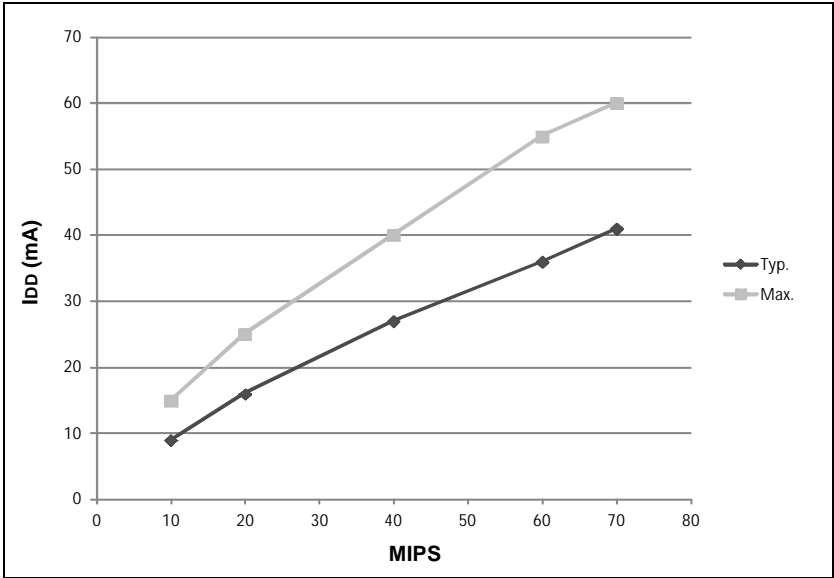


FIGURE 32-7: TYPICAL I_{DOZE} CURRENT @ $V_{DD} = 3.3V$

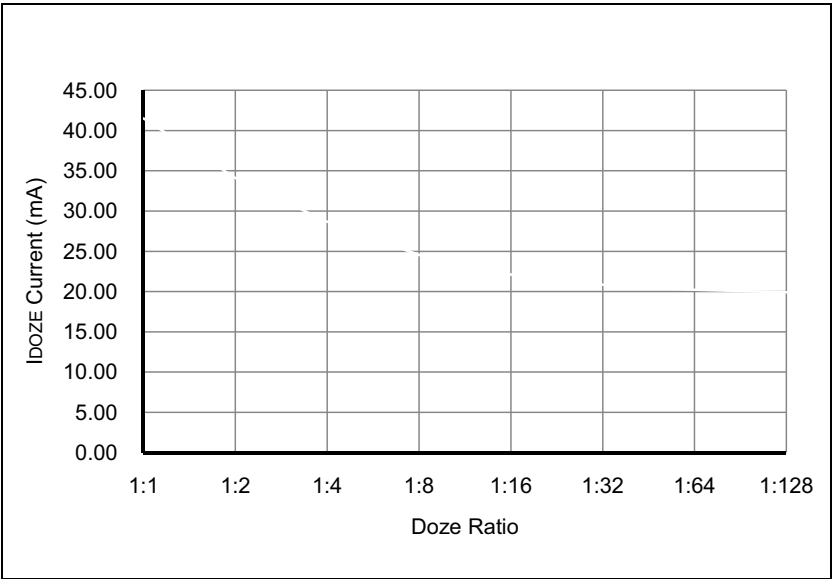
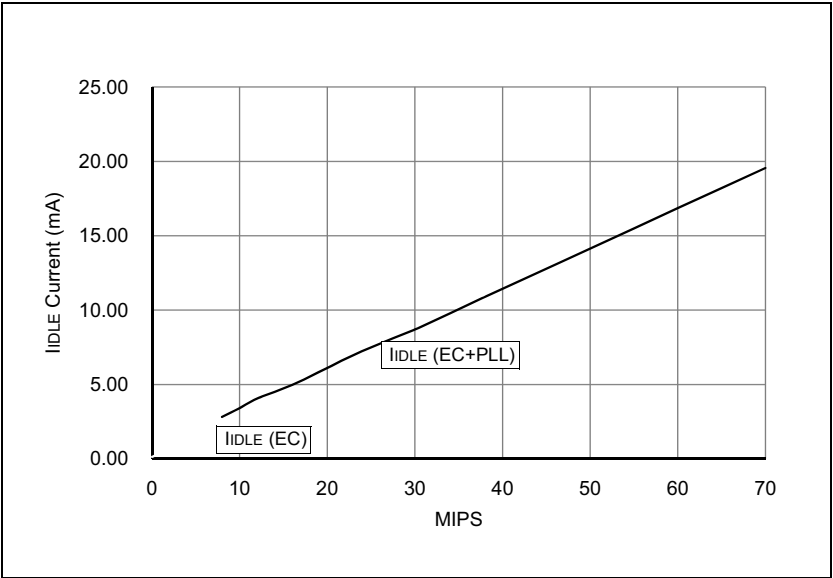
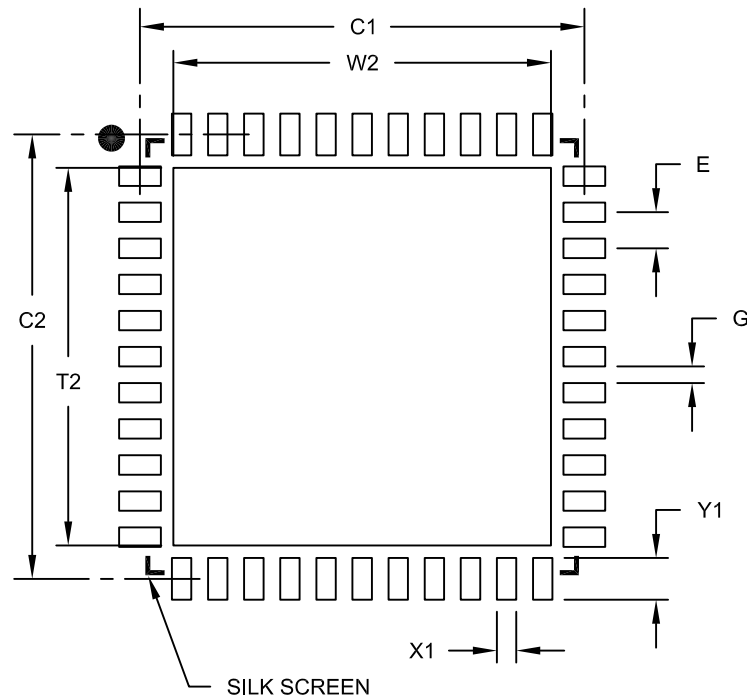


FIGURE 32-8: TYPICAL I_{IDLE} CURRENT @ $V_{DD} = 3.3V$



44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|----------------------------|----|-------------|------|------|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Optional Center Pad Width | W2 | | | 6.60 |
| Optional Center Pad Length | T2 | | | 6.60 |
| Contact Pad Spacing | C1 | | 8.00 | |
| Contact Pad Spacing | C2 | | 8.00 | |
| Contact Pad Width (X44) | X1 | | | 0.35 |
| Contact Pad Length (Y44) | Y1 | | | 0.85 |
| Distance Between Pads | G | 0.25 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B

NOTES: