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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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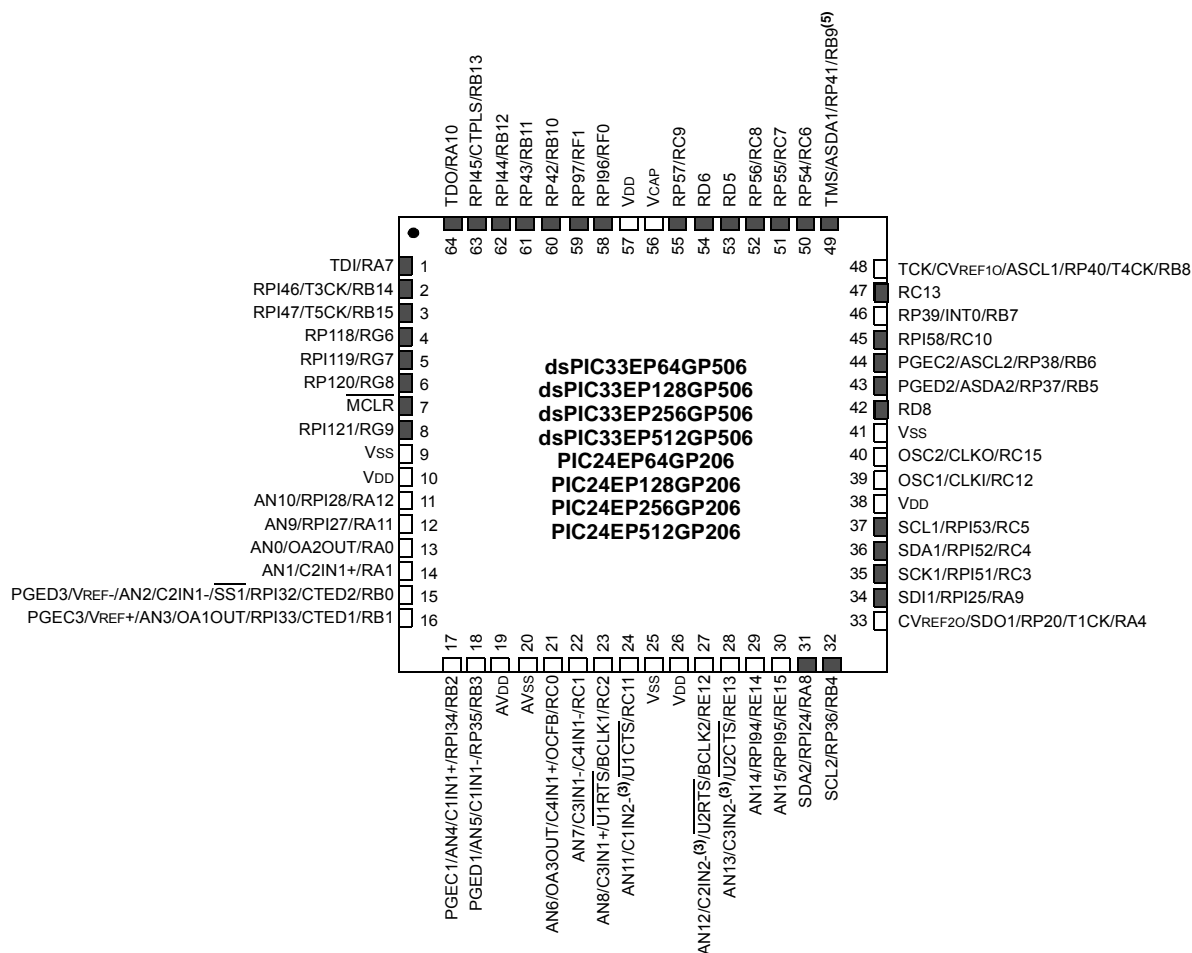
Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 60 MIPS |
| Connectivity | I ² C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 64KB (22K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 9x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-UQFN Exposed Pad |
| Supplier Device Package | 48-UQFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64mc204-e-mv |

Pin Diagrams (Continued)

64-Pin QFN^(1,2,3,4)

■ = Pins are up to 5V tolerant

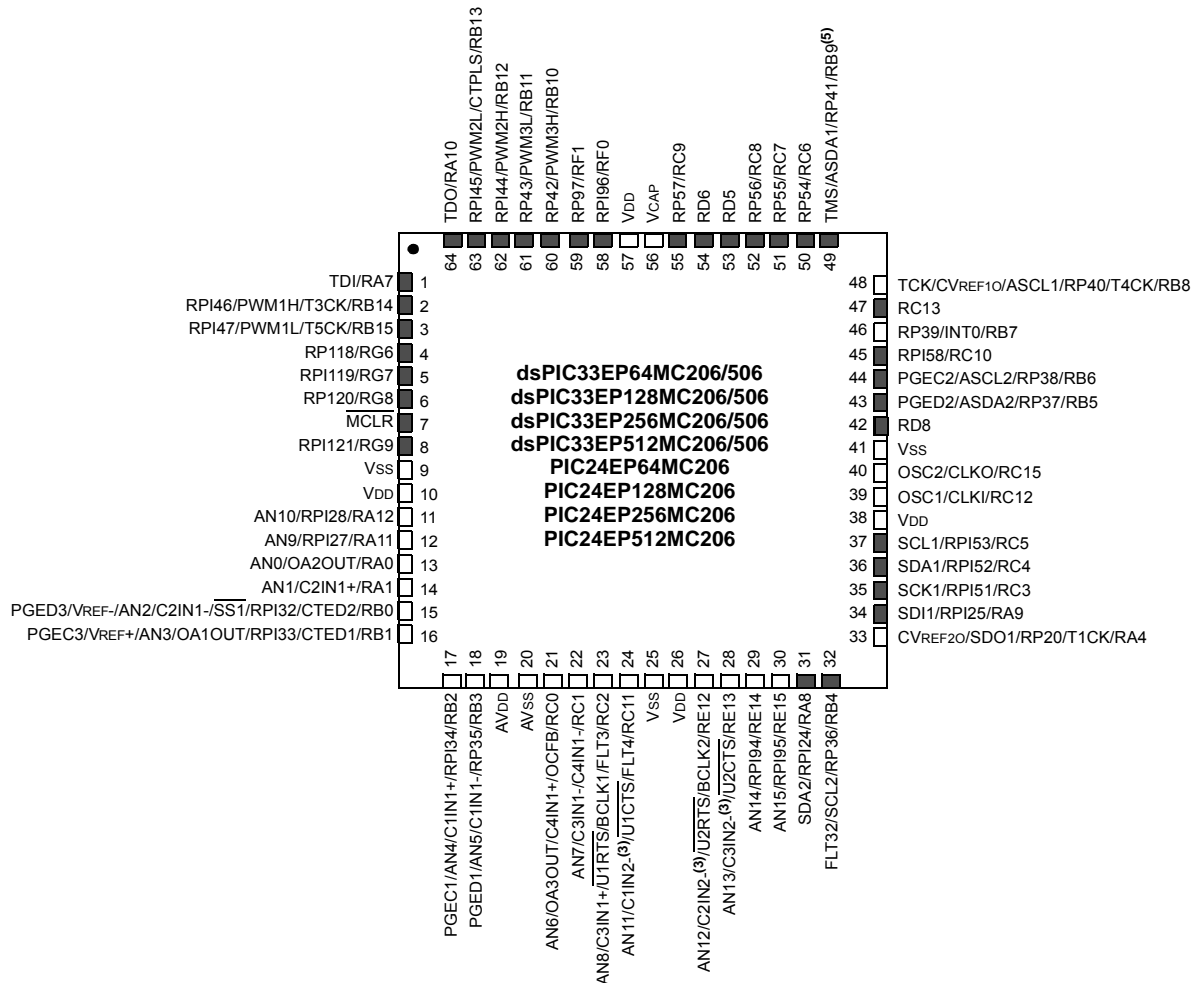


- Note 1:** The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** This pin is not available as an input when OPMODE (CMxCON<10>) = 1.
- Note 4:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
- Note 5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

Pin Diagrams (Continued)

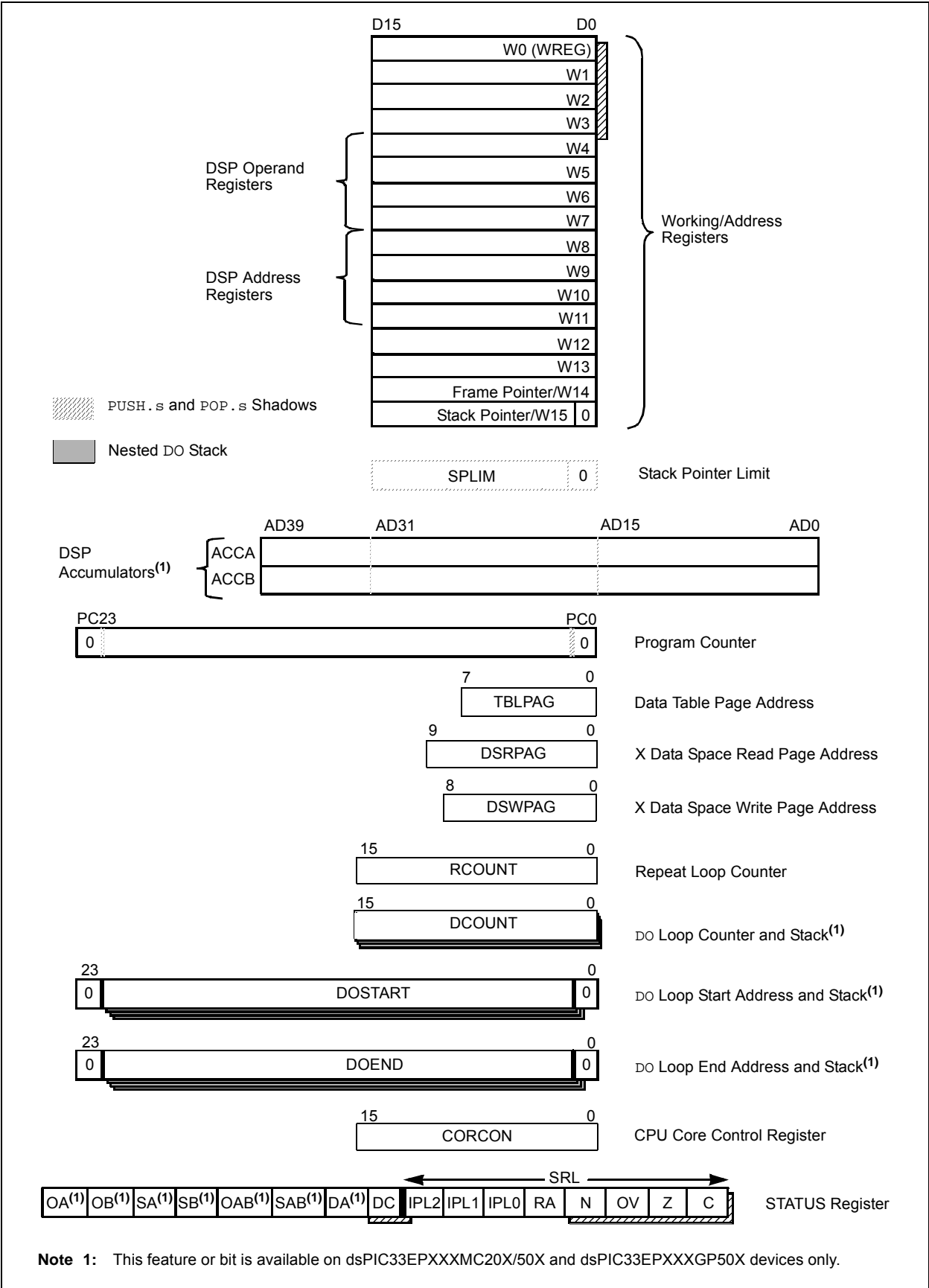
64-Pin QFN^(1,2,3,4)

■ = Pins are up to 5V tolerant



- Note**
- 1: The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
 - 3: This pin is not available as an input when OPMODE (CMXCON<10>) = 1.
 - 4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
 - 5: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

FIGURE 3-2: PROGRAMMER'S MODEL



3.6 CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|--------------|---|
| Note: | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |
|--------------|---|

3.6.1 KEY RESOURCES

- “**CPU**” (DS70359) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-------|--------|-------------|--------|--------|--------|--------------|---------|--------|-------|----------------|--------|--------|--------|--------------|-----------|---------|------------|
| IFS0 | 0800 | — | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | — | — | — | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | — | — | — | — | — | — | — | — | — | IC4IF | IC3IF | DMA3IF | C1IF | C1RXIF | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | — | — | — | — | — | — | — | — | — | — | — | — | — | MI2C2IF | SI2C2IF | — | 0000 |
| IFS4 | 0808 | — | — | CTMUIF | — | — | — | — | — | — | C1TXIF | — | — | CRCIF | U2EIF | U1EIF | — | 0000 |
| IFS6 | 080C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IF | 0000 |
| IFS8 | 0810 | JTAGIF | ICDIF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS9 | 0812 | — | — | — | — | — | — | — | — | — | PTG3IF | PTG2IF | PTG1IF | PTG0IF | PTGWDTIF | PTGSTIEIF | — | 0000 |
| IEC0 | 0820 | — | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | — | — | — | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | — | — | — | — | — | — | — | — | — | IC4IE | IC3IE | DMA3IE | C1IE | C1RXIE | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | — | — | — | — | — | — | — | — | — | — | — | — | — | MI2C2IE | SI2C2IE | — | 0000 |
| IEC4 | 0828 | — | — | CTMUIE | — | — | — | — | — | — | C1TXIE | — | — | CRCIE | U2EIE | U1EIE | — | 0000 |
| IEC8 | 0830 | JTAGIE | ICDIE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC9 | 0832 | — | — | — | — | — | — | — | — | — | PTG3IE | PTG2IE | PTG1IE | PTG0IE | PTGWDTIE | PTGSTIEIE | — | 0000 |
| IPC0 | 0840 | — | T1IP<2:0> | | | — | OC1IP<2:0> | | | — | IC1IP<2:0> | | | — | INT0IP<2:0> | | | 4444 |
| IPC1 | 0842 | — | T2IP<2:0> | | | — | OC2IP<2:0> | | | — | IC2IP<2:0> | | | — | DMA0IP<2:0> | | | 4444 |
| IPC2 | 0844 | — | U1RXIP<2:0> | | | — | SPI1IP<2:0> | | | — | SPI1EIP<2:0> | | | — | T3IP<2:0> | | | 4444 |
| IPC3 | 0846 | — | — | — | — | — | DMA1IP<2:0> | | | — | AD1IP<2:0> | | | — | U1TXIP<2:0> | | | 0444 |
| IPC4 | 0848 | — | CNIP<2:0> | | | — | CMIP<2:0> | | | — | MI2C1IP<2:0> | | | — | SI2C1IP<2:0> | | | 4444 |
| IPC5 | 084A | — | — | — | — | — | — | — | — | — | — | — | — | — | INT1IP<2:0> | | | 0004 |
| IPC6 | 084C | — | T4IP<2:0> | | | — | OC4IP<2:0> | | | — | OC3IP<2:0> | | | — | DMA2IP<2:0> | | | 4444 |
| IPC7 | 084E | — | U2TXIP<2:0> | | | — | U2RXIP<2:0> | | | — | INT2IP<2:0> | | | — | T5IP<2:0> | | | 4444 |
| IPC8 | 0850 | — | C1IP<2:0> | | | — | C1RXIP<2:0> | | | — | SPI2IP<2:0> | | | — | SPI2EIP<2:0> | | | 4444 |
| IPC9 | 0852 | — | — | — | — | — | IC4IP<2:0> | | | — | IC3IP<2:0> | | | — | DMA3IP<2:0> | | | 0444 |
| IPC11 | 0856 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IPC12 | 0858 | — | — | — | — | — | MI2C2IP<2:0> | | | — | SI2C2IP<2:0> | | | — | — | — | — | 0440 |
| IPC16 | 0860 | — | CRCIP<2:0> | | | — | U2EIP<2:0> | | | — | U1EIP<2:0> | | | — | — | — | — | 4440 |
| IPC17 | 0862 | — | — | — | — | — | C1TXIP<2:0> | | | — | — | — | — | — | — | — | — | 0400 |
| IPC19 | 0866 | — | — | — | — | — | — | — | — | — | CTMUIP<2:0> | | | — | — | — | — | 0040 |
| IPC35 | 0886 | — | JTAGIP<2:0> | | | — | ICDIP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC36 | 0888 | — | PTG0IP<2:0> | | | — | PTGWDIP<2:0> | | | — | PTGSTIEIP<2:0> | | | — | — | — | — | 4440 |
| IPC37 | 088A | — | — | — | — | — | PTG3IP<2:0> | | | — | PTG2IP<2:0> | | | — | PTG1IP<2:0> | | | 0444 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.2 EXTENDED X DATA SPACE

The lower portion of the base address space range, between 0x0000 and 0x7FFF, is always accessible regardless of the contents of the Data Space Page registers. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x007FFF with the base address bit, EA<15> = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF, of base Data Space, in combination with DSRPAG = 0x000 or DSWPAG = 0x000. Consequently, DSRPAG and DSWPAG are initialized to 0x001 at Reset.

Note 1: DSxPAG should not be used to access Page 0. An EDS access with DSxPAG set to 0x000 will generate an address error trap.

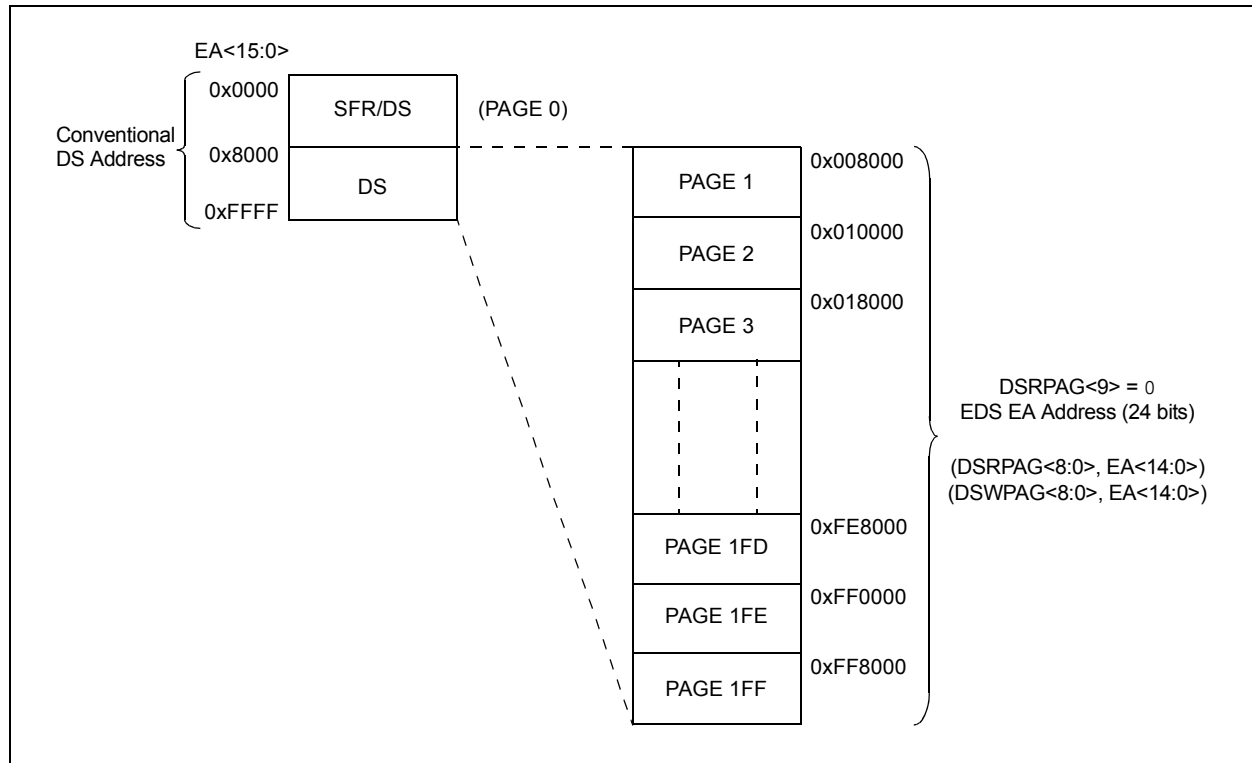
2: Clearing the DSxPAG in software has no effect.

The remaining pages, including both EDS and PSV pages, are only accessible using the DSRPAG or DSWPAG registers in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where base address bit, EA<15> = 1.

For example, when DSRPAG = 0x001 or DSWPAG = 0x001, accesses to the upper 32 Kbytes, 0x8000 to 0xFFFF, of the Data Space will map to the EDS address range of 0x008000 to 0x00FFFF. When DSRPAG = 0x002 or DSWPAG = 0x002, accesses to the upper 32 Kbytes of the Data Space will map to the EDS address range of 0x010000 to 0x017FFF and so on, as shown in the EDS memory map in Figure 4-17.

For more information on the PSV page access using Data Space Page registers, refer to the “**Program Space Visibility from Data Space**” section in “**Program Memory**” (DS70613) of the “*dsPIC33/PIC24 Family Reference Manual*”.

FIGURE 4-17: EDS MEMORY MAP



7.3 Interrupt Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

7.3.1 KEY RESOURCES

- “**Interrupts**” (DS70600) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

7.4 Interrupt Control and Status Registers

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON3
- INTCON4
- INTTREG

7.4.1 INTCON1 THROUGH INTCON4

Global interrupt control functions are controlled from INTCON1, INTCON2, INTCON3 and INTCON4.

INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS), as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior and also contains the Global Interrupt Enable bit (GIE).

INTCON3 contains the status flags for the DMA and DO stack overflow status trap sources.

The INTCON4 register contains the software generated hard trap status bit (SGHT).

7.4.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

7.4.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

7.4.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

7.4.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number bits (VECNUM<7:0>) and Interrupt Priority Level bits (ILR<3:0>) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 7-1. For example, the INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0> and the INT0IP bits in the first position of IPC0 (IPC0<2:0>).

7.4.6 STATUS/CONTROL REGISTERS

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers refer to “**CPU**” (DS70359) in the “*dsPIC33/PIC24 Family Reference Manual*”.

- The CPU STATUS Register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.
- The CORCON register contains the IPL3 bit which, together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-3 through Register 7-7 in the following pages.

13.0 TIMER2/3 AND TIMER4/5

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Timers**” (DS70362) of the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

- 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (32-bit timer pairs, and Timer3 and Timer5 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, and T4CON, T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. T3CON and T5CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsb); Timer3 and Timer5 are the most significant word (msb) of the 32-bit timers.

Note: For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

Note: Only Timer2, 3, 4 and 5 can trigger a DMA data transfer.

REGISTER 16-3: PTPER: PWM_x PRIMARY MASTER TIME BASE PERIOD REGISTER

| | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| PTPER<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
| PTPER<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PTPER<15:0>**: Primary Master Time Base (PMTMR) Period Value bits**REGISTER 16-4: SEVTCMP: PWM_x PRIMARY SPECIAL EVENT COMPARE REGISTER**

| | | | | | | | |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SEVTCMP<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| SEVTCMP<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **SEVTCMP<15:0>**: Special Event Compare Count Value bits

REGISTER 16-12: TRGCONx: PWMx TRIGGER CONTROL REGISTER

| | | | | | | | |
|-------------|-------|-------|-------|-------|-----|-----|-----|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
| TRGDIV<3:0> | | | | — | — | — | — |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|-------|-----|-----------------------------|-------|-------|-------|-------|-------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | TRGSTRT<5:0> ⁽¹⁾ | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **TRGDIV<3:0>**: Trigger # Output Divider bits

1111 = Trigger output for every 16th trigger event
 1110 = Trigger output for every 15th trigger event
 1101 = Trigger output for every 14th trigger event
 1100 = Trigger output for every 13th trigger event
 1011 = Trigger output for every 12th trigger event
 1010 = Trigger output for every 11th trigger event
 1001 = Trigger output for every 10th trigger event
 1000 = Trigger output for every 9th trigger event
 0111 = Trigger output for every 8th trigger event
 0110 = Trigger output for every 7th trigger event
 0101 = Trigger output for every 6th trigger event
 0100 = Trigger output for every 5th trigger event
 0011 = Trigger output for every 4th trigger event
 0010 = Trigger output for every 3rd trigger event
 0001 = Trigger output for every 2nd trigger event
 0000 = Trigger output for every trigger event

bit 11-6 **Unimplemented**: Read as '0'

bit 5-0 **TRGSTRT<5:0>**: Trigger Postscaler Start Enable Select bits⁽¹⁾

111111 = Waits 63 PWM cycles before generating the first trigger event after the module is enabled
 •
 •
 •
 000010 = Waits 2 PWM cycles before generating the first trigger event after the module is enabled
 000001 = Waits 1 PWM cycle before generating the first trigger event after the module is enabled
 000000 = Waits 0 PWM cycles before generating the first trigger event after the module is enabled

Note 1: The secondary PWM generator cannot generate PWMx trigger interrupts.

REGISTER 17-10: INDX1HLD: INDEX COUNTER 1 HOLD REGISTER

| | | | | | | | |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| INDXHLD<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| INDXHLD<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **INDXHLD<15:0>**: Hold Register for Reading and Writing INDX1CNTH bits

REGISTER 17-11: QE1ICH: QE1 INITIALIZATION/CAPTURE HIGH WORD REGISTER

| | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| QE1IC<31:24> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| QE1IC<23:16> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **QE1IC<31:16>**: High Word Used to Form 32-Bit Initialization/Capture Register (QE1IC) bits

REGISTER 17-12: QE1ICL: QE1 INITIALIZATION/CAPTURE LOW WORD REGISTER

| | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| QE1IC<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| QE1IC<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **QE1IC<15:0>**: Low Word Used to Form 32-Bit Initialization/Capture Register (QE1IC) bits

18.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
 - a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on \overline{SSx} .
 - b) If FRMPOL = 0, use a pull-up resistor on \overline{SSx} .

Note: This insures that the first frame transmission after initialization is not shifted or corrupted.

2. In Non-Framed 3-Wire mode, (i.e., not using \overline{SSx} from a master):
 - a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on \overline{SSx} .
 - b) If CKP = 0, always place a pull-down resistor on \overline{SSx} .

Note: This will insure that during power-up and initialization the master/slave will not lose Sync due to an errant SCKx transition that would cause the slave to accumulate data shift errors for both transmit and receive appearing as corrupted data.

3. FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the \overline{SSx} pin, which indicates the start of a data frame.

Note: Not all third-party devices support Frame mode timing. Refer to the SPIx specifications in **Section 30.0 “Electrical Characteristics”** for details.

4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a ‘1’ for the fastest SPIx data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user’s master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

18.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

18.2.1 KEY RESOURCES

- “**Serial Peripheral Interface (SPI)**” (DS70569) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

REGISTER 21-19: CxFMSKSEL2: ECANx FILTER 15-8 MASK SELECTION REGISTER 2

| | | | | | | | |
|-------------|-------|-------------|-------|-------------|-------|-------------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| F15MSK<1:0> | | F14MSK<1:0> | | F13MSK<1:0> | | F12MSK<1:0> | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | | |
|-------------|-------|-------------|-------|------------|-------|------------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | |
| F11MSK<1:0> | | F10MSK<1:0> | | F9MSK<1:0> | | F8MSK<1:0> | | |
| bit 7 | | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **F15MSK<1:0>**: Mask Source for Filter 15 bits
 11 = Reserved
 10 = Acceptance Mask 2 registers contain mask
 01 = Acceptance Mask 1 registers contain mask
 00 = Acceptance Mask 0 registers contain mask
- bit 13-12 **F14MSK<1:0>**: Mask Source for Filter 14 bits (same values as bits<15:14>)
- bit 11-10 **F13MSK<1:0>**: Mask Source for Filter 13 bits (same values as bits<15:14>)
- bit 9-8 **F12MSK<1:0>**: Mask Source for Filter 12 bits (same values as bits<15:14>)
- bit 7-6 **F11MSK<1:0>**: Mask Source for Filter 11 bits (same values as bits<15:14>)
- bit 5-4 **F10MSK<1:0>**: Mask Source for Filter 10 bits (same values as bits<15:14>)
- bit 3-2 **F9MSK<1:0>**: Mask Source for Filter 9 bits (same values as bits<15:14>)
- bit 1-0 **F8MSK<1:0>**: Mask Source for Filter 8 bits (same values as bits<15:14>)

REGISTER 21-20: CxRXMnSID: ECANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER REGISTER (n = 0-2)

| | | | | | | | |
|--------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-------|-------|-------|-----|-------|-----|-------|-------|
| R/W-x | R/W-x | R/W-x | U-0 | R/W-x | U-0 | R/W-x | R/W-x |
| SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-5 **SID<10:0>**: Standard Identifier bits
1 = Includes bit, SIDx, in filter comparison
0 = SIDx bit is a don't care in filter comparison
- bit 4 **Unimplemented**: Read as '0'
- bit 3 **MIDE**: Identifier Receive Mode bit
1 = Matches only message types (standard or extended address) that correspond to EXIDE bit in the filter
0 = Matches either standard or extended address message if filters match (i.e., if (Filter SID) = (Message SID) or if (Filter SID/EID) = (Message SID/EID))
- bit 2 **Unimplemented**: Read as '0'
- bit 1-0 **EID<17:16>**: Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = EIDx bit is a don't care in filter comparison

REGISTER 21-21: CxRXMnEID: ECANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER (n = 0-2)

| | | | | | | | |
|--------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| EID15 | EID14 | EID13 | EID12 | EID11 | EID10 | EID9 | EID8 |
| bit 15 | | | | | | bit 8 | |

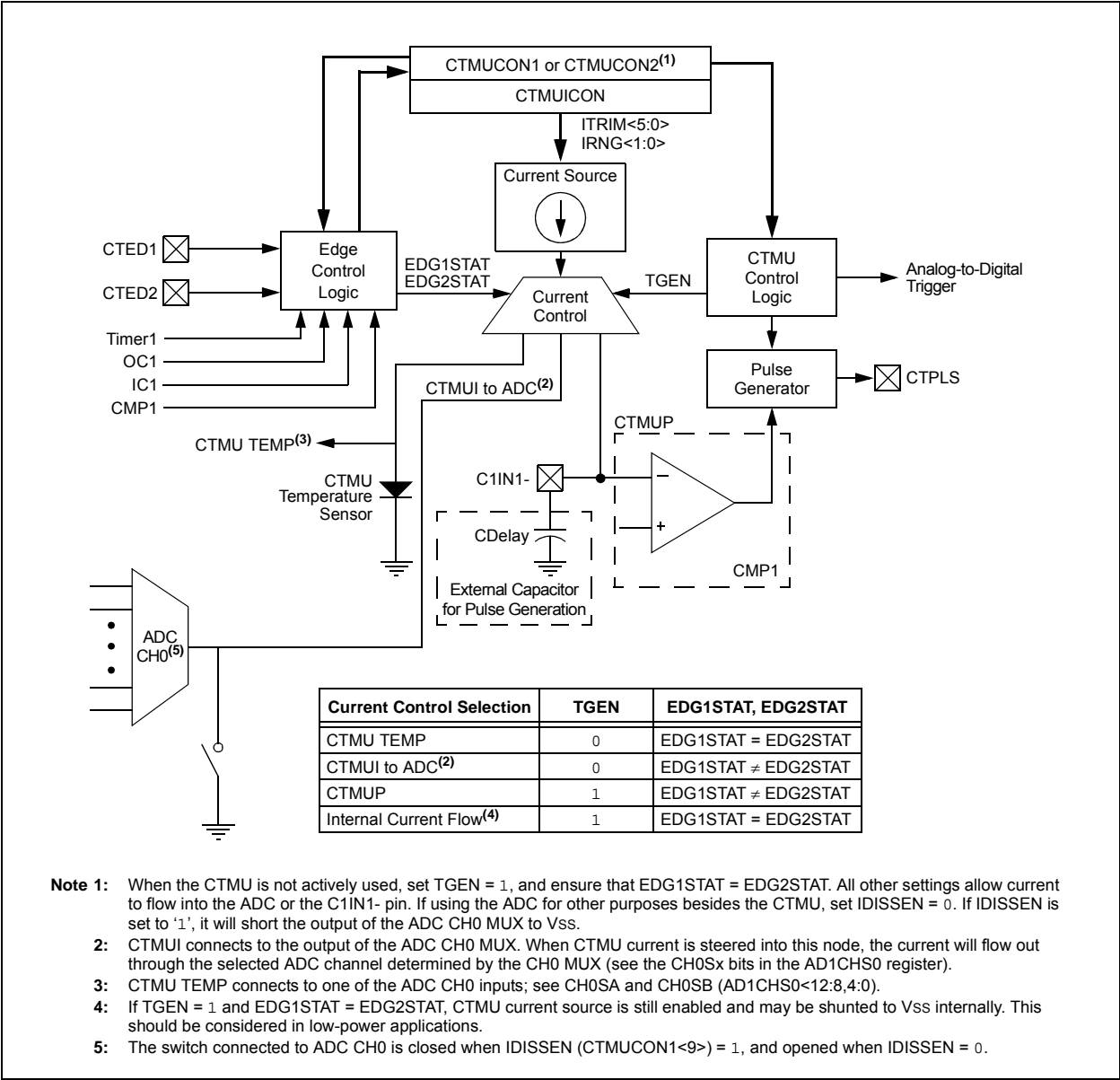
| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-0 **EID<15:0>**: Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = EIDx bit is a don't care in filter comparison

FIGURE 22-1: CTMU BLOCK DIAGRAM



22.1 CTMU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

22.1.1 KEY RESOURCES

- “Charge Time Measurement Unit (CTMU)” (DS70661) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools

24.3 PTG Control Registers

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER

| | | | | | | | |
|--------|-----|---------|---------|-----|-----------------------|------------------------|---------|
| R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| PTGEN | — | PTGSIDL | PTGTOGL | — | PTGSWT ⁽²⁾ | PTGSSEN ⁽³⁾ | PTGIVIS |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|---------|---------|-----|-----|-----|-----|------------------------|------------------------|
| R/W-0 | HS-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | |
| PTGSTRT | PTGWDTO | — | — | — | — | PTGITM1 ⁽¹⁾ | PTGITM0 ⁽¹⁾ |
| bit 7 | | | | | | | bit 0 |

| | | | |
|-------------------|----------------------------|------------------------------------|--------------------|
| Legend: | HS = Hardware Settable bit | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

- bit 15 **PTGEN:** Module Enable bit
1 = PTG module is enabled
0 = PTG module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **PTGSIDL:** PTG Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode
- bit 12 **PTGTOGL:** PTG TRIG Output Toggle Mode bit
1 = Toggle state of the PTGOx for each execution of the PTGTRIG command
0 = Each execution of the PTGTRIG command will generate a single PTGOx pulse determined by the value in the PTGPWDx bits
- bit 11 **Unimplemented:** Read as '0'
- bit 10 **PTGSWT:** PTG Software Trigger bit⁽²⁾
1 = Triggers the PTG module
0 = No action (clearing this bit will have no effect)
- bit 9 **PTGSSEN:** PTG Enable Single-Step bit⁽³⁾
1 = Enables Single-Step mode
0 = Disables Single-Step mode
- bit 8 **PTGIVIS:** PTG Counter/Timer Visibility Control bit
1 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the current values of their corresponding counter/timer registers (PTGSD, PTGCx, PTGTx)
0 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the value previously written to those limit registers
- bit 7 **PTGSTRT:** PTG Start Sequencer bit
1 = Starts to sequentially execute commands (Continuous mode)
0 = Stops executing commands
- bit 6 **PTGWDTO:** PTG Watchdog Timer Time-out Status bit
1 = PTG Watchdog Timer has timed out
0 = PTG Watchdog Timer has not timed out.
- bit 5-2 **Unimplemented:** Read as '0'

- Note 1:** These bits apply to the PTGWHI and PTGWLO commands only.
- Note 2:** This bit is only used with the PTGCTRL step command software trigger option.
- Note 3:** Use of the PTG Single-Step mode is reserved for debugging tools only.

25.3 Op Amp/Comparator Registers

REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER

| | | | | | | | |
|--------|-----|-----|-----|----------------------|----------------------|----------------------|----------------------|
| R/W-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
| PSIDL | — | — | — | C4EVT ⁽¹⁾ | C3EVT ⁽¹⁾ | C2EVT ⁽¹⁾ | C1EVT ⁽¹⁾ |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|-------|-----|-----|-----|----------------------|----------------------|----------------------|----------------------|
| U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
| — | — | — | — | C4OUT ⁽²⁾ | C3OUT ⁽²⁾ | C2OUT ⁽²⁾ | C1OUT ⁽²⁾ |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **PSIDL:** Comparator Stop in Idle Mode bit
 1 = Discontinues operation of all comparators when device enters Idle mode
 0 = Continues operation of all comparators in Idle mode
- bit 14-12 **Unimplemented:** Read as '0'
- bit 11 **C4EVT:** Op Amp/Comparator 4 Event Status bit⁽¹⁾
 1 = Op amp/comparator event occurred
 0 = Op amp/comparator event did not occur
- bit 10 **C3EVT:** Comparator 3 Event Status bit⁽¹⁾
 1 = Comparator event occurred
 0 = Comparator event did not occur
- bit 9 **C2EVT:** Comparator 2 Event Status bit⁽¹⁾
 1 = Comparator event occurred
 0 = Comparator event did not occur
- bit 8 **C1EVT:** Comparator 1 Event Status bit⁽¹⁾
 1 = Comparator event occurred
 0 = Comparator event did not occur
- bit 7-4 **Unimplemented:** Read as '0'
- bit 3 **C4OUT:** Comparator 4 Output Status bit⁽²⁾
When CPOL = 0:
 1 = VIN+ > VIN-
 0 = VIN+ < VIN-
When CPOL = 1:
 1 = VIN+ < VIN-
 0 = VIN+ > VIN-
- bit 2 **C3OUT:** Comparator 3 Output Status bit⁽²⁾
When CPOL = 0:
 1 = VIN+ > VIN-
 0 = VIN+ < VIN-
When CPOL = 1:
 1 = VIN+ < VIN-
 0 = VIN+ > VIN-

- Note 1:** Reflects the value of the of the CEVT bit in the respective Op Amp/Comparator Control register, CMxCON<9>.
- 2:** Reflects the value of the COUT bit in the respective Op Amp/Comparator Control register, CMxCON<8>.

REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER

| | | | | | | | |
|--------|-------|-------|-----|-----|-----|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| CON | COE | CPOL | — | — | — | CEVT | COUT |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|--------|--------|-----|---------------------|-----|-----|---------------------|---------------------|
| R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| EVPOL1 | EVPOL0 | — | CREF ⁽¹⁾ | — | — | CCH1 ⁽¹⁾ | CCH0 ⁽¹⁾ |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CON:** Comparator Enable bit
 1 = Comparator is enabled
 0 = Comparator is disabled
- bit 14 **COE:** Comparator Output Enable bit
 1 = Comparator output is present on the CxOUT pin
 0 = Comparator output is internal only
- bit 13 **CPOL:** Comparator Output Polarity Select bit
 1 = Comparator output is inverted
 0 = Comparator output is not inverted
- bit 12-10 **Unimplemented:** Read as '0'
- bit 9 **CEVT:** Comparator Event bit
 1 = Comparator event according to EVPOL<1:0> settings occurred; disables future triggers and interrupts until the bit is cleared
 0 = Comparator event did not occur
- bit 8 **COUT:** Comparator Output bit
 When CPOL = 0 (non-inverted polarity):
 1 = VIN+ > VIN-
 0 = VIN+ < VIN-
 When CPOL = 1 (inverted polarity):
 1 = VIN+ < VIN-
 0 = VIN+ > VIN-
- bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
 11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)
 10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
 If CPOL = 1 (inverted polarity):
 Low-to-high transition of the comparator output.
 If CPOL = 0 (non-inverted polarity):
 High-to-low transition of the comparator output.
 01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)
 If CPOL = 1 (inverted polarity):
 High-to-low transition of the comparator output.
 If CPOL = 0 (non-inverted polarity):
 Low-to-high transition of the comparator output.
 00 = Trigger/event/interrupt generation is disabled

Note 1: Inputs that are selected and not available will be tied to Vss. See the “Pin Diagrams” section for available inputs for each package.

FIGURE 30-27: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)
TIMING CHARACTERISTICS

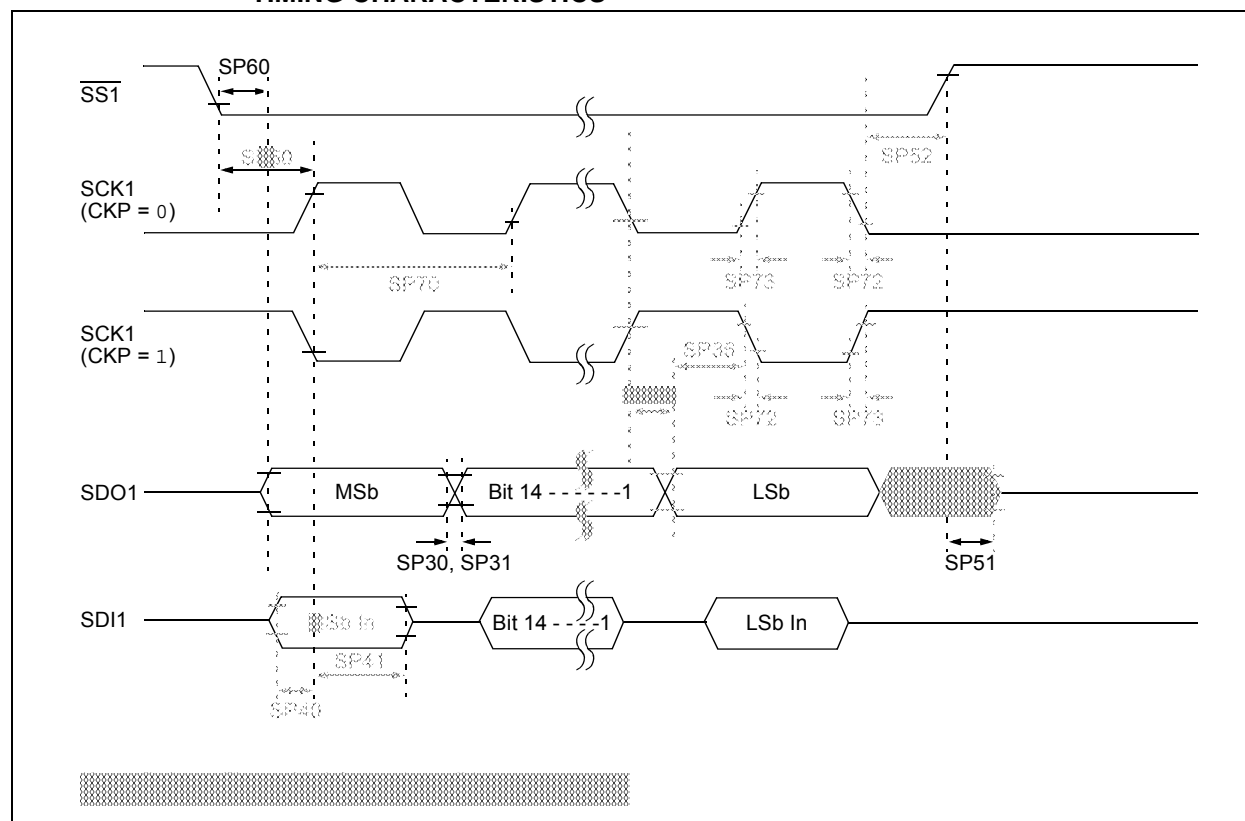


TABLE 30-60: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽¹⁾ Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended | | | | |
|--------------------|--------|---|--|---------|-------|-------|--------------------------------------|
| Param No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Conditions |
| Clock Parameters | | | | | | | |
| AD50 | TAD | ADC Clock Period | 117.6 | — | — | ns | |
| AD51 | tRC | ADC Internal RC Oscillator Period ⁽²⁾ | — | 250 | — | ns | |
| Conversion Rate | | | | | | | |
| AD55 | tCONV | Conversion Time | — | 14 TAD | — | ns | |
| AD56 | FCNV | Throughput Rate | — | — | 500 | ksps | |
| AD57a | TSAMP | Sample Time when Sampling any ANx Input | 3 TAD | — | — | — | |
| AD57b | TSAMP | Sample Time when Sampling the Op Amp Outputs (Configuration A and Configuration B) ^(4,5) | 3 TAD | — | — | — | |
| Timing Parameters | | | | | | | |
| AD60 | tPCS | Conversion Start from Sample Trigger ^(2,3) | 2 TAD | — | 3 TAD | — | Auto-convert trigger is not selected |
| AD61 | tPSS | Sample Start from Setting Sample (SAMP) bit ^(2,3) | 2 TAD | — | 3 TAD | — | |
| AD62 | tCSS | Conversion Completion to Sample Start (ASAM = 1) ^(2,3) | — | 0.5 TAD | — | — | |
| AD63 | tDPU | Time to Stabilize Analog Stage from ADC Off to ADC On ^(2,3) | — | — | 20 | μs | (Note 6) |

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: Parameters are characterized but not tested in manufacturing.

3: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

4: See Figure 25-6 for configuration information.

5: See Figure 25-7 for configuration information.

6: The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (AD1CON1<15>) = 1). During this time, the ADC result is indeterminate.