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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64mc204t-i-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams (Continued)



1.0 DEVICE OVERVIEW

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com)
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X BLOCK DIAGRAM



FIGURE 4-4: PROGRAM MEMORY MAP FOR dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X AND PIC24EP256GP/MC20X DEVICES



Note: Memory areas are not shown to scale.







EXAMPLE 4-3: PAGED DATA MEMORY SPACE

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

				(,			
R/SO-0 ⁽¹	⁾ R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	NVMSIDL ⁽²⁾			—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾
	—	—	<u> </u>	NVMOP3 ^(3,4)	NVMOP2 ^(3,4)	NVMOP1 ^(3,4)	NVMOP0 ^(3,4)
bit 7							bit 0
						_	
Legend:		SO = Settab	le Only bit				
R = Reada	ble bit	W = Writable	e bit	U = Unimplem	ented bit, read	as '0'	
-n = Value	at POR	'1' = Bit is se	t	'0' = Bit is clea	ired	x = Bit is unkn	iown
bit 15 WR: Write Control bit ⁽¹⁾ 1 = Initiates a Flash memory program or erase operation; the operation is self-timed a cleared by hardware once the operation is complete 0 = Program or erase operation is complete and inactive					and the bit is		
bit 14	WREN: Write 1 = Enables F 0 = Inhibits Fl	Enable bit ⁽¹⁾ ⁻ lash program ash program/	n/erase operati ⁄erase operatio	ons			
bit 13	 WRERR: Write Sequence Error Flag bit⁽¹⁾ 1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatica on any set attempt of the WR bit) 0 = The program or erase operation completed normally. 					t automatically	
bit 12	NVMSIDL: N\ 1 = Flash volt 0 = Flash volt	/M Stop in Idl age regulator age regulator	e Control bit ⁽²⁾ goes into Star is active durin	ndby mode duri g Idle mode	ng Idle mode		
bit 11-4	Unimplement	ted: Read as	'0'	-			
bit 11-4 Onimplemented: Read as 0 bit 3-0 NVMOP<3:0>: NVM Operation Select bits ^(1,3,4) 1111 = Reserved 1100 = Reserved 1101 = Reserved 1001 = Reserved 1011 = Reserved 1010 = Reserved 0011 = Memory page erase operation 0010 = Reserved 0001 = Memory double-word program operation ⁽⁵⁾ 0000 = Reserved							
Note 1: 2: 3: 4: 5:	These bits can only If this bit is set, the (TVREG) before Fla All other combination Execution of the PV Two adjacent word	/ be reset on a re will be mini sh memory be ons of NVMO wRSAV instruct s on a 4-word	a POR. mal power sav ecomes operat P<3:0> are uni tion is ignored I boundary are	rings (IIDLE) and ional. implemented. while any of the programmed d	d upon exiting lo e NVM operatio uring execution	the mode, there ns are in progra	is a delay ess. on.

REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0	
OA	OB	SA	SB	OAB	SAB	DA	DC	
bit 15							bit 8	
R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R-0	R/W-0	R/W-0	R/W-0	R/W-0	
	IPL<2:0> ⁽²⁾		RA	Ν	OV	Z	С	
bit 7						-	bit 0	
								1

REGISTER 7-1: SR: CPU STATUS REGISTER⁽¹⁾

Legend:	C = Clearable bit		-
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1'= Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5	IPL<2:0>: CPU Interrupt Priority Level Status bits ^(2,3)
	111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
	110 = CPU Interrupt Priority Level is 6 (14)
	101 = CPU Interrupt Priority Level is 5 (13)
	100 = CPU Interrupt Priority Level is 4 (12)
	011 = CPU Interrupt Priority Level is 3 (11)
	010 = CPU Interrupt Priority Level is 2 (10)
	001 = CPU Interrupt Priority Level is 1 (9)
	000 = CPU Interrupt Priority Level is 0 (8)

- **Note 1:** For complete register details, see Register 3-1.
 - 2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
 - **3:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	_	PPST3	PPST2	PPST1	PPST0
bit 7							bit 0

REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER

Legend:					
R = Readable bit		W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value a	at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	
bit 15-4	Unimple	mented: Read as '0'			
bit 3	PPST3: [MA Channel 3 Ping-Pong	Mode Status Flag bit		
	1 = DMA	STB3 register is selected			
	0 = DMA	STA3 register is selected			
bit 2	PPST2: [MA Channel 2 Ping-Pong	Mode Status Flag bit		
	1 = DMA	STB2 register is selected			
	0 = DMA	STA2 register is selected			
bit 1	PPST1: [MA Channel 1 Ping-Pong	Mode Status Flag bit		

- 1 = DMASTB1 register is selected0 = DMASTA1 register is selected
- bit 0 PPST0: DMA Channel 0 Ping-Pong Mode Status Flag bit
 - 1 = DMASTB0 register is selected
 - 0 = DMASTA0 register is selected

10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the powersaving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the ECAN[™] module has been configured for 500 kbps, based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the ECAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC[®] DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note:	If a PMD bit is set, the corresponding
	module is disabled after a delay of one
	instruction cycle. Similarly, if a PMD bit is
	cleared, the corresponding module is
	enabled after a delay of one instruction
	cycle (assuming the module control regis-
	ters are already configured to enable
	module operation).

10.5 Power-Saving Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.



10.5.1 KEY RESOURCES

- "Watchdog Timer and Power-Saving Modes" (DS70615) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

14.2 Input Capture Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13	ICSIDL: Input Capture Stop in Idle Control bit
	1 = Input capture will Halt in CPU Idle mode
	0 = Input capture will continue to operate in CPU Idle mode
bit 12-10	ICTSEL<2:0>: Input Capture Timer Select bits
	111 = Peripheral clock (FP) is the clock source of the ICx
	110 = Reserved
	101 = Reserved
	100 - 11 CLR is the clock source of the ICx (only the synchronous clock is supported) 011 = T5CLK is the clock source of the ICx
	010 = T4CLK is the clock source of the ICx
	001 = T2CLK is the clock source of the ICx
	000 = T3CLK is the clock source of the ICx
bit 9-7	Unimplemented: Read as '0'
bit 6-5	ICI<1:0>: Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
	11 = Interrupt on every fourth capture event
	10 = Interrupt on every third capture event
	01 = Interrupt on every second capture event
hit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
Dit 4	1 = Input capture buffer overflow occurred
	0 = No input capture buffer overflow occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	1 = Input capture buffer is not empty, at least one more capture value can be read
	0 = Input capture buffer is empty
bit 2-0	ICM<2:0>: Input Capture Mode Select bits
	111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
	110 = Unused (module is disabled)
	101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
	100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
	011 = Capture mode, every falling edge (Simple Capture mode)
	001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
	000 = Input capture module is turned off

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	_		LEB	<11:8>	
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			LEE	3<7:0>			
bit 7							bit 0
Legend:							
R = Readable	dable bit W = Writable bit U = Unimplemented bit, read as '0'						
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown				nown			

REGISTER 16-17: LEBDLYx: PWMx LEADING-EDGE BLANKING DELAY REGISTER

bit 15-12 Unimplemented: Read as '0'

bit 11-0 LEB<11:0>: Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN ⁽¹⁾	UTXBF	TRMT
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0
Legend:		HC = Hardwar	e Clearable bit	C = Clearable	e bit		
R = Readable	bit	W = Writable b	bit	U = Unimplemented bit, read as '0'			

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15,13 UTXISEL<1:0>: UARTx Transmission Interrupt Mode Selection bits

- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 UTXINV: UARTx Transmit Polarity Inversion bit
 - $\frac{\text{If IREN = 0:}}{1 = \text{UxTX Idle state is '0'}}$
 - 0 = UxTX Idle state is '1'
 - If IREN = 1:
 - 1 = IrDA encoded, UxTX Idle state is '1'
 - 0 = IrDA encoded, UxTX Idle state is '0'
- bit 12 Unimplemented: Read as '0'
- bit 11 UTXBRK: UARTx Transmit Break bit
 - 1 = Sends Sync Break on next transmission Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
 - 0 = Sync Break transmission is disabled or completed
- bit 10 UTXEN: UARTx Transmit Enable bit⁽¹⁾ 1 = Transmit is enabled, UxTX pin is controlled by UARTx
 - 0 = Transmit is disabled, any pending transmission is aborted and buffer is reset; UxTX pin is controlled by the PORT
- bit 9 UTXBF: UARTx Transmit Buffer Full Status bit (read-only)
 - 1 = Transmit buffer is full
 - 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 TRMT: Transmit Shift Register Empty bit (read-only)
 - 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
 - 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
- bit 7-6 URXISEL<1:0>: UARTx Receive Interrupt Mode Selection bits
 - 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
 - 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
 - 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters
- **Note 1:** Refer to the "**UART**" (DS70582) section in the "*dsPIC33/PIC24 Family Reference Manual*" for information on enabling the UARTx module for transmit operation.

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	_	_	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0
bit 15							bit 8
U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
	ICODE6	ICODE5	ICODE4	ICODE3	ICODE2	ICODE1	ICODE0
bit 7			1	1	I	1	bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own
bit 15-13	Unimplemen	ted: Read as '	0'				
bit 12-8	FILHIT<4:0>:	Filter Hit Num	ber bits				
	10000-1111	1 = Reserved					
	01111 = Filte	r 15					
	•						
	•						
	•						
	00001 = Filte 00000 = Filte	r 1 r 0					
bit 7	Unimplemen	ted: Read as '	0'				
bit 6-0	ICODE<6:0>:	: Interrupt Flag	Code bits				
	1000101-11	11111 = Rese	rved				
	1000100 = F	IFO almost full	interrupt				
	1000011 = R 1000010 = W	ake-up interru	pt				
	1000001 = E	rror interrupt					
	1000000 = N	o interrupt					
	•						
	•						
	•						
	0010000-01	11111 = Kese B15 buffer inte	rved				
	•		nupt				
	•						
	•						
	0001001 = R	B9 buffer inter	rupt				
	0001000 = R	B8 buffer inter	rupt				
	0000111 = T	RB7 buffer inte	rrupt				
	0000110 = 1	RB5 buffer inte	errupt				
	0000100 = T	RB4 buffer inte	errupt				
	0000011 = T	RB3 buffer inte	rrupt				
	0000010 = T	RB2 buffer inte	rrupt				
	0000001 = T	RB1 buffer inte	errupt				
			πupι				

REGISTER 21-3: CxVEC: ECANx INTERRUPT CODE REGISTER

REGISTER 21-22: CxRXFUL1: ECANx RECEIVE BUFFER FULL REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8
bit 15							bit 8

| R/C-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| RXFUL7 | RXFUL6 | RXFUL5 | RXFUL4 | RXFUL3 | RXFUL2 | RXFUL1 | RXFUL0 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 **RXFUL<15:0>:** Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)

REGISTER 21-23: CxRXFUL2: ECANx RECEIVE BUFFER FULL REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXFUL31 | RXFUL30 | RXFUL29 | RXFUL28 | RXFUL27 | RXFUL26 | RXFUL25 | RXFUL24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXFUL23 | RXFUL22 | RXFUL21 | RXFUL20 | RXFUL19 | RXFUL18 | RXFUL17 | RXFUL16 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 **RXFUL<31:16>:** Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)

REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2 (CONTINUED)

bit 1	BUFM: Buffer Fill Mode Select bit					
	 1 = Starts the buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on next interrupt 0 = Always starts filling the buffer from the start address. 					
bit 0	ALTS: Alternate Input Sample Mode Select bit					

1 = Uses channel input selects for Sample MUXA on first sample and Sample MUXB on next sample 0 = Always uses channel input selects for Sample MUXA

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0								
		—	_	—	—		ADDMAEN								
bit 15							bit 8								
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0								
—	—	—	—	—	DMABL2	DMABL1	DMABL0								
bit 7							bit 0								
Legend:															
R = Readable	e bit	W = Writable b	pit	U = Unimple	mented bit, read	d as '0'									
-n = Value at	-n = Value at POR '1' = Bit is set			'0' = Bit is cle	eared	x = Bit is unknown									
L															
bit 15-9	Unimplemen	ted: Read as 'o)'												
bit 8	ADDMAEN: /	ADC1 DMA Ena	able bit												
	1 = Conversio	on results are st	ored in the Al	DC1BUF0 regi	ster for transfer	to RAM using	DMA								
	0 = Conversio	on results are st	ored in ADC1	BUF0 through	ADC1BUFF reg	gisters; DMA w	vill not be used								
bit 7-3	Unimplemen	ted: Read as '0)'												
bit 2-0	DMABL<2:0>	Selects Number Selects Number	per of DMA Bu	uffer Locations	per Analog Inp	ut bits									
	111 = Allocat	es 128 words o	f buffer to eac	h analog input	t										
	110 = Allocat	es 64 words of	buffer to each	analog input											
	101 = Allocat	es 32 words of	buffer to each	analog input											
	100 = Allocat	es 16 words of	buffer to each	analog input											
		es 8 words of b	uffer to each a	analog input											
		es 2 words of h	uffer to each :	analog input											
	000 = Allocat	es 1 word of bu	ffer to each a	nalog input											
							000 – Allocates T word of buller to each analog input								

REGISTER 23-4: AD1CON4: ADC1 CONTROL REGISTER 4







DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM



DC CHARACTERISTICS			$\begin{tabular}{ l l l l l l l l l l l l l l l l l l l$					
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions	
Operating Voltage								
DC10	Vdd	Supply Voltage	3.0	_	3.6	V		
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	_	_	Vss	V		
DC17	Svdd	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.03	—	—	V/ms	0V-1V in 100 ms	

TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

TABLE 30-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated):Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended							
Param No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Comments
	Cefc	External Filter Capacitor Value ⁽¹⁾	4.7	10	_	μF	Capacitor must have a low series resistance (< 1 Ohm)

Note 1: Typical VCAP voltage = 1.8 volts when VDD \geq VDDMIN.

DC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions		
	VIL	Input Low Voltage							
DI10		Any I/O Pin and MCLR	Vss	—	0.2 VDD	V			
DI18		I/O Pins with SDAx, SCLx	Vss	_	0.3 VDD	V	SMBus disabled		
DI19		I/O Pins with SDAx, SCLx	Vss	—	0.8	V	SMBus enabled		
	Vih	Input High Voltage							
DI20		I/O Pins Not 5V Tolerant	0.8 VDD	—	Vdd	V	(Note 3)		
		I/O Pins 5V Tolerant and MCLR	0.8 VDD	—	5.5	V	(Note 3)		
		I/O Pins with SDAx, SCLx	0.8 VDD	—	5.5	V	SMBus disabled		
		I/O Pins with SDAx, SCLx	2.1	—	5.5	V	SMBus enabled		
	ICNPU	Change Notification Pull-up Current							
DI30			150	250	550	μA	VDD = 3.3V, VPIN = VSS		
	ICNPD	Change Notification Pull-Down Current ⁽⁴⁾							
DI31			20	50	100	μA	VDD = 3.3V, VPIN = VDD		

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 2: Negative current is defined as current sourced by the pin.
- 3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 4: VIL source < (VSS 0.3). Characterized but not tested.

5: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

- 6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.



FIGURE 30-36: ADC CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)