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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64mc502-e-mm

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams (Continued)



TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL		0000
INTCON2	08C2	GIE	DISI	SWTRAP	_	_		_	_	_	_	_	_	_	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	_	_	_	_	_		_	_	_	_	DAE	DOOVR	_	_	_	_	0000
INTCON4	08C6					_	_			_				_	—		SGHT	0000
INTTREG	08C8						ILR<	3:0>					VECNU	M<7:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

10.0 POWER-SAVING FEATURES

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Watchdog Timer and Power-Saving Modes" (DS70615) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- · Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

PWRSAV	#SLEEP_MODE	;	Put	the	device	into	Sleep mode
PWRSAV	#IDLE_MODE	;	Put	the	device	into	Idle mode

10.1 Clock Frequency and Clock Switching

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or highprecision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

10.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 10-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

11.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code, or a complete redesign, may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the label, "RPn" or "RPIn", in their full pin designation, where "n" is the remappable pin number. "RP" is used to designate pins that support both remappable input and output functions, while "RPI" indicates pins that support remappable input functions only.

11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs. In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C^{TM} and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and nonremappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheralselectable pin is handled in two different ways, depending on whether an input or output is being mapped.

14.2 Input Capture Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend: HC = Hardware Clearable bit		HS = Hardware Settable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-14	Unimplemented: Read as '0'
bit 13	ICSIDL: Input Capture Stop in Idle Control bit
	1 = Input capture will Halt in CPU Idle mode
	0 = Input capture will continue to operate in CPU Idle mode
bit 12-10	ICTSEL<2:0>: Input Capture Timer Select bits
	111 = Peripheral clock (FP) is the clock source of the ICx
	110 = Reserved
	101 = Reserved
	100 - 11 CLR is the clock source of the ICx (only the synchronous clock is supported) 011 = T5CLK is the clock source of the ICx
	010 = T4CLK is the clock source of the ICx
	001 = T2CLK is the clock source of the ICx
	000 = T3CLK is the clock source of the ICx
bit 9-7	Unimplemented: Read as '0'
bit 6-5	ICI<1:0>: Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
	11 = Interrupt on every fourth capture event
	10 = Interrupt on every third capture event
	01 = Interrupt on every second capture event
hit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
Dit 4	1 = Input capture buffer overflow occurred
	0 = No input capture buffer overflow occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	1 = Input capture buffer is not empty, at least one more capture value can be read
	0 = Input capture buffer is empty
bit 2-0	ICM<2:0>: Input Capture Mode Select bits
	111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
	110 = Unused (module is disabled)
	101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
	100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
	011 = Capture mode, every falling edge (Simple Capture mode)
	001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
	000 = Input capture module is turned off

FIGURE 17-1: QEI BLOCK DIAGRAM



19.2 I²C Control Registers

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	_	I2CSIDL	SCLREL	IPMIEN ⁽¹⁾	A10M	DISSLW	SMEN
bit 15					•		bit 8
R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0
Legend:		HC = Hardware	Clearable bit				
R = Readable	e bit	W = Writable bit	t	U = Unimpler	mented bit, rea	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
bit 15	12CEN: 12Cx	Enable bit					
	1 = Enables t	he I2Cx module a	and configures	the SDAx and	SCLx pins as	serial port pins	;
h it 4.4			all I-C ···· pins a	are controlled	by port function	15	
DIL 14		ted: Read as 0	da hit				
DIE 13	1 - Discontinu	x Stop in Idle Mo	de bli ation whon dow	ico ontore an l	dla mada		
	0 = Continues	s module operation	on in Idle mode		die mode		
bit 12	SCLREL: SC	Lx Release Cont	rol bit (when or	perating as I ² C	slave)		
	1 = Releases	SCLx clock		U	,		
	0 = Holds SC	Lx clock low (cloo	ck stretch)				
	$\frac{\text{If STREN} = 1}{\text{Distance}}$	<u>:</u>			· · · · · · · · · · · · · · · · · · ·		
	Bit is R/W (i.e	., software can w	rite '0' to initiate o data byte tra	e stretch and w	rite '1' to relea	se clock). Harc	dware is clear
	address byte	reception. Hardw	are is clear at	the end of eve	ry slave data b	yte reception.	l every slave
	If STREN = 0	<u>:</u>			-		
	Bit is R/S (i.e.	, software can on	ly write '1' to re	elease clock). I	Hardware is cle	ar at the begin	ning of every
	slave data by		Hardware is cle	ar at the end o	of every slave a	address byte re	eception.
bit 11	IPMIEN: Intel	ligent Peripheral	Management I	nterface (IPMI)) Enable bit		
	1 = IPMI mod 0 = IPMI mod	e is enabled, all a		Acknowledged	I		
bit 10	A10M: 10-Bit	Slave Address b	it				
	1 = I2CxADD	is a 10-bit slave	address				
	0 = I2CxADD	is a 7-bit slave a	ddress				
bit 9	DISSLW: Disa	able Slew Rate C	Control bit				
	1 = Slew rate 0 = Slew rate	control is disable control is enable	ed d				
bit 8	SMEN: SMBL	us Input Levels bi	t				
	1 = Enables I 0 = Disables \$	/O pin thresholds SMBus input thre	compliant with sholds	SMBus speci	fication		
bit 7	GCEN: Gene	ral Call Enable bi	it (when operat	ing as I ² C slav	re)		
	1 = Enables in 0 = General c	terrupt when a ge all address disab	neral call addre	ss is received ir	12CxRSR (mo	dule is enabled	for reception)

Note 1: When performing master operations, ensure that the IPMIEN bit is set to '0'.

20.1 UART Helpful Tips

- 1. In multi-node, direct-connect UART networks, receive inputs UART react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
 - a) If URXINV = 0, use a pull-up resistor on the RX pin.
 - b) If URXINV = 1, use a pull-down resistor on the RX pin.
- 2. The first character received on a wake-up from Sleep mode caused by activity on the UxRX pin of the UARTx module will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid; this is to be expected.

20.2 UART Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

20.2.1 KEY RESOURCES

- "UART" (DS70582) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

21.4 ECAN Control Registers

REGISTER 21-1:	CxCTRL1: ECANx CONTROL REGISTER 1
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U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0		
		CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0		
bit 15				·			bit 8		
R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0		
OPMODE2	OPMODE1	OPMODE0		CANCAP	—	—	WIN		
bit 7							bit 0		
[
Legena:	hit	M = M/ritabla I		II – Unimplor	nonted bit read				
		'1' = Bit is set	Witable bit $U = Unimplemented bit, read as U Bit is set U' = Bit is cleared x = Bit is upknown$						
	UK	I - DILIS SEL			aleu		IOWIT		
bit 15-14	Unimplemen	ted: Read as '()'						
bit 13	CSIDL: ECAN	Nx Stop in Idle I	Mode bit						
	1 = Discontin	ues module ope	eration when	device enters I	dle mode				
	0 = Continues	s module opera	tion in Idle m	ode					
bit 12	ABAT: Abort	All Pending Tra	nsmissions b	it					
	1 = Signals al	I transmit buffe	rs to abort tra when all tran	ansmission smissions are a	aborted				
bit 11		CANx Module C	lock (ECAN) S	Source Select b	bit				
2	1 = FCAN is e	qual to 2 * FP							
	0 = FCAN is e	qual to FP							
bit 10-8	REQOP<2:0>	Request Ope	ration Mode	bits					
	111 = Set Lis	ten All Messag	es mode						
	101 = Reserv	red							
	100 = Set Co	nfiguration mod	le						
	011 = Set Lis	ten Only mode							
	001 = Set Dis	able mode							
	000 = Set No	rmal Operation	mode						
bit 7-5	OPMODE<2:	0> : Operation N	/lode bits						
	111 = Module	e is in Listen All	Messages m	node					
	110 = Reserv 101 = Reserv	red red							
	100 = Module	e is in Configura	ation mode						
	011 = Module	e is in Listen Or	ly mode						
	010 = Module	e is in Loopback e is in Disable n	node						
	000 = Module	e is in Normal C	peration mod	de					
bit 4	Unimplemen	ted: Read as 'o)'						
bit 3	CANCAP: CA	N Message Re	eceive Timer	Capture Event	Enable bit				
	1 = Enables in 0 = Disables (nput capture ba CAN capture	ised on CAN	message recei	ve				
bit 2-1	Unimplemen	ted: Read as '()'						
bit 0	WIN: SFR Ma	ap Window Sele	ect bit						
	1 = Uses filter	r window							
	0 = Uses buff	er window							

REGISTER 21-16: CxRXFnSID: ECANx ACCEPTANCE FILTER n STANDARD IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	
bit 15							bit 8	
R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x	
SID2	SID1	SID0	—	EXIDE	_	EID17	EID16	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	d as '0'		
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown		
bit 15-5	SID<10:0>: S	tandard Identif	ier bits					
	1 = Message 0 = Message	address bit, SI address bit, SI	Dx, must be '2 Dx, must be '0	L' to match filte	er er			
bit 4	Unimplement	ted: Read as '	כי					
bit 3	EXIDE: Exten	ded Identifier E	Enable bit					
	If MIDE = 1:							
	1 = Matches c	only messages	with Extende	d Identifier add	lresses			
		only messages	with Standard		resses			
	Ignores EXIDI	E bit.						
bit 2	Unimplement	ted: Read as '	כ'					
bit 1-0	EID<17:16>:	Extended Iden	tifier bits					
	1 = Message	address bit, El	Dx, must be 'a	L' to match filte	er			
	0 = Message	address bit, El	Dx, must be '	o' to match filte	er			

REGISTER 24-12: PTGQPTR: PTG STEP QUEUE POINTER REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—	—		—	_	—		—		
bit 15							bit 8		
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—	—	—	PTGQPTR<4:0>						
bit 7							bit 0		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 Unimplemented: Read as '0'

bit 4-0 **PTGQPTR<4:0>:** PTG Step Queue Pointer Register bits This register points to the currently active Step command in the Step queue.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-13: PTGQUEX: PTG STEP QUEUE REGISTER x (x = 0-7)^(1,3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
STEP(2x + 1)<7:0> ⁽²⁾									
bit 15							bit 8		
R/M/-0	R/M_0	R/M_0	R///_0	R/W_0	R/W_0	R/M_0	R/W_0		

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STEP(2x	()<7:0> ⁽²⁾			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8	STEP(2x + 1)<7:0>: PTG Step Queue Pointer Register bits ⁽²⁾
	A queue location for storage of the STEP(2x + 1) command byte
bit 7-0	STEP(2x)<7:0>: PTG Step Queue Pointer Register bits ⁽²⁾
	A queue location for storage of the STEP(2x) command byte.

- **Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).
 - 2: Refer to Table 24-1 for the Step command encoding.

3: The Step registers maintain their values on any type of Reset.

REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	RW-0
—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0
bit 15							bit 8

| R/W-0 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SELSRCB3 | SELSRCB2 | SELSRCB1 | SELSRCB0 | SELSRCA3 | SELSRCA2 | SELSRCA1 | SELSRCA0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 Unimplemented: Read as '0'

bit 11-8	SELSRCC<3:0>: Mask C Input Select bits
	1111 = FLT4
	1110 = FLT2
	1101 = PTGO19
	1100 = PTGO18
	1011 = Reserved
	1010 = Reserved
	1001 = Reserved
	1000 = Reserved
	0111 = Reserved
	0110 = Reserved
	0101 = PWM3H
	0100 = PWM3L
	0011 = PWM2H
	0010 = PWM2L
	0001 = PWM1H
	0000 = PWM1L
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1001 = Reserved 1000 = Reserved 0011 = Reserved 0111 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved 0110 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1000 = Reserved 1000 = Reserved 0111 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3I
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1000 = Reserved 0111 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0100 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2I
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0101 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0101 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H 0000 = PWM1I

REGISTER 27-1: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R	R	R
			DEVID<2	3:16> (1)			
bit 23							bit 16
R	R	R	R	R	R	R	R
			DEVID<	15:8> (1)			
bit 15							bit 8
R	R	R	R	R	R	R	R
			DEVID<	7:0> (1)			
bit 7							bit 0
Legend:	R = Read-Only bit			U = Unimplen	nented bit		

bit 23-0 **DEVID<23:0>:** Device Identifier bits⁽¹⁾

Note 1: Refer to the "dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration *Bits*" (DS70663) for the list of device ID values.

REGISTER 27-2: DEVREV: DEVICE REVISION REGISTER

R	R	R	R	R	R	R	R
			DEVREV<	<23:16> ⁽¹⁾			
bit 23							bit 16
R	R	R	R	R	R	R	R
			DEVREV	<15:8> (1)			
bit 15							bit 8
R	R	R	R	R	R	R	R
			DEVRE	/<7:0> ⁽¹⁾			
bit 7							bit 0
Legend:	R = Read-only bit			U = Unimpler	nented bit		

bit 23-0 **DEVREV<23:0>:** Device Revision bits⁽¹⁾

Note 1: Refer to the "dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration *Bits*" (DS70663) for the list of device revision values.

DC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$			
Parameter No.	Тур.	Max.	Units	Units Conditions		
DC61d	8		μΑ	-40°C		
DC61a	10	—	μA	+25°C	2.21/	
DC61b	12	_	μA	+85°C	3.3V	
DC61c	13		μA	+125°C		

TABLE 30-9: DC CHARACTERISTICS: WATCHDOG TIMER DELTA CURRENT (Δ Iwdt)⁽¹⁾

Note 1: The \triangle IwDT current is the additional current consumed when the module is enabled. This current should be added to the base IPD current. All parameters are characterized but not tested during manufacturing.

TABLE 30-10: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

DC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Parameter No. Typ. Max.			Doze Ratio	Units	Conditions		
Doze Current (IDOZE) ⁽¹⁾							
DC73a ⁽²⁾	35	_	1:2	mA	40°C	3.3V	Fosc = 140 MHz
DC73g	20	30	1:128	mA	-40 C		
DC70a ⁽²⁾	35	—	1:2	mA	+25%	3.3V	Fosc = 140 MHz
DC70g	20	30	1:128	mA	720 C		
DC71a ⁽²⁾	35	—	1:2	mA	+95°C	3.3V	Fosc = 140 MHz
DC71g	20	30	1:128	mA	+05 C		
DC72a ⁽²⁾	28	_	1:2	mA	±125°C	3 3\/	Ecco - 120 MHz
DC72g	15	30	1:128	mA	+120 C	3.3V	FUSC - 120 MHZ

Note 1: IDOZE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDOZE measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- · All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- CPU is executing while(1) statement
- · JTAG is disabled
- 2: Parameter is characterized but not tested in manufacturing.

AC CHARACTERISTICS		$ \begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)}^{(1)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array} $					
Param No.	Symbol	Symbol Characteristic		Тур.	Max.	Units	Conditions
		ADC /	Accuracy	/ (12-Bit	Mode)		
AD20a	Nr	Resolution	12	2 Data Bi	its	bits	
AD21a	INL	Integral Nonlinearity	-2.5		2.5	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-5.5	_	5.5	LSb	+85°C < TA \leq +125°C (Note 2)
AD22a	DNL	Differential Nonlinearity	-1		1	LSb	-40°C \leq TA \leq +85°C (Note 2)
			-1		1	LSb	+85°C < TA \leq +125°C (Note 2)
AD23a	Gerr	Gain Error ⁽³⁾	-10		10	LSb	-40°C \leq TA \leq +85°C (Note 2)
			-10		10	LSb	+85°C < TA \leq +125°C (Note 2)
AD24a	EOFF	Offset Error	-5		5	LSb	$-40^{\circ}C \le TA \le +85^{\circ}C$ (Note 2)
			-5		5	LSb	+85°C < TA \leq +125°C (Note 2)
AD25a	—	Monotonicity	—			—	Guaranteed
		Dynamic	Performa	ance (12	-Bit Mod	e)	
AD30a	THD	Total Harmonic Distortion ⁽³⁾	—	75		dB	
AD31a	SINAD	Signal to Noise and Distortion ⁽³⁾		68	-	dB	
AD32a	SFDR	Spurious Free Dynamic Range ⁽³⁾	_	80	_	dB	
AD33a	Fnyq	Input Signal Bandwidth ⁽³⁾	_	250	—	kHz	
AD34a	ENOB	Effective Number of Bits ⁽³⁾	11.09	11.3	_	bits	

TABLE 30-58: ADC MODULE SPECIFICATIONS (12-BIT MODE)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

3: Parameters are characterized but not tested in manufacturing.

28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	Limits	MIN	NOM	MAX	
Number of Pins	Ν	28			
Pitch	е	0.65 BSC			
Overall Height	А	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Terminal Thickness		0.20 REF			
Overall Width	Е	6.00 BSC			
Exposed Pad Width	E2	3.65	3.70	4.70	
Overall Length	D	6.00 BSC			
Exposed Pad Length	D2	3.65	3.70	4.70	
Terminal Width	b	0.23	0.30	0.35	
Terminal Length	L	0.30	0.40	0.50	
Terminal-to-Exposed Pad K		0.20	-	-	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated

3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

 $\label{eq:REF:Reference Dimension, usually without tolerance, for information purposes only.$

Microchip Technology Drawing C04-124C Sheet 2 of 2

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS				
Dimension	Dimension Limits		NOM	MAX		
Number of Pins	N	44				
Pitch	Pitch e		0.65 BSC			
Overall Height	А	0.80 0.90 1.00				
Standoff	A1	0.00	0.02	0.05		
Terminal Thickness	A3	0.20 REF				
Overall Width E		8.00 BSC				
Exposed Pad Width	E2	6.25 6.45 6.60		6.60		
Overall Length		8.00 BSC				
Exposed Pad Length	D2	6.25 6.45 6.60		6.60		
Terminal Width	b	0.20	0.30	0.35		
Terminal Length	L	0.30	0.40	0.50		
Terminal-to-Exposed-Pad		0.20	-	-		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated

3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension. usually without tolerance. for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch E		0.65 BSC		
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing			8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44) Y				0.85
Distance Between Pads G		0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B

TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 30.0 "Electrical Characteristics"	Removed Voltage on VCAP with respect to Vss and added Note 5 in Absolute Maximum Ratings ⁽¹⁾ .
	Removed Parameter DC18 (VCORE) and Note 3 from the DC Temperature and Voltage Specifications (see Table 30-4).
	Updated Note 1 in the DC Characteristics: Operating Current (IDD) (see Table 30-6).
	Updated Note 1 in the DC Characteristics: Idle Current (IIDLE) (see Table 30-7).
	Changed the Typical values for Parameters DC60a-DC60d and updated Note 1 in the DC Characteristics: Power-down Current (IPD) (see Table 30-8).
	Updated Note 1 in the DC Characteristics: Doze Current (IDOZE) (see Table 30-9).
	Updated Note 2 in the Electrical Characteristics: BOR (see Table 30-12).
	Updated Parameters CM20 and CM31, and added Parameters CM44 and CM45 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14).
	Added the Op amp/Comparator Reference Voltage Settling Time Specifications (see Table 30-15).
	Added Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16).
	Updated Internal FRC Accuracy Parameter F20a (see Table 30-21).
	Updated the Typical value and Units for Parameter CTMUI1, and added Parameters CTMUI4, CTMUFV1, and CTMUFV2 to the CTMU Current Source Specifications (see Table 30-55).
Section 31.0 "Packaging Information"	Updated packages by replacing references of VLAP with TLA.
"Product Identification System"	Changed VLAP to TLA.

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