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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

⊡XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64mc502-i-mm

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#### **Pin Diagrams (Continued)**



## Pin Diagrams (Continued)



Pin Name <sup>(4)</sup>	Pin Type	Buffer Type	PPS	Description							
U2CTS	1	ST	No	UART2 Clear-To-Send.							
U2RTS	0		No	UART2 Ready-To-Send.							
U2RX	I.	ST	Yes	UART2 receive.							
U2TX	Ó	_	Yes	UART2 transmit.							
BCLK2	Ō	ST	No	UART2 IrDA <sup>®</sup> baud clock output.							
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.							
SDI1	I	ST	No	SPI1 data in.							
SDO1	0	—	No	SPI1 data out.							
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.							
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.							
SDI2	I	ST	Yes	SPI2 data in.							
SDO2	0	—	Yes	SPI2 data out.							
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.							
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.							
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.							
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.							
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.							
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.							
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.							
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.							
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.							
TMS <sup>(5)</sup>	Ι	ST	No	JTAG Test mode select pin.							
TCK	I	ST	No	JTAG test clock input pin.							
TDI	I	ST	No	JTAG test data input pin.							
TDO	0	_	No	JTAG test data output pin.							
C1RX <sup>(2)</sup>	I	ST	Yes	ECAN1 bus receive pin.							
C1TX <sup>(2)</sup>	0	_	Yes	ECAN1 bus transmit pin.							
FLT1 <sup>(1)</sup> , FLT2 <sup>(1)</sup>	I	ST	Yes	PWM Fault Inputs 1 and 2.							
FLT3 <sup>(1)</sup> , FLT4 <sup>(1)</sup>	I	ST	No	PWM Fault Inputs 3 and 4.							
FLT32 <sup>(1,3)</sup>	I	ST	No	PWM Fault Input 32 (Class B Fault).							
DTCMP1-DTCMP3 <sup>(1)</sup>	I	ST	Yes	PWM Dead-Time Compensation Inputs 1 through 3.							
PWM1L-PWM3L <sup>(1)</sup>	0	—	No	PWM Low Outputs 1 through 3.							
PWM1H-PWM3H <sup>(1)</sup>	0	—	No	PWM High Outputs 1 through 3.							
SYNCI1 <sup>(1)</sup>	I	ST	Yes	PWM Synchronization Input 1.							
SYNCO1 <sup>(1)</sup>	0	—	Yes	PWM Synchronization Output 1.							
INDX1 <sup>(1)</sup>	Ι	ST	Yes	Quadrature Encoder Index1 pulse input.							
HOME1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Home1 pulse input.							
QEA1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer							
(4)				external clock/gate input in Timer mode.							
QEB1 <sup>(1)</sup>	I	ST	Yes	Quadrature Encoder Phase B input in QEI1 mode. Auxiliary timer							
				external clock/gate input in Timer mode.							
CNTCMP1''	υ	—	Yes	Quadrature Encoder Compare Output 1.							

# TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

 Legend:
 CMOS = CMOS compatible input or output
 Analog = Analog input

 ST = Schmitt Trigger input with CMOS levels
 O = Output

 PPS = Peripheral Pin Select
 TTL = TTL input buffer

P = Power I = Input

Note 1: This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This pin is available on dsPIC33EPXXXGP/MC50X devices only.

3: This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)" for more information.

4: Not all pins are available in all packages variants. See the "Pin Diagrams" section for pin availability.

5: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

#### TABLE 4-34: NVM REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0728	WR	WREN	WRERR	NVMSIDL	_	_	_	_	_	_	_	_	NVMOP<3:0>			0000	
NVMADRL	072A	NVMADR<15:0>										0000						
NVMADRH	072C		_	_	_	_		_		NVMADR<23:16>						0000		
NVMKEY	072E	_	_		_	_	_	_	_	NVMKEY<7:0>						0000		

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

#### TABLE 4-35: SYSTEM CONTROL REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	_		VREGSF	_	СМ	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	Note 1
OSCCON	0742	_	(	COSC<2:0>				NOSC<2:0>		CLKLOCK	IOLOCK	LOCK	_	CF	_	_	OSWEN	Note 2
CLKDIV	0744	ROI	[	DOZE<2:0>		DOZEN	N FRCDIV<2:0>			PLLPOS	LLPOST<1:0> — PLLPRE<4:0>				0030			
PLLFBD	0746	_	_	_			_	—	PLLDIV<8:0>				0030					
OSCTUN	0748	_	_	_	_	_	_	_	_	— — — TUN<5:0>				0000				

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: RCON register Reset values are dependent on the type of Reset.

2: OSCCON register Reset values are dependent on the Configuration Fuses.

### TABLE 4-36: REFERENCE CLOCK REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
REFOCON	074E	ROON	_	ROSSLP	ROSEL		RODI	V<3:0>		_	—		-	-	-		—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	_	PPST3	PPST2	PPST1	PPST0
bit 7							bit 0

#### REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER

Legend:										
R = Readable bit		W = Writable bit	U = Unimplemented bit, read as '0'							
-n = Value a	at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown						
bit 15-4	Unimple	mented: Read as '0'								
bit 3 PPST		PST3: DMA Channel 3 Ping-Pong Mode Status Flag bit								
	1 = DMA	STB3 register is selected								
	0 = DMA	STA3 register is selected								
bit 2	PPST2: [	MA Channel 2 Ping-Pong	Mode Status Flag bit							
	1 = DMA	STB2 register is selected								
	0 = DMA	STA2 register is selected								
bit 1	PPST1: [	MA Channel 1 Ping-Pong	Mode Status Flag bit							

- 1 = DMASTB1 register is selected0 = DMASTA1 register is selected
- bit 0 PPST0: DMA Channel 0 Ping-Pong Mode Status Flag bit
  - 1 = DMASTB0 register is selected
    - 0 = DMASTA0 register is selected

#### 11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-17). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

#### FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



#### 11.4.4.1 Virtual Connections

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support virtual (internal) connections to the output of the op amp/ comparator module (see Figure 25-1 in Section 25.0 "Op Amp/Comparator Module"), and the PTG module (see Section 24.0 "Peripheral Trigger Generator (PTG) Module").

In addition, dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support virtual connections to the filtered QEI module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)".

Virtual connections provide a simple way of interperipheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of `b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QEI module allows peripherals to be connected to the QEI digital filter input. To utilize this filter, the QEI module must be enabled and its inputs must be connected to a physical RPn pin. Example 11-2 illustrates how the input capture module can be connected to the QEI digital filter.

# EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QEI1 DIGITAL FILTER INPUT ON PIN 43 OF THE dsPIC33EPXXXMC206 DEVICE

RPINR15 = 0x2500;	/* Connect the QEI1 HOME1 input to RP37 (pin 43) */
RPINR7 = 0x009;	/* Connect the IC1 input to the digital filter on the FHOME1 input */
QEI1IOC = 0x4000;	/* Enable the QEI digital filter */
QEI1CON = 0x8000;	/* Enable the QEI module */

#### 11.7 **Peripheral Pin Select Registers**

#### REGISTER 11-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				INT1R<6:0>			
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	-	—	—	_	—	—
bit 7	•		•	•			bit 0

Legend:
---------

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 14-8 INT1R<6:0>: Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121 0000001 = Input tied to CMP1 0000000 = Input tied to Vss bit 7-0 Unimplemented: Read as '0'

#### REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

- bit 4-0 SYNCSEL<4:0>: Input Source Select for Synchronization and Trigger Operation bits<sup>(4)</sup>
  - 11111 = No Sync or Trigger source for ICx
  - 11110 = Reserved
  - 11101 = Reserved
  - 11100 = CTMU module synchronizes or triggers ICx
  - 11011 = ADC1 module synchronizes or triggers  $ICx^{(5)}$
  - 11010 = CMP3 module synchronizes or triggers  $ICx^{(5)}$
  - $11001 = CMP2 \text{ module synchronizes or triggers ICx}^{(5)}$
  - 11000 = CMP1 module synchronizes or triggers  $ICx^{(5)}$
  - 10111 = Reserved
  - 10110 = Reserved
  - 10101 = Reserved
  - 10100 = Reserved
  - 10011 = IC4 module synchronizes or triggers ICx
  - 10010 = IC3 module synchronizes or triggers ICx
  - 10001 = IC2 module synchronizes or triggers ICx
  - 10000 = IC1 module synchronizes or triggers ICx
  - 01111 = Timer5 synchronizes or triggers ICx
  - 01110 = Timer4 synchronizes or triggers ICx
  - 01101 = Timer3 synchronizes or triggers ICx (default)
  - 01100 = Timer2 synchronizes or triggers ICx
  - 01011 = Timer1 synchronizes or triggers ICx
  - 01010 = PTGOx module synchronizes or triggers  $ICx^{(6)}$
  - 01001 = Reserved
  - 01000 = Reserved
  - 00111 = Reserved
  - 00110 = Reserved
  - 00101 = Reserved
  - 00100 = OC4 module synchronizes or triggers ICx
  - 00011 = OC3 module synchronizes or triggers ICx
  - 00010 = OC2 module synchronizes or triggers ICx
  - 00001 = OC1 module synchronizes or triggers ICx
  - 00000 = No Sync or Trigger source for ICx
- **Note 1:** The IC32 bit in both the Odd and Even IC must be set to enable Cascade mode.
  - 2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
  - **3:** This bit is set by the selected input source (selected by SYNCSEL<4:0> bits). It can be read, set and cleared in software.
  - 4: Do not use the ICx module as its own Sync or Trigger source.
  - 5: This option should only be selected as a trigger source and not as a synchronization source.
  - Each Input Capture x (ICx) module has one PTG input source. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.
     PTGO8 = IC1

PTGO9 = IC2 PTGO10 = IC3 PTGO11 = IC4

# 18.0 SERIAL PERIPHERAL INTERFACE (SPI)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Serial Peripheral Interface (SPI)" (DS70569) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with Motorola<sup>®</sup> SPI and SIOP interfaces. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X device family offers two SPI modules on a single device. These modules, which are designated as SPI1 and SPI2, are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

Note: In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 and SPI2 modules.

The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of the SPI2 module, but results in a lower maximum speed for SPI2. See **Section 30.0** "**Electrical Characteristics**" for more information.

The SPIx serial interface consists of four pins, as follows:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- SSx/FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, SSx is not used. In 2-pin mode, neither SDOx nor SSx is used.

Figure 18-1 illustrates the block diagram of the SPIx module in Standard and Enhanced modes.

### REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2 (CONTINUED)

bit 1	BUFM: Buffer Fill Mode Select bit				
	<ul> <li>1 = Starts the buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on next interrupt</li> <li>0 = Always starts filling the buffer from the start address.</li> </ul>				
bit 0	ALTS: Alternate Input Sample Mode Select bit				

1 = Uses channel input selects for Sample MUXA on first sample and Sample MUXB on next sample 0 = Always uses channel input selects for Sample MUXA

#### REGISTER 23-5: AD1CHS123: ADC1 INPUT CHANNEL 1, 2, 3 SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CH123NB1	CH123NB0	CH123SB
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0

0-0	0-0	0-0	0-0	U-0 R/W-0 R/W-U		R/W-0	R/W-0
—	—	—	—	—	CH123NA1	CH123NA0	CH123SA
bit 7							bit 0

# Legend:

Legenu.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 Unimplemented: Read as '0'

bit 10-9

CH123NB<1:0>: Channel 1, 2, 3 Negative Input Select for Sample MUXB bits

In 12-bit mode (AD21B = 1), CH123NB is Unimplemented and is Read as '0':

Value	ADC Channel					
	CH1	CH2	CH3			
11	AN9	AN10	AN11			
10 <b>(1,2)</b>	OA3/AN6	AN7	AN8			
0x	VREFL	VREFL	VREFL			

bit 8 **CH123SB:** Channel 1, 2, 3 Positive Input Select for Sample MUXB bit In 12-bit mode (AD21B = 1), CH123SB is Unimplemented and is Read as '0':

Value	ADC Channel					
value	CH1	CH2	СНЗ			
1 <b>(2)</b>	OA1/AN3	OA2/AN0	OA3/AN6			
0 <b>(1,2)</b>	OA2/AN0	AN1	AN2			

bit 7-3 Unimplemented: Read as '0'

bit 2-1 **CH123NA<1:0>:** Channel 1, 2, 3 Negative Input Select for Sample MUXA bits In 12-bit mode (AD21B = 1), CH123NA is Unimplemented and is Read as '<u>0</u>':

Value	ADC Channel						
	CH1	CH2	CH3				
11	AN9	AN10	AN11				
10 <b>(1,2)</b>	OA3/AN6	AN7	AN8				
0x	VREFL	VREFL	VREFL				

- **Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.
  - 2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

REGISTER 24-6:	PTGSDLIM: PTG STEP DELAY LIMIT REGISTER <sup>(1,2)</sup>

					· · · · · · · · · · · · · · · · · · ·		· · · · · · · · · · · · · · · · · · ·
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGSD	LIM<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGSD	)LIM<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			it	U = Unimplemented bit, read as '0'			
-n = Value at POR		'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 **PTGSDLIM<15:0>:** PTG Step Delay Limit Register bits Holds a PTG Step delay value representing the number of additional PTG clocks between the start of a Step command and the completion of a Step command.

**Note 1:** A base Step delay of one PTG clock is added to any value written to the PTGSDLIM register (Step Delay = (PTGSDLIM) + 1).

2: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

## REGISTER 24-7: PTGC0LIM: PTG COUNTER 0 LIMIT REGISTER<sup>(1)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC0	LIM<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC	)LIM<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		pit	U = Unimplemented bit, read as '0'				
-n = Value at F	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkı	nown	

bit 15-0 **PTGC0LIM<15:0>:** PTG Counter 0 Limit Register bits May be used to specify the loop count for the PTGJMPC0 Step command or as a limit register for the General Purpose Counter 0.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

#### REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER (CONTINUED)

- bit 3-0 SELSRCA<3:0>: Mask A Input Select bits
  - 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved 0101 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H 0000 = PWM1L

### 27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

TABLE 27-3:USER ID WORDS REGISTER<br/>MAP

File Name	Address	Bits 23-16	Bits 15-0
FUID0	0x800FF8	—	UID0
FUID1	0x800FFA	—	UID1
FUID2	0x800FFC	—	UID2
FUID3	0x800FFE	—	UID3

**Legend:** — = unimplemented, read as '1'.

## 27.3 On-Chip Voltage Regulator

All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family incorporate an onchip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in **Section 30.0 "Electrical Characteristics"**.

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

#### FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE

REGULATOR<sup>(1,2,3)</sup>



# 27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 30-22 of **Section 30.0 "Electrical Characteristics"** for specific TFSCM values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

AC CHARACTERISTICS			Standard Oper (unless otherw Operating temp	ating Co vise stat perature	onditions: 3.0V ed) -40°C ≤ TA ≤ + -40°C ≤ TA ≤ +	to 3.6V -85°C foi -125°C fo	r Industrial pr Extended	
Param No.	Symbol	Characteristic <sup>(1)</sup>		Min.	Тур.	Max.	Units	Conditions
ТВ10	TtxH	TxCK High Time	Synchronous mode	Greater of: 20 or (TcY + 20)/N		_	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB11	TtxL	TxCK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB15	TtxP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N		_	ns	N = prescale value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40		1.75 Tcy + 40	ns	

TABLE 30-24:	TIMER2 AND TI	MER4 (TYPE B TIM	ER) EXTERNAL CLOC	K TIMING REQUIREMENTS
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Note 1: These parameters are characterized, but are not tested in manufacturing.

### TABLE 30-25: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic <sup>(1)</sup>		Min.	Тур.	Max.	Units	Conditions
TC10	TtxH	TxCK High Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC11	TtxL	TxCK Low Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC15	TtxP	TxCK Input Period	Synchronous, with prescaler	2 Tcy + 40	—	_	ns	N = prescale value (1, 8, 64, 256)
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40		1.75 Tcy + 40	ns	

**Note 1:** These parameters are characterized, but are not tested in manufacturing.



#### FIGURE 30-12: QEA/QEB INPUT CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

### TABLE 30-31: QUADRATURE DECODER TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Тур. <sup>(2)</sup>	Max.	Units	Conditions	
TQ30	TQUL	Quadrature Input Low Time	6 Tcy		ns		
TQ31	ΤουΗ	Quadrature Input High Time	6 Tcy	—	ns		
TQ35	ΤουΙΝ	Quadrature Input Period	12 Tcy	—	ns		
TQ36	ΤουΡ	Quadrature Phase Period	3 Tcy	—	ns		
TQ40	TQUFL	Filter Time to Recognize Low, with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 <b>(Note 3)</b>	
TQ41	TQUFH	Filter Time to Recognize High, with Digital Filter	3 * N * Tcy		ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 <b>(Note 3)</b>	

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: N = Index Channel Digital Filter Clock Divide Select bits. Refer to "Quadrature Encoder Interface (QEI)" (DS70601) in the "*dsPIC33/PIC24 Family Reference Manual*". Please see the Microchip web site for the latest family reference manual sections.



#### FIGURE 30-34: ECAN<sub>x</sub> MODULE I/O TIMING CHARACTERISTICS

#### TABLE 30-51: ECANx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min. Typ. <sup>(2)</sup> Max. Units Condition		Conditions		
CA10	TIOF	Port Output Fall Time		_	_	ns	See Parameter DO32
CA11	TIOR	Port Output Rise Time	_	_	_	ns	See Parameter DO31
CA20	TCWF	Pulse Width to Trigger CAN Wake-up Filter	120			ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

#### **FIGURE 30-35: UARTX MODULE I/O TIMING CHARACTERISTICS**



#### TABLE 30-52: UARTX MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min.	Тур. <sup>(2)</sup>	Max.	Units	Conditions
UA10	TUABAUD	UARTx Baud Time	66.67	_	_	ns	
UA11	FBAUD	UARTx Baud Frequency	—	—	15	Mbps	
UA20	TCWF	Start Bit Pulse Width to Trigger UARTx Wake-up	500	_	_	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.



#### FIGURE 30-36: ADC CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)

Section Name	Update Description
Section 30.0 "Electrical Characteristics"	<ul> <li>Throughout: qualifies all footnotes relating to the operation of analog modules below VDDMIN (replaces "will have" with "may have")</li> </ul>
	<ul> <li>Throughout: changes all references of SPI timing parameter symbol "TscP" to "FscP"</li> <li>Table 30-1: changes VDD range to 3.0V to 3.6V</li> </ul>
	Table 30-4: removes Parameter DC12 (RAM Retention Voltage)
	<ul> <li>Table 30-7: updates Maximum values at 10 and 20 MIPS</li> </ul>
	<ul> <li>Table 30-8: adds Maximum IPD values, and removes all ∆IWDT entries</li> </ul>
	<ul> <li>Adds new Table 30-9 (Watchdog Timer Delta Current) with consolidated values removed from Table 30-8. All subsequent tables are renumbered accordingly.</li> </ul>
	Table 30-10: adds footnote for all parameters for 1:2 Doze ratio     Table 30-11:
	- changes Minimum and Maximum values for D120 and D130
	<ul> <li>adds Minimum and Maximum values for D131</li> </ul>
	<ul> <li>adds Minimum and Maximum values for D150 through D156, and removes Typical values</li> </ul>
	• Table 30-12:
	- reformats table for readability
	- changes IoL conditions for DO10
	Table 30-14: adds foothote to D135     Table 30-17: changes Minimum and Maximum values for OS20
	Table 30-19:     Table 30-19:
	- splits temperature range and adds new values for F20a
	<ul> <li>reduces temperature range for F20b to extended temperatures only</li> </ul>
	• Table 30-20:
	<ul> <li>splits temperature range and adds new values for F21a</li> </ul>
	<ul> <li>reduces temperature range for F20b to extended temperatures only</li> </ul>
	Iable 30-53:
	- adds footnote ("Parameter characterized") to multiple parameters
	<ul> <li>Table 30-55: adds Minimum and Maximum values for all CTMUI specifications, and removes Typical values</li> </ul>
	<ul> <li>Table 30-57: adds new footnote to AD09</li> <li>Table 30-58:</li> </ul>
	<ul> <li>removes all specifications for accuracy with external voltage references</li> <li>removes Typical values for AD23a and AD24a</li> </ul>
	<ul> <li>replaces Minimum and Maximum values for AD21a, AD22a, AD23a and AD24a with new values, split by Industrial and Extended temperatures</li> </ul>
	- removes Maximum value of AD30
	- removes Minimum values from AD31a and AD32a
	- adds of changes Typical values for AD30, AD31a, AD32a and AD33a • Table 30-50
	<ul> <li>removes all specifications for accuracy with external voltage references</li> </ul>
	<ul> <li>removes Maximum value of AD30</li> </ul>
	<ul> <li>removes Typical values for AD23b and AD24b</li> </ul>
	- replaces Minimum and Maximum values for AD21b, AD22b, AD23b and AD24b
	with new values, split by Industrial and Extended temperatures
	<ul> <li>removes withintum and waximum values from AD310, AD320, AD330 and AD340</li> <li>adds or changes Typical values for AD30, AD31a, AD32a and AD33a</li> </ul>
	Table 30-61: Adds footnote to AD51
Section 32.0 "DC and AC	Updates Figure 32-6 (Typical IDD @ 3.3V) with individual current vs. processor speed
Device Characteristics	curves for the different program memory sizes
Graphs"	
Section 33.0 "Packaging	• Replaces drawing C04-149C (64-pin QFN, 7.15 x 7.15 exposed pad) with C04-154A
Information"	(64-pin QFN, 5.4 x 5.4 exposed pad)

### TABLE A-5: MAJOR SECTION UPDATES (CONTINUED)