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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64mc502t-e-mm

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REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)

- bit 3 SPI1MD: SPI1 Module Disable bit 1 = SPI1 module is disabled
 - 0 = SPI1 module is enabled
- bit 2 Unimplemented: Read as '0'
- bit 1 C1MD: ECAN1 Module Disable bit⁽²⁾ 1 = ECAN1 module is disabled 0 = ECAN1 module is enabled
- bit 0 AD1MD: ADC1 Module Disable bit 1 = ADC1 module is disabled 0 = ADC1 module is enabled
- Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
 - 2: This bit is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment	Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
000 0000	I	Vss	010 1101	I	RPI45
000 0001	I	C1OUT ⁽¹⁾	010 1110	I	RPI46
000 0010	I	C2OUT ⁽¹⁾	010 1111	I	RPI47
000 0011	I	C3OUT ⁽¹⁾	011 0000	_	_
000 0100	I	C4OUT ⁽¹⁾	011 0001		—
000 0101	_	_	011 0010		_
000 0110	I	PTGO30 ⁽¹⁾	011 0011	I	RPI51
000 0111	I	PTGO31 ⁽¹⁾	011 0100	I	RPI52
000 1000	I	FINDX1 ^(1,2)	011 0101	I	RPI53
000 1001	I	FHOME1 ^(1,2)	011 0110	I/O	RP54
000 1010	—	—	011 0111	I/O	RP55
000 1011	_	—	011 1000	I/O	RP56
000 1100	_	—	011 1001	I/O	RP57
000 1101		—	011 1010	I	RPI58
000 1110	_	—	011 1011	—	—
000 1111	_	—	011 1100	_	—
001 0000		—	011 1101		—
001 0001		_	011 1110	_	_
001 0010		_	011 1111	—	_
001 0011		—	100 0000		—
001 0100	I/O	RP20	100 0001	_	—
001 0101	_	—	100 0010	_	—
001 0110	—	—	100 0011	—	_
001 0111	—	—	100 0100	_	—
001 1000	I	RPI24	100 0101	—	—
001 1001	I	RPI25	100 0110	—	—
001 1010			100 0111		—
001 1011	I	RPI27	100 1000	_	—
001 1100	I	RPI28	100 1001	—	—
001 1101	—	—	100 1010	_	—
001 1110	_	—	100 1011	_	—
001 1111	—	—	100 1100	—	—
010 0000	I	RPI32	100 1101		—
010 0001	I	RPI33	100 1110	_	—
010 0010	I	RPI34	100 1111	—	—
010 0011	I/O	RP35	101 0000		
010 0100	I/O	RP36	101 0001	_	_
010 0101	I/O	RP37	101 0010	—	—
010 0110	I/O	RP38	101 0011		—
010 0111	I/O	RP39	101 0100	_	—

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Legend: Shaded rows indicate PPS Input register values that are unimplemented.

Note 1: See Section 11.4.4.1 "Virtual Connections" for more information on selecting this pin assignment.

2: These inputs are available on dsPIC33EPXXXGP/MC50X devices only.

REGISTER 11-7: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
_				FLT2R<6:0>						
bit 15							bit 8			
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
				FLT1R<6:0>						
bit 7							bit 0			
Legend:										
R = Readab	ole bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'				
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown			
bit 15	Unimpleme	ented: Read as '	0'							
bit 14-8	FLT2R<6:0: (see Table 1	Assign PWM 1-2 for input pin	Fault 2 (FLT2 selection nur) to the Corresp mbers)	onding RPn F	Pin bits				
	1111001 =	Input tied to RPI	121							
	•									
	•									
	0000001 =	Input tied to CM	P1							
	0000000 =	0000000 = Input tied to Vss								
bit 7	Unimpleme	ented: Read as '	0'							
bit 6-0	FLT1R<6:0: (see Table 1	Second States	Fault 1 (FLT1 selection nur) to the Corresp nbers)	onding RPn F	Pin bits				
	1111001 =	Input tied to RPI	121							
	•									
	-									
		Input tied to CM	P1							
	0000000 =	Input tied to Vss	; ;							

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	—			RP57	R<5:0>				
bit 15							bit 8		
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	—			RP56	R<5:0>				
bit 7							bit 0		
Legend:									
R = Readab	le bit	W = Writable	bit	U = Unimplem	nented bit, rea	d as '0'			
-n = Value a	t POR	'1' = Bit is set	t	'0' = Bit is clea	ared	x = Bit is unkr	nown		
bit 15-14	Unimpleme	nted: Read as '	0'						
bit 13-8	RP57R<5:0> (see Table 1 [*]	RP57R<5:0>: Peripheral Output Function is Assigned to RP57 Output Pin bits (see Table 11-3 for peripheral function numbers)							
bit 7-6	Unimpleme	Unimplemented: Read as '0'							

REGISTER 11-24: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

(see Table	11-3 for peripheral function numbers)	

REGISTER 11-25: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—		RP97R<5:0>					
bit 15							bit 8	

RP56R<5:0>: Peripheral Output Function is Assigned to RP56 Output Pin bits

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

bit 13-8 **RP97R<5:0>:** Peripheral Output Function is Assigned to RP97 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-0 Unimplemented: Read as '0'

bit 5-0

12.2 Timer1 Control Register

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON ⁽¹⁾	—	TSIDL	—	_	—	—	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	TCKPS1	TCKPS0	_	TSYNC ⁽¹⁾	TCS ⁽¹⁾	—
bit 7							bit 0
Legend:							
R = Readab	ole bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own
		(4)					
bit 15	TON: Timer1	On bit ⁽¹⁾					
	1 = Starts 16-	bit Limer1 bit Timer1					
bit 1/	Unimplement	ted: Pead as '	ı'				
bit 13		1 Stop in Idle N	/ode hit				
DIC 15	1 = Discontinu	i stop in lae k	eration when a	device enters l	dle mode		
	0 = Continues	module opera	tion in Idle mo	ode			
bit 12-7	Unimplement	ted: Read as ')'				
bit 6	TGATE: Time	r1 Gated Time	Accumulation	Enable bit			
	When TCS =	<u>1:</u> prod					
	When TCS =	0. 0.					
	1 = Gated tim	<u>e</u> accumulatior	n is enabled				
	0 = Gated tim	e accumulatior	n is disabled				
bit 5-4	TCKPS<1:0>	: Timer1 Input	Clock Prescal	e Select bits			
	11 = 1:256						
	10 = 1:64 01 = 1:8						
	01 = 1.0 00 = 1.1						
bit 3	Unimplement	ted: Read as ')'				
bit 2	TSYNC: Time	er1 External Clo	ock Input Sync	chronization Se	elect bit ⁽¹⁾		
	When TCS =	1:					
	1 = Synchroni	izes external cl	ock input				
	0 = Does not	synchronize ex	ternal clock in	nput			
	This bit is jand	<u>ored</u> .					
bit 1	TCS: Timer1 (Clock Source S	Select bit ⁽¹⁾				
	1 = External c	lock is from pir	n, T1CK (on th	ne rising edge)			
	0 = Internal cl	ock (FP)		5 5-7			
bit 0	Unimplement	ted: Read as ')'				
Note 1: \	When Timer1 is en attempts by user so	abled in Exterr oftware to write	al Synchrono to the TMR1	us Counter mo register are ig	ode (TCS = 1, T nored.	SYNC = 1, TO	N = 1), any

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

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REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)

bit 6-4	SYNCSRC<2:0>: Synchronous Source Selection bits ⁽¹⁾ 111 = Reserved
	•
	• 100 = Reserved 011 = PTGO17 ⁽²⁾ 010 = PTGO16 ⁽²⁾ 001 = Reserved 000 = SYNCI1 input from PPS
bit 3-0	<pre>SEVTPS<3:0>: PWMx Special Event Trigger Output Postscaler Select bits⁽¹⁾ 1111 = 1:16 Postscaler generates Special Event Trigger on every sixteenth compare match event</pre>
	0001 = 1:2 Postscaler generates Special Event Trigger on every second compare match event 0000 = 1:1 Postscaler generates Special Event Trigger on every compare match event

- **Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.
 - 2: See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

REGISTER 16-2: PTCON2: PWMx PRIMARY MASTER CLOCK DIVIDER SELECT REGISTER
--

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
—	—	—	_	_	—	—	—	
bit 15							bit 8	
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
	_	—	—	—	PCLKDIV2 ⁽¹⁾	PCLKDIV1 ⁽¹⁾	PCLKDIV0(1)	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1'		'1' = Bit is set	'1' = Bit is set		ared	x = Bit is unknown		
hit 15.2 Unimplemented, Road as '0'								

bit 15-3 Unimplemented: Read as '0'

bit 2-0 PCLKDIV<2:0>: PWMx Input Clock Prescaler (Divider) Select bits⁽¹⁾

- 111 = Reserved 110 = Divide-by-64 101 = Divide-by-32
- 100 = Divide-by-32100 = Divide-by-16
- 011 = Divide-by-8
- 010 = Divide-by-4
- 001 = Divide-by-2
- 000 = Divide-by-1, maximum PWMx timing resolution (power-on default)
- **Note 1:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.



FIGURE 18-1: SPIX MODULE BLOCK DIAGRAM

19.0 INTER-INTEGRATED CIRCUIT[™] (I²C[™])

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Inter-Integrated Circuit™ (I²C™)" (DS70330) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.
 - 3: There are minimum bit rates of approximately FCY/512. As a result, high processor speeds may not support 100 Kbit/second operation. See timing specifications, IM10 and IM11, and the "Baud Rate Generator" in the "dsPIC33/PIC24 Family Reference Manual".

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X family of devices contains two Inter-Integrated Circuit (I²C) modules: I2C1 and I2C2.

The l^2C module provides complete hardware support for both Slave and Multi-Master modes of the l^2C serial communication standard, with a 16-bit interface.

The I^2C module has a 2-pin interface:

- · The SCLx pin is clock
- The SDAx pin is data

The I²C module offers the following key features:

- I²C interface supporting both Master and Slave modes of operation
- I²C Slave mode supports 7 and 10-bit addressing
- I²C Master mode supports 7 and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation, detects bus collision and arbitrates accordingly
- Intelligent Platform Management Interface (IPMI)
 support
- System Management Bus (SMBus) support

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	_	—	—	BCL	GCSTAT	ADD10
bit 15							bit 8
R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF
bit 7							bit 0
Legend:		C = Clearab	le bit	HS = Hardwa	re Settable bit	HSC = Hardware S	ettable/Clearable bit
R = Readabl	e bit	W = Writable	e bit	U = Unimplemented bit, read as '0'			
-n = Value at	POR	'1' = Bit is se	et	'0' = Bit is clea	ared	x = Bit is unknown	

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

bit 15	ACKSTAT: Acknowledge Status bit (when operating as I^2C^{TM} master, applicable to master transmit operation)
	1 = NACK received from slave 0 = ACK received from slave
	Hardware is set or clear at the end of slave Acknowledge.
bit 14	TRSTAT: Transmit Status bit (when operating as I^2C master, applicable to master transmit operation) 1 = Master transmit is in progress (8 bits + ACK)
	0 = Master transmit is not in progress Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
bit 13-11	Unimplemented: Read as '0'
bit 10	BCL: Master Bus Collision Detect bit
	1 = A bus collision has been detected during a master operation0 = No bus collision detected
	Hardware is set at detection of a bus collision.
bit 9	GCSTAT: General Call Status bit
	1 = General call address was received
	0 = General call address was not received
1.1.0	Hardware is set when address matches general call address. Hardware is clear at Stop detection.
DIT 8	ADD10: 10-Bit Address Status bit
	I = 10-bit address was matched 0 = 10-bit address was not matched
	Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
bit 7	IWCOL: I2Cx Write Collision Detect bit
~	1 = An attempt to write to the I2CxTRN register failed because the I^2 C module is busy 0 = No collision
	Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
bit 6	I2COV: I2Cx Receive Overflow Flag bit
	 1 = A byte was received while the I2CxRCV register was still holding the previous byte 0 = No overflow
	Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
bit 5	D_A: Data/Address bit (when operating as I ² C slave)
	1 = Indicates that the last byte received was data
	 Indicates that the last byte received was a device address Hardware is clear at a device address match. Hardware is set by reception of a slave byte.
bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware is set or clear when a Start, Repeated Start or Stop is detected.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
_	—	ТХВО	TXBP	RXBP	TXWAR	RXWAR	EWARN
bit 15							bit 8
R/C-0	R/C-0	R/C-0	U-0	R/C-0	R/C-0	R/C-0	R/C-0
IVRIF	WAKIF	ERRIF	_	FIFOIF	RBOVIF	RBIF	TBIF
bit 7							bit 0
Legend:		C = Writable b	oit, but only '0'	can be writter	n to clear the bit		
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							

'0' = Bit is cleared

x = Bit is unknown

REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER

'1' = Bit is set

bit 15-14	Unimplemented: Read as '0'
bit 13	TXBO: Transmitter in Error State Bus Off bit
	1 = Transmitter is in Bus Off state
	0 = Transmitter is not in Bus Off state
bit 12	TXBP: Transmitter in Error State Bus Passive bit
	1 = Transmitter is in Bus Passive state
	0 = Transmitter is not in Bus Passive state
bit 11	RXBP: Receiver in Error State Bus Passive bit
	1 = Receiver is in Bus Passive state
h:+ 40	0 = Receiver is not in Bus Passive state
Dit 10	IXWAR: Transmitter in Error State Warning bit
	1 = Transmitter is in Error Warning state
hit 0	BYWAB: Deceiver in Error State Warning bit
bit 9	1 - Receiver is in Error Warning state
	0 = Receiver is not in Error Warning state
bit 8	EWARN: Transmitter or Receiver in Error State Warning bit
	1 = Transmitter or receiver is in Error Warning state
	0 = Transmitter or receiver is not in Error Warning state
bit 7	IVRIF: Invalid Message Interrupt Flag bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 6	WAKIF: Bus Wake-up Activity Interrupt Flag bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 5	ERRIF: Error Interrupt Flag bit (multiple sources in CxINTF<13:8>)
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 4	Unimplemented: Read as '0'
bit 3	FIFOIF: FIFO Almost Full Interrupt Flag bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 2	RBOVIF: RX Buffer Overflow Interrupt Flag bit
	1 = Interrupt request has occurred
	v = merupi request has not occurred

-n = Value at POR

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0
bit 7	·					•	bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimplei	mented bit, read	d as '0'	
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown				nown			

REGISTER 23-8: AD1CSSL: ADC1 INPUT SCAN SELECT REGISTER LOW^(1,2)

bit 15-0 CSS<15:0>: ADC1 Input Scan Selection bits

1 = Selects ANx for input scan

0 = Skips ANx for input scan

Note 1: On devices with less than 16 analog inputs, all AD1CSSL bits can be selected by the user. However, inputs selected for scan, without a corresponding input on the device, convert VREFL.

2: CSSx = ANx, where x = 0-15.

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
53	NEG	NEG	Acc(1)	Negate Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		NEG	f	$f = \overline{f} + 1$	1	1	C,DC,N,OV,Z
		NEG	f,WREG	WREG = \overline{f} + 1	1	1	C,DC,N,OV,Z
		NEG	Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
54	NOP	NOP		No Operation	1	1	None
		NOPR		No Operation 1 1			None
55	POP	POP	f	Pop f from Top-of-Stack (TOS)	1	1	None
		POP	Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
		POP.D	Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)	1	2	None
		POP.S		Pop Shadow Registers	1	1	All
56	PUSH	PUSH	f	Push f to Top-of-Stack (TOS)	1	1	None
		PUSH	Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
		PUSH.D	Wns	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None
		PUSH.S		Push Shadow Registers	1	1	None
57	PWRSAV	PWRSAV	#lit1	Go into Sleep or Idle mode	1	1	WDTO,Sleep
58	RCALL	RCALL	Expr	Relative Call	1	4	SFA
		RCALL	Wn	Computed Call	1	4	SFA
59	REPEAT	REPEAT	#lit15	Repeat Next Instruction lit15 + 1 times	1	1	None
		REPEAT	Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
60	RESET	RESET		Software device Reset	1	1	None
61	RETFIE	RETFIE		Return from interrupt	1	6 (5)	SFA
62	RETLW	RETLW	#lit10,Wn	Return with literal in Wn	1	6 (5)	SFA
63	RETURN	RETURN		Return from Subroutine	1	6 (5)	SFA
64	RLC	RLC	f	f = Rotate Left through Carry f	1	1	C,N,Z
		RLC	f,WREG	WREG = Rotate Left through Carry f	1	1	C,N,Z
		RLC	Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C,N,Z
65	RLNC	RLNC	f	f = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	f,WREG	WREG = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N,Z
66	RRC	RRC	f	f = Rotate Right through Carry f	1	1	C,N,Z
		RRC	f,WREG	WREG = Rotate Right through Carry f	1	1	C,N,Z
07		RRC	Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C,N,Z
67	RRNC	RRNC	f	f = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	Í,WREG	WREG = Rotate Right (No Carry) f	1	1	N,Z
<u></u>		RRNC	Ws, Wd	Wd = Rotate Right (No Carry) Ws	1	1	N,Z
68	SAC	SAC	Acc, #Slit4, Wdo''	Store Accumulator	1	1	None
60	0.77	SAC.R	Acc, #SIIL4, Wdo',	Wed = sign extended We	1	1	
70	OFTM	SE	ws; wha		1	1	C,N,Z
10	STITI	OF TM	L WRFC		1	1	None
		GETM	WC	We = 0xFFFF	1	1	None
71	SFTAC	SFTAC	Acc, Wn ⁽¹⁾	Arithmetic Shift Accumulator by (Wn)	1	1	OA,OB,OAB, SA SB SAB
		SFTAC	Acc,#Slit6 ⁽¹⁾	Arithmetic Shift Accumulator by Slit6	1	1	OA,OB,OAB,

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

29.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- Command-line interface
- · Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

29.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline
 assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

29.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

29.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- · Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- · Command-line interface
- · Rich directive set
- Flexible macro language
- · MPLAB X IDE compatibility

DC CH	ARACTE	RISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions	
DI60a	licl	Input Low Injection Current	0	_	₋₅ (4,7)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP and RB7	
DI60b	Іісн	Input High Injection Current	0	_	+5 ^(5,6,7)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB7 and all 5V tolerant pins ⁽⁶⁾	
DI60c	∑lict	Total Input Injection Current (sum of all I/O and control pins)	-20 ⁽⁸⁾	_	+20(8)	mA	Absolute instantaneous sum of all \pm input injection cur- rents from all I/O pins (IICL + IICH) $\leq \sum$ IICT	

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

2: Negative current is defined as current sourced by the pin.

3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.

4: VIL source < (Vss – 0.3). Characterized but not tested.

5: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

FIGURE 30-7: OUTPUT COMPARE x MODULE (OCx) TIMING CHARACTERISTICS



TABLE 30-27: OUTPUT COMPARE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic ⁽¹⁾	Min. Typ. Max. Units Conditions					
OC10	TccF	OCx Output Fall Time	—			ns	See Parameter DO32	
OC11	TccR	OCx Output Rise Time	— — ns See Parameter DO31				See Parameter DO31	

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-8: OCx/PWMx MODULE TIMING CHARACTERISTICS



TABLE 30-28: OCx/PWMx MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic ⁽¹⁾	Min. Typ. Max. Units Conditions					
OC15	TFD	Fault Input to PWMx I/O Change	—	_	Tcy + 20	ns		
OC20	TFLT	Fault Input Pulse Width	Tcy + 20	_	—	ns		

Note 1: These parameters are characterized but not tested in manufacturing.



FIGURE 30-13: QEI MODULE INDEX PULSE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

TABLE 30-32: QEI INDEX PULSE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHA	RACTERI	STICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic ⁽¹⁾	Min. Max. Units Conditions				
TQ50	TqiL	Filter Time to Recognize Low, with Digital Filter	3 * N * Tcy	_	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)	
TQ51	TqiH	Filter Time to Recognize High, with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)	
TQ55	Tqidxr	Index Pulse Recognized to Position Counter Reset (ungated index)	3 TCY	—	ns		

Note 1: These parameters are characterized but not tested in manufacturing.

2: Alignment of index pulses to QEA and QEB is shown for position counter Reset timing only. Shown for forward direction only (QEA leads QEB). Same timing applies for reverse direction (QEA lags QEB) but index pulse recognition occurs on the falling edge.

AC CHARA	CTERISTICS		$\begin{tabular}{lllllllllllllllllllllllllllllllllll$						
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	СКР	SMP			
15 MHz	Table 30-42			0,1	0,1	0,1			
10 MHz	—	Table 30-43	—	1	0,1	1			
10 MHz	—	Table 30-44	—	0	0,1	1			
15 MHz	—	—	Table 30-45	1	0	0			
11 MHz	—	—	Table 30-46	1	1	0			
15 MHz	_	_	Table 30-47	0	1	0			
11 MHz	_	_	Table 30-48	0	0	0			

TABLE 30-41: SPI1 MAXIMUM DATA/CLOCK RATE SUMMARY

FIGURE 30-22: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS













