

Welcome to [E-XFL.COM](#)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

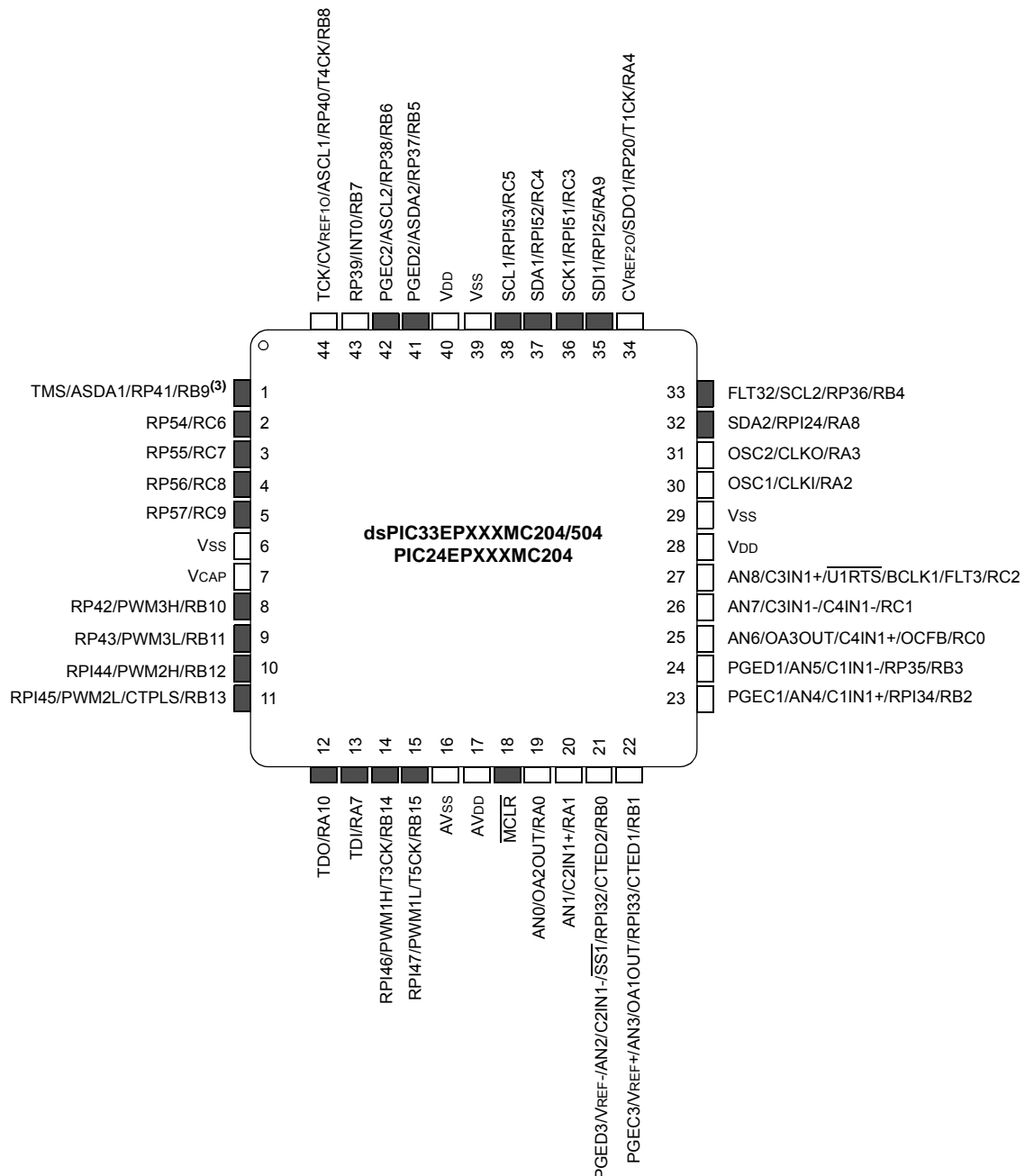
#### Details

Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64mc503t-e-tl">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64mc503t-e-tl</a>

## Pin Diagrams (Continued)

44-Pin TQFP<sup>(1,2)</sup>

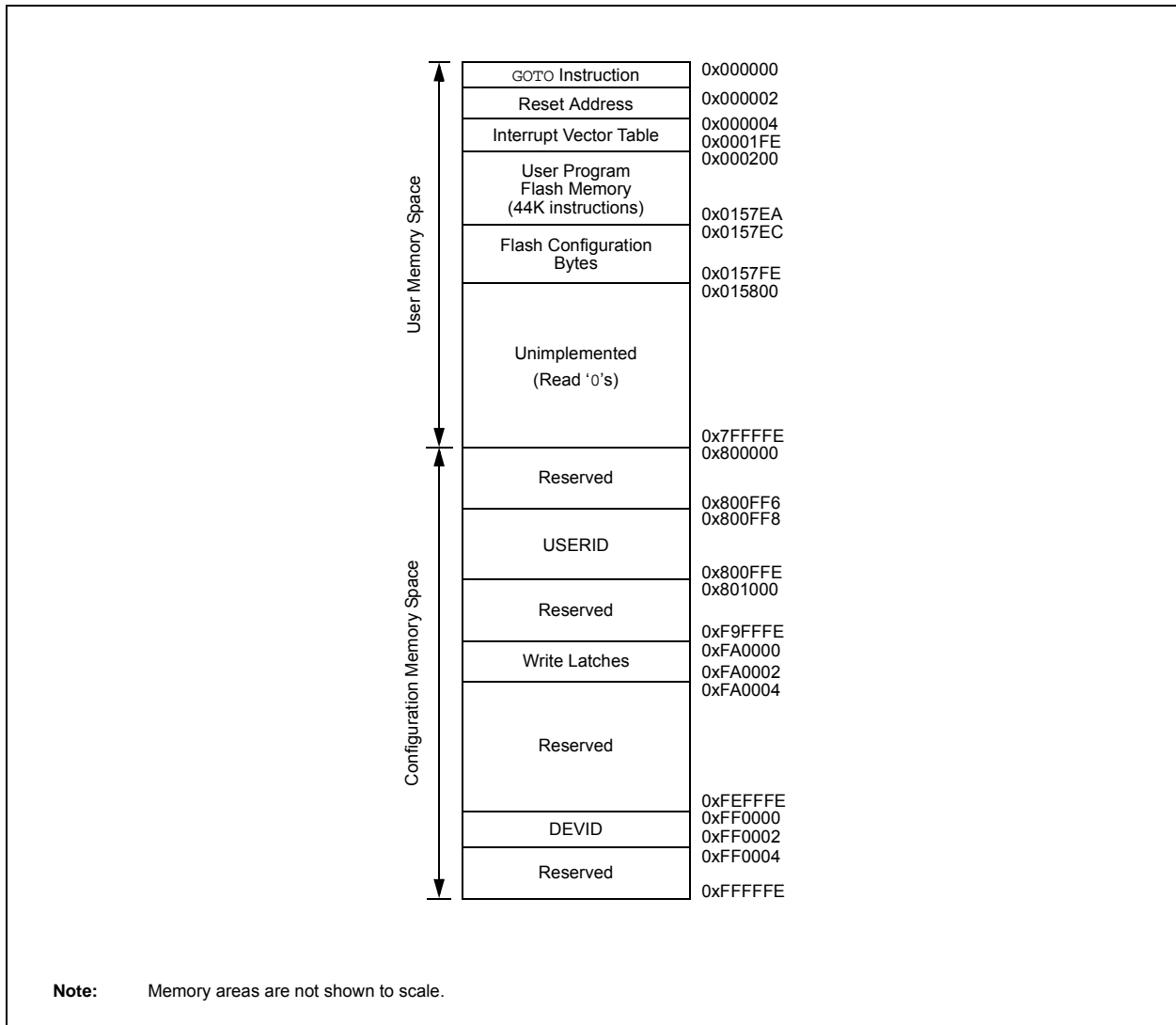
■ = Pins are up to 5V tolerant



- Note**
- 1: The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
  - 2: Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
  - 3: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.



**FIGURE 4-3: PROGRAM MEMORY MAP FOR dsPIC33EP128GP50X, dsPIC33EP128MC20X/50X AND PIC24EP128GP/MC20X DEVICES**



**TABLE 4-14: PWM GENERATOR 2 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
PWMCON2	0C40	FLTSTAT	CLSTAT	TRGSTAT	FLTIE	CLIE	TRGIE	ITB	MDCS	DTC<1:0>		DTCP	—	MTBS	CAM	XPRES	IUE	0000	
IOCON2	0C42	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	C000	
FCLCON2	0C44	—	CLSRC<4:0>					CLPOL	CLMOD	FLTSRC<4:0>					FLTPOL	FLTMOD<1:0>		00F8	
PDC2	0C46	PDC2<15:0>																	0000
PHASE2	0C48	PHASE2<15:0>																	0000
DTR2	0C4A	—	—	DTR2<13:0>														0000	
ALTDTR2	0C4C	—	—	ALTDTR2<13:0>														0000	
TRIG2	0C52	TRGCMPL<15:0>																	0000
TRGCON2	0C54	TRGDIV<3:0>				—	—	—	—	—	—	TRGSTRT<5:0>							0000
LEBCON2	0C5A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000	
LEBDLY2	0C5C	—	—	—	—	LEB<11:0>												0000	
AUXCON2	0C5E	—	—	—	—	BLANKSEL<3:0>				—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000	

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-15: PWM GENERATOR 3 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
PWMCON3	0C60	FLTSTAT	CLSTAT	TRGSTAT	FLTIE	CLIE	TRGIE	ITB	MDCS	DTC<1:0>		DTCP	—	MTBS	CAM	XPRES	IUE	0000	
IOCON3	0C62	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	C000	
FCLCON3	0C64	—	CLSRC<4:0>					CLPOL	CLMOD	FLTSRC<4:0>					FLTPOL	FLTMOD<1:0>			00F8
PDC3	0C66	PDC3<15:0>																	0000
PHASE3	0C68	PHASE3<15:0>																	0000
DTR3	0C6A	—	—	DTR3<13:0>														0000	
ALTDTR3	0C6C	—	—	ALTDTR3<13:0>														0000	
TRIG3	0C72	TRGCMPL<15:0>																	0000
TRGCON3	0C74	TRGDIV<3:0>				—	—	—	—	—	—	TRGSTRT<5:0>							0000
LEBCON3	0C7A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000	
LEBDLY3	0C7C	—	—	—	—	LEB<11:0>												0000	
AUXCON3	0C7E	—	—	—	—	BLANKSEL<3:0>				—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000	

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 8-5: DMAxSTBH: DMA CHANNEL x START ADDRESS REGISTER B (HIGH)**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<23:16>							
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'bit 7-0 **STB<23:16>:** Secondary Start Address bits (source or destination)**REGISTER 8-6: DMAxSTBL: DMA CHANNEL x START ADDRESS REGISTER B (LOW)**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<7:0>							
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **STB<15:0>:** Secondary Start Address bits (source or destination)

**REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INT2R<6:0>						
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **INT2R<6:0>:** Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits  
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

**REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	T2CKR<6:0>							
bit 7								bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **T2CKR<6:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits  
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

**REGISTER 11-5: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC4R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC3R<6:0>						
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC4R<6:0>:** Assign Input Capture 4 (IC4) to the Corresponding RPn Pin bits  
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC3R<6:0>:** Assign Input Capture 3 (IC3) to the Corresponding RPn Pin bits  
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss



## 14.2 Input Capture Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—
bit 15						bit 8	

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	IC11	IC10	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7						bit 0	

<b>Legend:</b>	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture Stop in Idle Control bit  
 1 = Input capture will Halt in CPU Idle mode  
 0 = Input capture will continue to operate in CPU Idle mode

bit 12-10 **ICTSEL<2:0>:** Input Capture Timer Select bits  
 111 = Peripheral clock (FP) is the clock source of the ICx  
 110 = Reserved  
 101 = Reserved  
 100 = T1CLK is the clock source of the ICx (only the synchronous clock is supported)  
 011 = T5CLK is the clock source of the ICx  
 010 = T4CLK is the clock source of the ICx  
 001 = T2CLK is the clock source of the ICx  
 000 = T3CLK is the clock source of the ICx

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **IC1<1:0>:** Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)  
 11 = Interrupt on every fourth capture event  
 10 = Interrupt on every third capture event  
 01 = Interrupt on every second capture event  
 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)  
 1 = Input capture buffer overflow occurred  
 0 = No input capture buffer overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)  
 1 = Input capture buffer is not empty, at least one more capture value can be read  
 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits  
 111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)  
 110 = Unused (module is disabled)  
 101 = Capture mode, every 16th rising edge (Prescaler Capture mode)  
 100 = Capture mode, every 4th rising edge (Prescaler Capture mode)  
 011 = Capture mode, every rising edge (Simple Capture mode)  
 010 = Capture mode, every falling edge (Simple Capture mode)  
 001 = Capture mode, every edge rising and falling (Edge Detect mode (IC1<1:0>) is not used in this mode)  
 000 = Input capture module is turned off

## 16.2 PWM Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

<p><b>Note:</b> In the event you are not able to access the product page using the link above, enter this URL in your browser: <a href="http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464">http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464</a></p>
--

### 16.2.1 KEY RESOURCES

- **“High-Speed PWM”** (DS70645) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

**REGISTER 20-1: UxMODE: UARTx MODE REGISTER (CONTINUED)**

- bit 5      **ABAUD:** Auto-Baud Enable bit  
1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion  
0 = Baud rate measurement is disabled or completed
- bit 4      **URXINV:** UARTx Receive Polarity Inversion bit  
1 = UxRX Idle state is '0'  
0 = UxRX Idle state is '1'
- bit 3      **BRGH:** High Baud Rate Enable bit  
1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode)  
0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
- bit 2-1    **PDSEL<1:0>:** Parity and Data Selection bits  
11 = 9-bit data, no parity  
10 = 8-bit data, odd parity  
01 = 8-bit data, even parity  
00 = 8-bit data, no parity
- bit 0      **STSEL:** Stop Bit Selection bit  
1 = Two Stop bits  
0 = One Stop bit

- Note 1:** Refer to the “**UART**” (DS70582) section in the “*dsPIC33/PIC24 Family Reference Manual*” for information on enabling the UARTx module for receive or transmit operation.
- 2:** This feature is only available for the 16x BRG mode (BRGH = 0).
- 3:** This feature is only available on 44-pin and 64-pin devices.
- 4:** This feature is only available on 64-pin devices.

**REGISTER 21-13: CxBUFPNT2: ECANx FILTER 4-7 BUFFER POINTER REGISTER 2**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP<3:0>				F6BP<3:0>			
bit 15				bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP<3:0>				F4BP<3:0>			
bit 7				bit 0			

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-12      **F7BP<3:0>**: RX Buffer Mask for Filter 7 bits  
1111 = Filter hits received in RX FIFO buffer  
1110 = Filter hits received in RX Buffer 14  
•  
•  
•  
0001 = Filter hits received in RX Buffer 1  
0000 = Filter hits received in RX Buffer 0
- bit 11-8      **F6BP<3:0>**: RX Buffer Mask for Filter 6 bits (same values as bits<15:12>)
- bit 7-4      **F5BP<3:0>**: RX Buffer Mask for Filter 5 bits (same values as bits<15:12>)
- bit 3-0      **F4BP<3:0>**: RX Buffer Mask for Filter 4 bits (same values as bits<15:12>)

**REGISTER 21-14: CxBUFPNT3: ECANx FILTER 8-11 BUFFER POINTER REGISTER 3**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11BP<3:0>				F10BP<3:0>			
bit 15				bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F9BP<3:0>				F8BP<3:0>			
bit 7				bit 0			

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-12      **F11BP<3:0>**: RX Buffer Mask for Filter 11 bits  
1111 = Filter hits received in RX FIFO buffer  
1110 = Filter hits received in RX Buffer 14  
•  
•  
•  
0001 = Filter hits received in RX Buffer 1  
0000 = Filter hits received in RX Buffer 0
- bit 11-8      **F10BP<3:0>**: RX Buffer Mask for Filter 10 bits (same values as bits<15:12>)
- bit 7-4      **F9BP<3:0>**: RX Buffer Mask for Filter 9 bits (same values as bits<15:12>)
- bit 3-0      **F8BP<3:0>**: RX Buffer Mask for Filter 8 bits (same values as bits<15:12>)

**REGISTER 23-1: AD1CON1: ADC1 CONTROL REGISTER 1 (CONTINUED)**

bit 7-5	<p><b>SSRC&lt;2:0&gt;:</b> Sample Trigger Source Select bits</p> <p><u>If SSRCG = 1:</u></p> <p>111 = Reserved</p> <p>110 = PTGO15 primary trigger compare ends sampling and starts conversion<sup>(1)</sup></p> <p>101 = PTGO14 primary trigger compare ends sampling and starts conversion<sup>(1)</sup></p> <p>100 = PTGO13 primary trigger compare ends sampling and starts conversion<sup>(1)</sup></p> <p>011 = PTGO12 primary trigger compare ends sampling and starts conversion<sup>(1)</sup></p> <p>010 = PWM Generator 3 primary trigger compare ends sampling and starts conversion<sup>(2)</sup></p> <p>001 = PWM Generator 2 primary trigger compare ends sampling and starts conversion<sup>(2)</sup></p> <p>000 = PWM Generator 1 primary trigger compare ends sampling and starts conversion<sup>(2)</sup></p> <p><u>If SSRCG = 0:</u></p> <p>111 = Internal counter ends sampling and starts conversion (auto-convert)</p> <p>110 = CTMU ends sampling and starts conversion</p> <p>101 = Reserved</p> <p>100 = Timer5 compare ends sampling and starts conversion</p> <p>011 = PWM primary Special Event Trigger ends sampling and starts conversion<sup>(2)</sup></p> <p>010 = Timer3 compare ends sampling and starts conversion</p> <p>001 = Active transition on the INT0 pin ends sampling and starts conversion</p> <p>000 = Clearing the Sample bit (SAMP) ends sampling and starts conversion (Manual mode)</p>
bit 4	<p><b>SSRCG:</b> Sample Trigger Source Group bit</p> <p>See SSRC&lt;2:0&gt; for details.</p>
bit 3	<p><b>SIMSAM:</b> Simultaneous Sample Select bit (only applicable when CHPS&lt;1:0&gt; = 01 or 1x)</p> <p><u>In 12-bit mode (AD21B = 1), SIMSAM is Unimplemented and is Read as '0':</u></p> <p>1 = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS&lt;1:0&gt; = 1x); or samples CH0 and CH1 simultaneously (when CHPS&lt;1:0&gt; = 01)</p> <p>0 = Samples multiple channels individually in sequence</p>
bit 2	<p><b>ASAM:</b> ADC1 Sample Auto-Start bit</p> <p>1 = Sampling begins immediately after the last conversion; SAMP bit is auto-set</p> <p>0 = Sampling begins when the SAMP bit is set</p>
bit 1	<p><b>SAMP:</b> ADC1 Sample Enable bit</p> <p>1 = ADC Sample-and-Hold amplifiers are sampling</p> <p>0 = ADC Sample-and-Hold amplifiers are holding</p> <p>If ASAM = 0, software can write '1' to begin sampling. Automatically set by hardware if ASAM = 1. If SSRC&lt;2:0&gt; = 000, software can write '0' to end sampling and start conversion. If SSRC&lt;2:0&gt; ≠ 000, automatically cleared by hardware to end sampling and start conversion.</p>
bit 0	<p><b>DONE:</b> ADC1 Conversion Status bit<sup>(3)</sup></p> <p>1 = ADC conversion cycle has completed</p> <p>0 = ADC conversion has not started or is in progress</p> <p>Automatically set by hardware when the ADC conversion is complete. Software can write '0' to clear the DONE status bit (software is not allowed to write '1'). Clearing this bit does NOT affect any operation in progress. Automatically cleared by hardware at the start of a new conversion.</p>

- Note 1:** See Section 24.0 “Peripheral Trigger Generator (PTG) Module” for information on this selection.
- 2:** This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- 3:** Do not clear the DONE bit in software if Auto-Sample is enabled (ASAM = 1).

**REGISTER 24-12: PTGQPTR: PTG STEP QUEUE POINTER REGISTER<sup>(1)</sup>**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	PTGQPTR<4:0>				
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'bit 4-0 **PTGQPTR<4:0>**: PTG Step Queue Pointer Register bits

This register points to the currently active Step command in the Step queue.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**REGISTER 24-13: PTGQUEX: PTG STEP QUEUE REGISTER x (x = 0-7)<sup>(1,3)</sup>**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP(2x + 1)<7:0> <sup>(2)</sup>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP(2x)<7:0> <sup>(2)</sup>							
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **STEP(2x + 1)<7:0>**: PTG Step Queue Pointer Register bits<sup>(2)</sup>

A queue location for storage of the STEP(2x + 1) command byte.

bit 7-0 **STEP(2x)<7:0>**: PTG Step Queue Pointer Register bits<sup>(2)</sup>

A queue location for storage of the STEP(2x) command byte.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**2:** Refer to Table 24-1 for the Step command encoding.

**3:** The Step registers maintain their values on any type of Reset.

**REGISTER 25-4: CMxMSKSRCA: COMPARATOR x MASK SOURCE SELECT  
CONTROL REGISTER (CONTINUED)**

bit 3-0      **SELSRCA<3:0>**: Mask A Input Select bits

1111 = FLT4  
1110 = FLT2  
1101 = PTGO19  
1100 = PTGO18  
1011 = Reserved  
1010 = Reserved  
1001 = Reserved  
1000 = Reserved  
0111 = Reserved  
0110 = Reserved  
0101 = PWM3H  
0100 = PWM3L  
0011 = PWM2H  
0010 = PWM2L  
0001 = PWM1H  
0000 = PWM1L

## 28.0 INSTRUCTION SET SUMMARY

**Note:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

The dsPIC33EP instruction set is almost identical to that of the dsPIC30F and dsPIC33F. The PIC24EP instruction set is almost identical to that of the PIC24F and PIC24H.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into five basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- DSP operations
- Control operations

Table 28-1 lists the general symbols used in describing the instructions.

The dsPIC33E instruction set summary in Table 28-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register ‘Wb’ without any address modifier
- The second source operand, which is typically a register ‘Ws’ with or without an address modifier
- The destination of the result, which is typically a register ‘Wd’ with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value ‘f’
- The destination, which could be either the file register ‘f’ or the W0 register, which is denoted as ‘WREG’

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of ‘Ws’ or ‘f’)
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register ‘Wb’)

The literal instructions that involve data movement can use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by ‘k’)
- The W register or file register where the literal value is to be loaded (specified by ‘Wb’ or ‘f’)

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register ‘Wb’ without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register ‘Wd’ with or without an address modifier

The MAC class of DSP instructions can use some of the following operands:

- The accumulator (A or B) to be used (required operand)
- The W registers to be used as the two operands
- The X and Y address space prefetch operations
- The X and Y address space prefetch destinations
- The accumulator write back destination

The other DSP instructions do not involve any multiplication and can include:

- The accumulator to be used (required)
- The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
- The amount of shift specified by a W register ‘Wn’ or a literal value

The control instructions can use some of the following operands:

- A program memory address
- The mode of the Table Read and Table Write instructions



FIGURE 30-2: EXTERNAL CLOCK TIMING

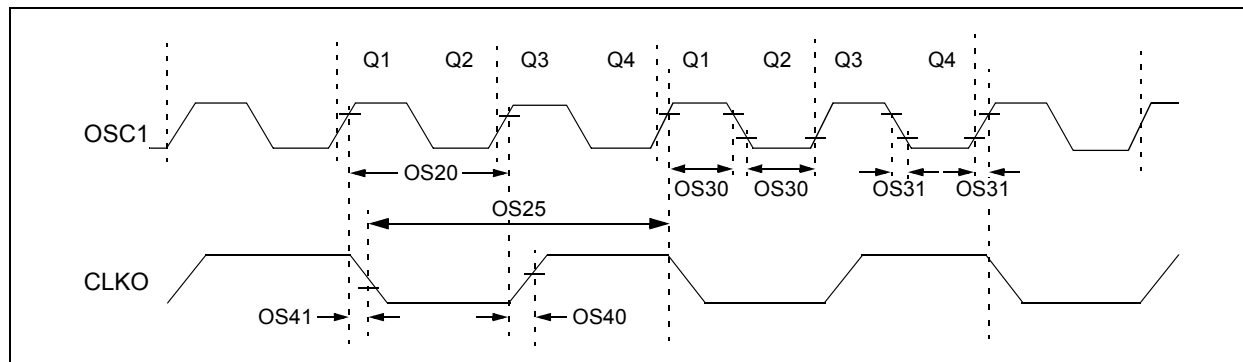


TABLE 30-17: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symb	Characteristic	Min.	Typ. <sup>(1)</sup>	Max.	Units	Conditions
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	60	MHz	EC
		Oscillator Crystal Frequency	3.5 10	— —	10 25	MHz MHz	XT HS
OS20	Tosc	Tosc = 1/Fosc	8.33	—	DC	ns	+125°C
		Tosc = 1/Fosc	7.14	—	DC	ns	+85°C
OS25	Tcy	Instruction Cycle Time <sup>(2)</sup>	16.67	—	DC	ns	+125°C
		Instruction Cycle Time <sup>(2)</sup>	14.28	—	DC	ns	+85°C
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.45 x Tosc	—	0.55 x Tosc	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time <sup>(3,4)</sup>	—	5.2	—	ns	
OS41	TckF	CLKO Fall Time <sup>(3,4)</sup>	—	5.2	—	ns	
OS42	GM	External Oscillator Transconductance <sup>(4)</sup>	—	12	—	mA/V	HS, VDD = 3.3V, TA = +25°C
			—	6	—	mA/V	XT, VDD = 3.3V, TA = +25°C

**Note 1:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

- 2:** Instruction cycle period (Tcy) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “Minimum” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “Maximum” cycle time limit is “DC” (no clock) for all devices.
- 3:** Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.
- 4:** This parameter is characterized, but not tested in manufacturing.

TABLE 30-24: TIMER2 AND TIMER4 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>		Min.	Typ.	Max.	Units	Conditions
TB10	TtxH	TxCK High Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	—	—	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB11	TtxL	TxCK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	—	—	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB15	TtxP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N	—	—	ns	N = prescale value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40	—	1.75 Tcy + 40	ns	

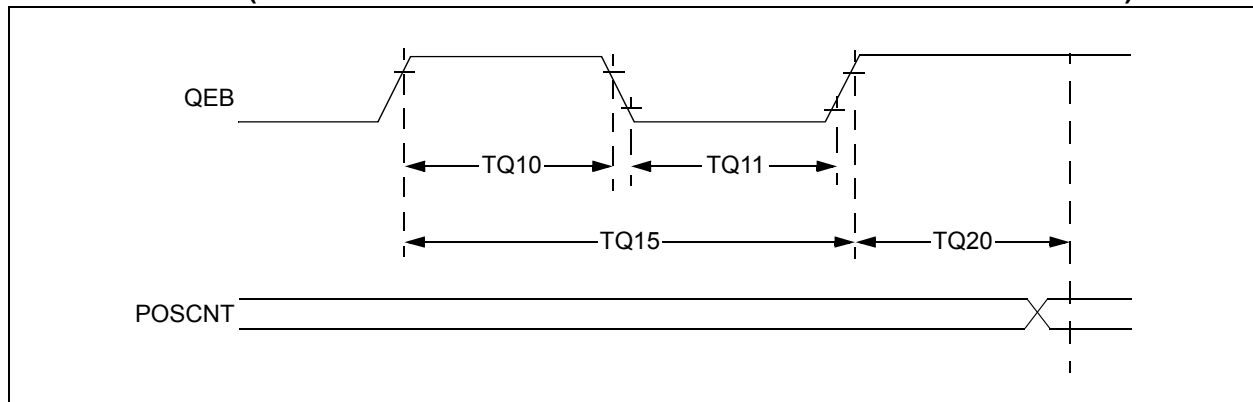
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

TABLE 30-25: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>		Min.	Typ.	Max.	Units	Conditions
TC10	TtxH	TxCK High Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC11	TtxL	TxCK Low Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC15	TtxP	TxCK Input Period	Synchronous, with prescaler	2 Tcy + 40	—	—	ns	N = prescale value (1, 8, 64, 256)
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40	—	1.75 Tcy + 40	ns	

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**FIGURE 30-11: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS  
(dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)**

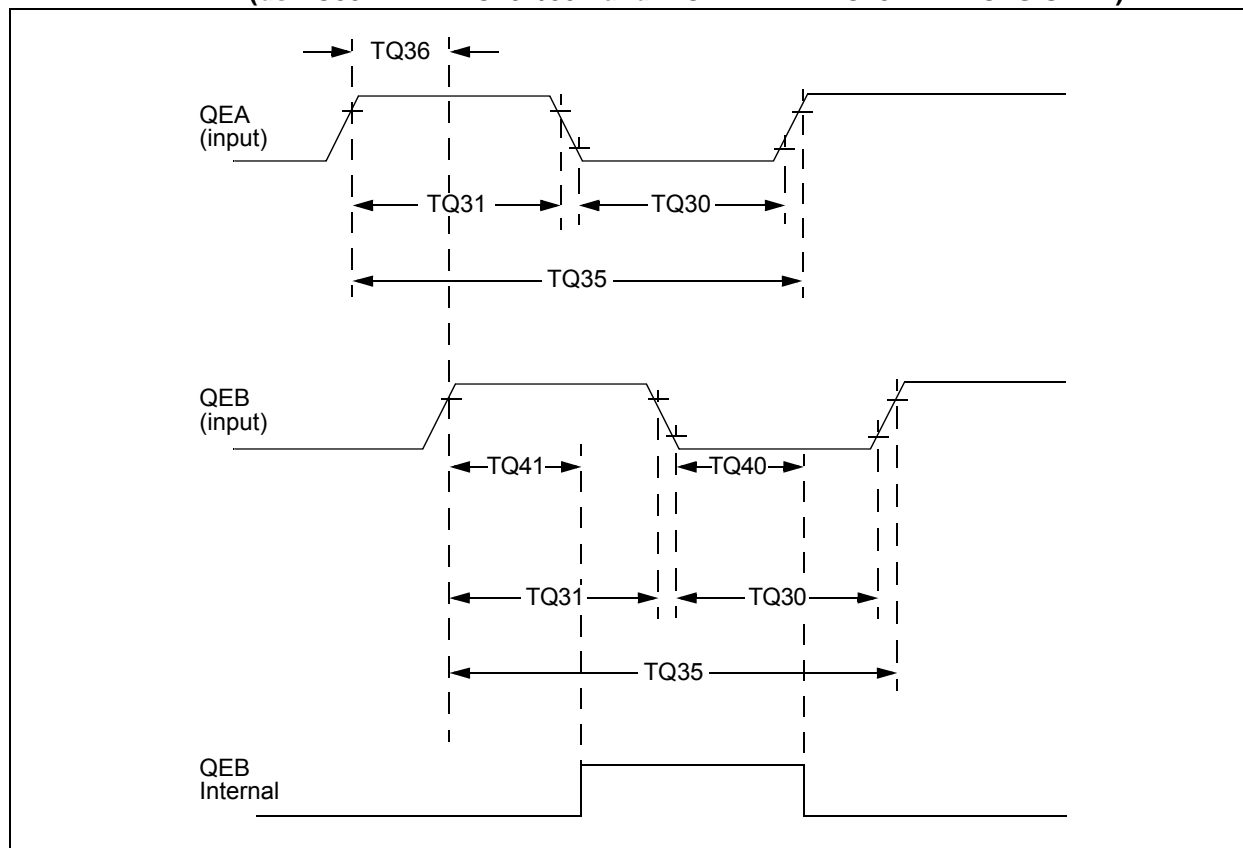


**TABLE 30-30: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS  
(dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)**

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic <sup>(1)</sup>		Min.	Typ.	Max.	Units	Conditions
TQ10	TtQH	TQCK High Time	Synchronous, with prescaler	Greater of $12.5 + 25$ or $(0.5 T_{CY}/N) + 25$	—	—	ns	Must also meet Parameter TQ15
TQ11	TtQL	TQCK Low Time	Synchronous, with prescaler	Greater of $12.5 + 25$ or $(0.5 T_{CY}/N) + 25$	—	—	ns	Must also meet Parameter TQ15
TQ15	TtQP	TQCP Input Period	Synchronous, with prescaler	Greater of $25 + 50$ or $(1 T_{CY}/N) + 50$	—	—	ns	
TQ20	TCKEXTMRL	Delay from External TQCK Clock Edge to Timer Increment		—	1	$T_{CY}$	—	

**Note 1:** These parameters are characterized but not tested in manufacturing.

**FIGURE 30-12: QEA/QEB INPUT CHARACTERISTICS**  
(dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)



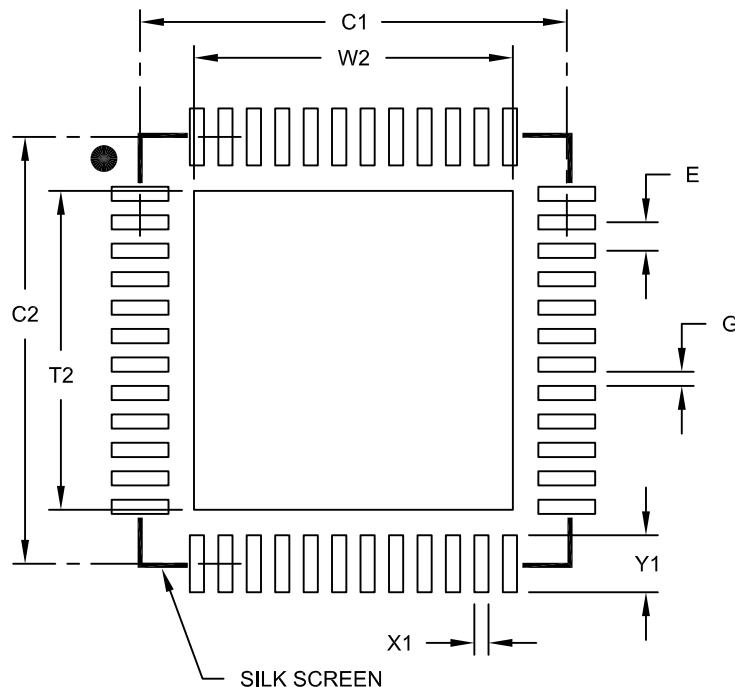
**TABLE 30-31: QUADRATURE DECODER TIMING REQUIREMENTS**  
(dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	Symbol	Characteristic <sup>(1)</sup>	Typ. <sup>(2)</sup>	Max.	Units	Conditions
TQ30	TQuL	Quadrature Input Low Time	6 TcY	—	ns	
TQ31	TQuH	Quadrature Input High Time	6 TcY	—	ns	
TQ35	TQuIN	Quadrature Input Period	12 TcY	—	ns	
TQ36	TQuP	Quadrature Phase Period	3 TcY	—	ns	
TQ40	TQuFL	Filter Time to Recognize Low, with Digital Filter	3 * N * TcY	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 ( <b>Note 3</b> )
TQ41	TQuFH	Filter Time to Recognize High, with Digital Filter	3 * N * TcY	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 ( <b>Note 3</b> )

- Note 1:** These parameters are characterized but not tested in manufacturing.
- Note 2:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- Note 3:** N = Index Channel Digital Filter Clock Divide Select bits. Refer to “**Quadrature Encoder Interface (QEI)**” (DS70601) in the “*dsPIC33/PIC24 Family Reference Manual*”. Please see the Microchip web site for the latest family reference manual sections.

48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN]  
With 0.40 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Optional Center Pad Width	W2			4.45
Optional Center Pad Length	T2			4.45
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A