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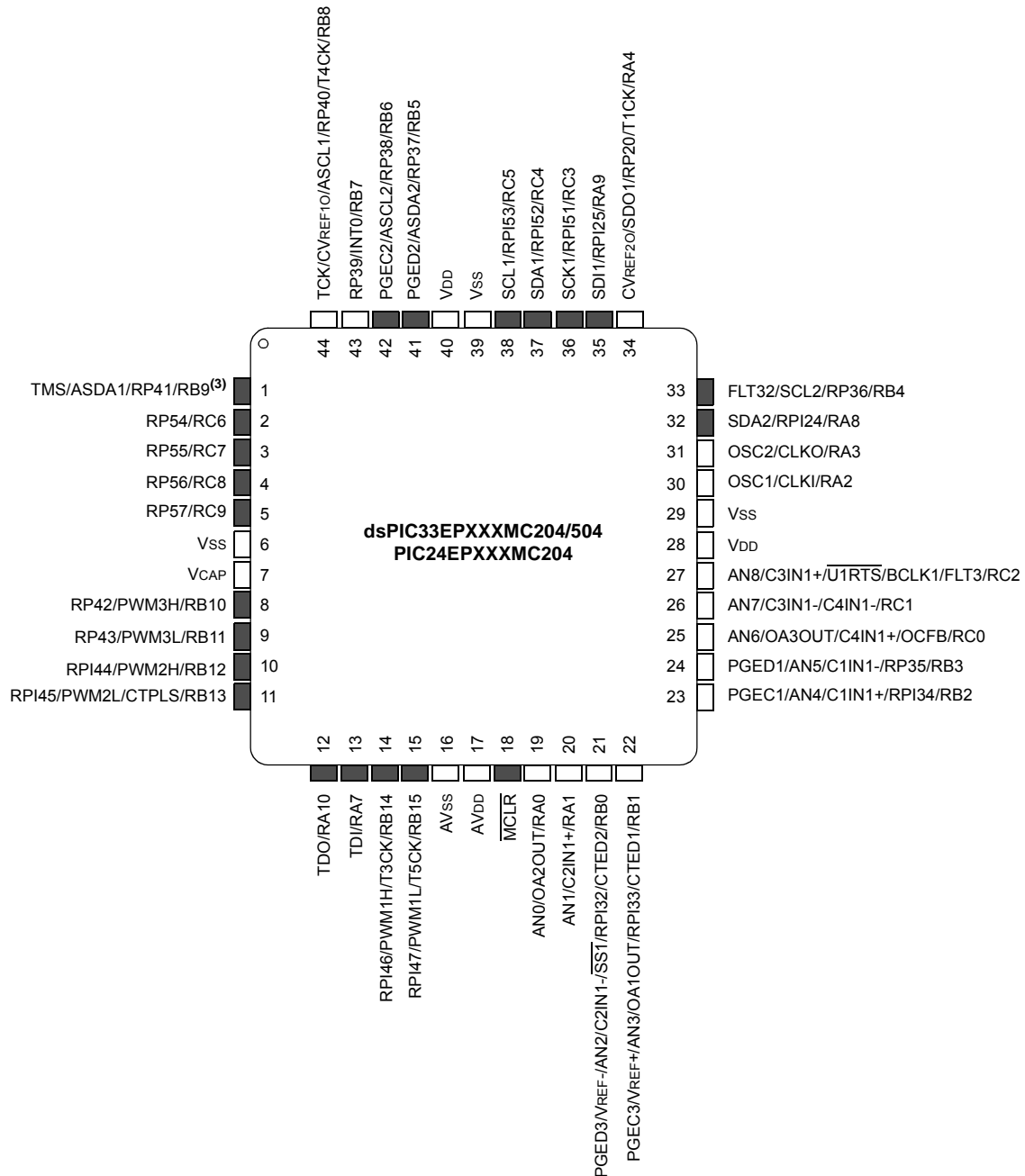
Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64mc504-e-mv

Pin Diagrams (Continued)

44-Pin TQFP[1,2]

■ = Pins are up to 5V tolerant

Top pins (left to right, 44–34):
- 44 TCK/CV$_{REF1O}$/ASCL1/RP40/T4CK/RB8
- 43 RP39/INT0/RB7
- 42 PGEC2/ASCL2/RP38/RB6
- 41 PGED2/ASDA2/RP37/RB5
- 40 VDD
- 39 VSS
- 38 SCL1/RPI53/RC5
- 37 SDA1/RPI52/RC4
- 36 SCK1/RPI51/RC3
- 35 SDI1/RPI25/RA9
- 34 CV$_{REF2O}$/SDO1/RP20/T1CK/RA4

Left pins (1–11):
- 1 TMS/ASDA1/RP41/RB9[3]
- 2 RP54/RC6
- 3 RP55/RC7
- 4 RP56/RC8
- 5 RP57/RC9
- 6 VSS
- 7 VCAP
- 8 RP42/PWM3H/RB10
- 9 RP43/PWM3L/RB11
- 10 RPI44/PWM2H/RB12
- 11 RPI45/PWM2L/CTPLS/RB13

Device label:
dsPIC33EPXXXMC204/504
PIC24EPXXXMC204

Right pins (33–23):
- 33 FLT32/SCL2/RP36/RB4
- 32 SDA2/RPI24/RA8
- 31 OSC2/CLKO/RA3
- 30 OSC1/CLKI/RA2
- 29 VSS
- 28 VDD
- 27 AN8/C3IN1+/$\overline{U1RTS}$/BCLK1/FLT3/RC2
- 26 AN7/C3IN1-/C4IN1-/RC1
- 25 AN6/OA3OUT/C4IN1+/OCFB/RC0
- 24 PGED1/AN5/C1IN1-/RP35/RB3
- 23 PGEC1/AN4/C1IN1+/RPI34/RB2

Bottom pins (left to right, 12–22):
- 12 TDO/RA10
- 13 TDI/RA7
- 14 RPI46/PWM1H/T3CK/RB14
- 15 RPI47/PWM1L/T5CK/RB15
- 16 AVSS
- 17 AVDD
- 18 $\overline{MCLR}$
- 19 AN0/OA2OUT/RA0
- 20 AN1/C2IN1+/RA1
- 21 PGED3/V$_{REF}$-/AN2/C2IN1-/$\overline{SS1}$/RPI32/CTED2/RB0
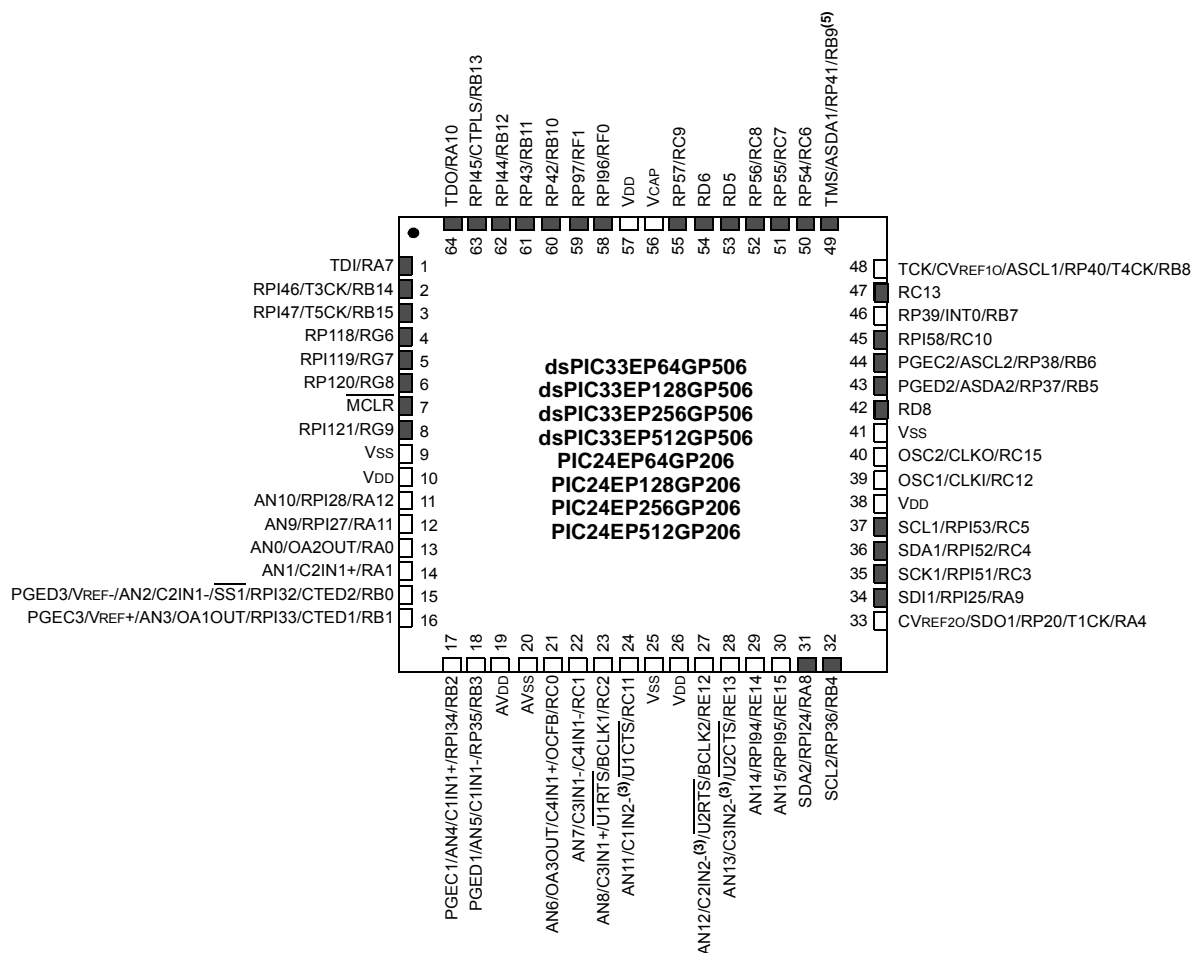- 22 PGEC3/V$_{REF}$+/AN3/OA1OUT/RPI33/CTED1/RB1

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

Pin Diagrams (Continued)

64-Pin QFN[1,2,3,4]

■ = Pins are up to 5V tolerant

Pins (top, left to right, 64–49):
- 64 TDO/RA10
- 63 RPI45/CTPLS/RB13
- 62 RP144/RB12
- 61 RP43/RB11
- 60 RP42/RB10
- 59 RP97/RF1
- 58 RPI96/RF0
- 57 VDD
- 56 VCAP
- 55 RP57/RC9
- 54 RD6
- 53 RD5
- 52 RP56/RC8
- 51 RP55/RC7
- 50 RP54/RC6
- 49 TMS/ASDA1/RP41/RB9[5]

Pins (left side, 1–16):
- 1 TDI/RA7
- 2 RPI46/T3CK/RB14
- 3 RPI47/T5CK/RB15
- 4 RP118/RG6
- 5 RPI119/RG7
- 6 RP120/RG8
- 7 MCLR
- 8 RPI121/RG9
- 9 VSS
- 10 VDD
- 11 AN10/RPI28/RA12
- 12 AN9/RPI27/RA11
- 13 AN0/OA2OUT/RA0
- 14 AN1/C2IN1+/RA1
- 15 PGED3/VREF-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0
- 16 PGEC3/VREF+/AN3/OA1OUT/RPI33/CTED1/RB1

Device label (center):
dsPIC33EP64GP506
dsPIC33EP128GP506
dsPIC33EP256GP506
dsPIC33EP512GP506
PIC24EP64GP206
PIC24EP128GP206
PIC24EP256GP206
PIC24EP512GP206

Pins (right side, 48–33):
- 48 TCK/CVREF1O/ASCL1/RP40/T4CK/RB8
- 47 RC13
- 46 RP39/INT0/RB7
- 45 RPI58/RC10
- 44 PGEC2/ASCL2/RP38/RB6
- 43 PGED2/ASDA2/RP37/RB5
- 42 RD8
- 41 VSS
- 40 OSC2/CLKO/RC15
- 39 OSC1/CLKI/RC12
- 38 VDD
- 37 SCL1/RPI53/RC5
- 36 SDA1/RPI52/RC4
- 35 SCK1/RPI51/RC3
- 34 SDI1/RPI25/RA9
- 33 CVREF2O/SDO1/RP20/T1CK/RA4

Pins (bottom, 17–32):
- 17 PGEC1/AN4/C1IN1+/RPI34/RB2
- 18 PGED1/AN5/C1IN1-/RP35/RB3
- 19 AVDD
- 20 AVSS
- 21 AN6/OA3OUT/C4IN1+/RC0
- 22 AN7/C3IN1-/C4IN1-/RC1
- 23 AN8/C3IN1+/U1RTS/BCLK1/RC2
- 24 AN11/C1IN2-/U1CTS/RC11
- 25 VSS
- 26 VDD
- 27 AN12/C2IN2-/U2RTS/BCLK2/RE12
- 28 AN13/C3IN2-/U2CTS/RE13
- 29 AN14/RPI94/RE14
- 30 AN15/RPI95/RE15
- 31 SDA2/RPI24/RA8
- 32 SCL2/RP36/RB4

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: This pin is not available as an input when OPMODE (CMxCON<10>) = `1`.

4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

5: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com)
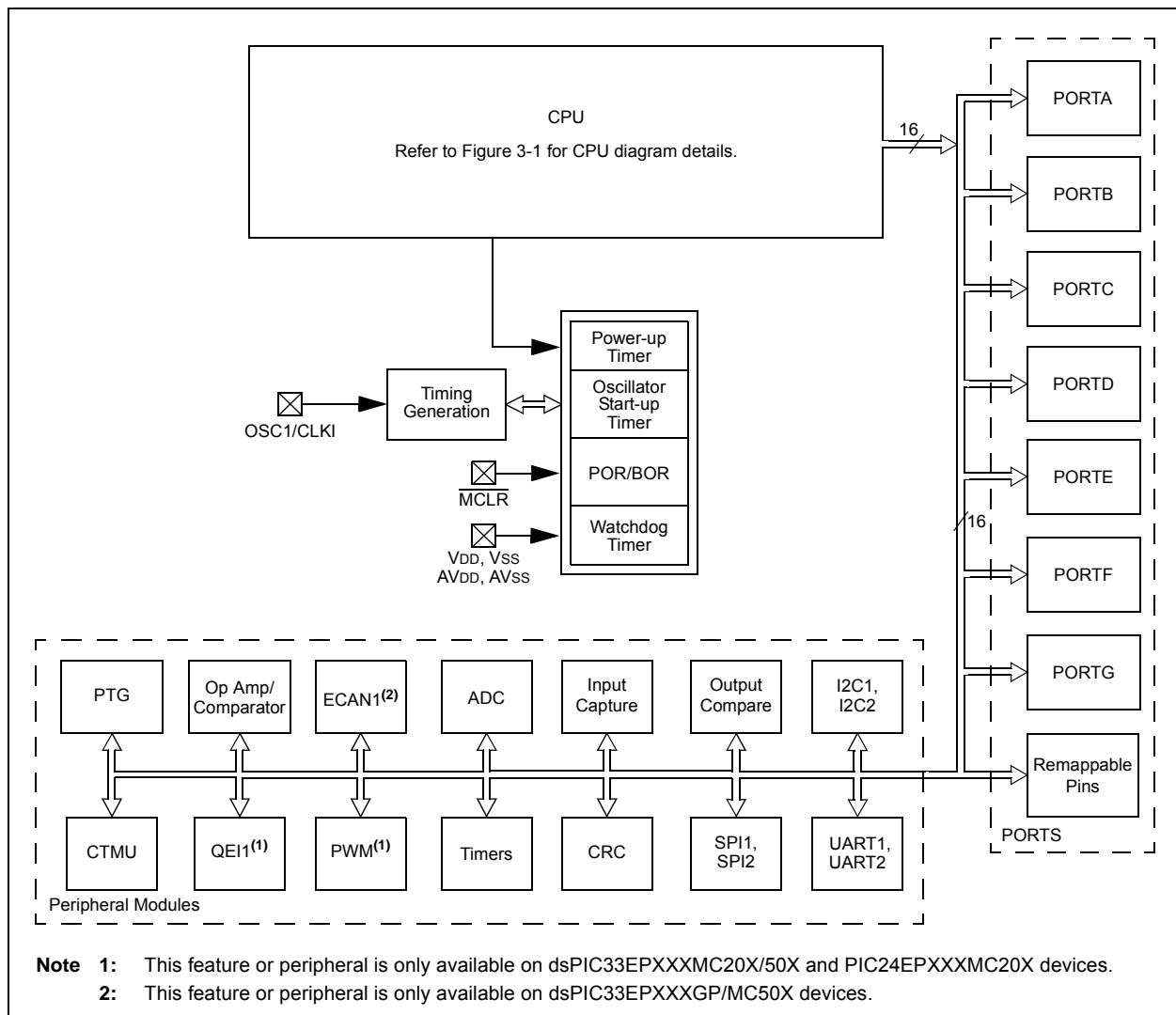
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X BLOCK DIAGRAM

Note 1: This feature or peripheral is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.
2: This feature or peripheral is only available on dsPIC33EPXXXGP/MC50X devices.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1[1]	US0[1]	EDT[1,2]	DL2[1]	DL1[1]	DL0[1]
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA[1]	SATB[1]	SATDW[1]	ACCSAT[1]	IPL3[3]	SFA	RND[1]	IF[1]
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit

    1 = Variable exception processing latency is enabled
    0 = Fixed exception processing latency is enabled

bit 14 **Unimplemented:** Read as '0'

bit 13-12 **US<1:0>:** DSP Multiply Unsigned/Signed Control bits[1]

    11 = Reserved
    10 = DSP engine multiplies are mixed-sign
    01 = DSP engine multiplies are unsigned
    00 = DSP engine multiplies are signed

bit 11 **EDT:** Early DO Loop Termination Control bit[1,2]

    1 = Terminates executing DO loop at end of current loop iteration
    0 = No effect

bit 10-8 **DL<2:0>:** DO Loop Nesting Level Status bits[1]

    111 = 7 DO loops are active
    •
    •
    •
    001 = 1 DO loop is active
    000 = 0 DO loops are active

bit 7 **SATA:** ACCA Saturation Enable bit[1]

    1 = Accumulator A saturation is enabled
    0 = Accumulator A saturation is disabled

bit 6 **SATB:** ACCB Saturation Enable bit[1]

    1 = Accumulator B saturation is enabled
    0 = Accumulator B saturation is disabled

bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit[1]

    1 = Data Space write saturation is enabled
    0 = Data Space write saturation is disabled

bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit[1]

    1 = 9.31 saturation (super saturation)
    0 = 1.31 saturation (normal saturation)

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3[3]

    1 = CPU Interrupt Priority Level is greater than 7
    0 = CPU Interrupt Priority Level is 7 or less

Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

    2: This bit is always read as '0'.

    3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

4.2.5 X AND Y DATA SPACES

The dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X core has two Data Spaces, X and Y. These Data Spaces can be considered either separate (for some DSP instructions) or as one unified linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X Data Space is used by all instructions and supports all addressing modes. X Data Space has separate read and write data buses. The X read data bus is the read data path for all instructions that view Data Space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y Data Space is used in concert with the X Data Space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY.N and MSC) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X Data Space. Modulo Addressing and Bit-Reversed Addressing are not present in PIC24EPXXXGP/MC20X devices.

All data memory writes, including in DSP instructions, view Data Space as combined X and Y address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

4.3 Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

> **Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

4.3.1 KEY RESOURCES

- **"Program Memory"** (DS70613) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

TABLE 4-5: **INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	—	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	ILR<3:0>				VECNUM<7:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

7.3 Interrupt Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

> **Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

7.3.1 KEY RESOURCES

- **"Interrupts"** (DS70600) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

7.4 Interrupt Control and Status Registers

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON3
- INTCON4
- INTTREG

7.4.1 INTCON1 THROUGH INTCON4

Global interrupt control functions are controlled from INTCON1, INTCON2, INTCON3 and INTCON4.

INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS), as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior and also contains the Global Interrupt Enable bit (GIE).

INTCON3 contains the status flags for the DMA and DO stack overflow status trap sources.

The INTCON4 register contains the software generated hard trap status bit (SGHT).

7.4.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

7.4.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

7.4.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

7.4.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number bits (VECNUM<7:0>) and Interrupt Priority Level bits (ILR<3:0>) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 7-1. For example, the INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0> and the INT0IP bits in the first position of IPC0 (IPC0<2:0>).

7.4.6 STATUS/CONTROL REGISTERS

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers refer to **"CPU"** (DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*.

- The CPU STATUS Register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.
- The CORCON register contains the IPL3 bit which, together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-3 through Register 7-7 in the following pages.

14.0 INPUT CAPTURE

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Input Capture"** (DS70352) in the "*dsPIC33/dsPIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).
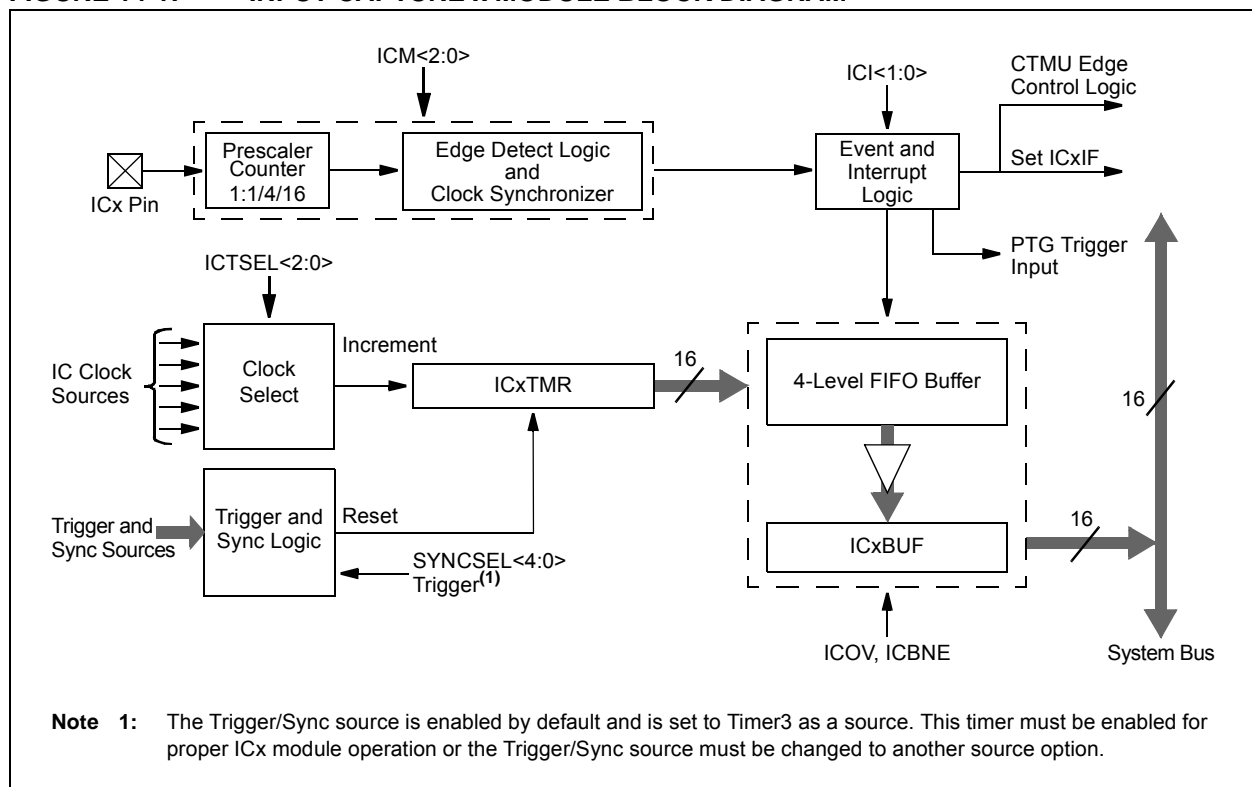>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support four input capture channels.

Key features of the input capture module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 19 user-selectable Trigger/Sync sources available
- A 4-level FIFO buffer for capturing and holding timer values for several events
- Configurable interrupt generation
- Up to six clock sources available for each module, driving a separate internal 16-bit counter

FIGURE 14-1: INPUT CAPTURE x MODULE BLOCK DIAGRAM

Note 1: The Trigger/Sync source is enabled by default and is set to Timer3 as a source. This timer must be enabled for proper ICx module operation or the Trigger/Sync source must be changed to another source option.

14.2   Input Capture Registers

REGISTER 14-1:   ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend:		HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-14   **Unimplemented:** Read as '0'

bit 13   **ICSIDL:** Input Capture Stop in Idle Control bit

    1 = Input capture will Halt in CPU Idle mode
    0 = Input capture will continue to operate in CPU Idle mode

bit 12-10   **ICTSEL<2:0>:** Input Capture Timer Select bits

    111 = Peripheral clock (FP) is the clock source of the ICx
    110 = Reserved
    101 = Reserved
    100 = T1CLK is the clock source of the ICx (only the synchronous clock is supported)
    011 = T5CLK is the clock source of the ICx
    010 = T4CLK is the clock source of the ICx
    001 = T2CLK is the clock source of the ICx
    000 = T3CLK is the clock source of the ICx

bit 9-7   **Unimplemented:** Read as '0'

bit 6-5   **ICI<1:0>:** Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)

    11 = Interrupt on every fourth capture event
    10 = Interrupt on every third capture event
    01 = Interrupt on every second capture event
    00 = Interrupt on every capture event

bit 4   **ICOV:** Input Capture Overflow Status Flag bit (read-only)

    1 = Input capture buffer overflow occurred
    0 = No input capture buffer overflow occurred

bit 3   **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)

    1 = Input capture buffer is not empty, at least one more capture value can be read
    0 = Input capture buffer is empty

bit 2-0   **ICM<2:0>:** Input Capture Mode Select bits

    111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
    110 = Unused (module is disabled)
    101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
    100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
    011 = Capture mode, every rising edge (Simple Capture mode)
    010 = Capture mode, every falling edge (Simple Capture mode)
    001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
    000 = Input capture module is turned off

17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Quadrature Encoder Interface (QEI)"** (DS70601) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI module include:

- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 16-Bit Velocity Counter
- 32-Bit Position Initialization/Capture/Compare High register
- 32-Bit Position Compare Low register
- x4 Quadrature Count mode
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Internal Timer mode

Figure 17-1 illustrates the QEI block diagram.

REGISTER 21-3:   CxVEC: ECANx INTERRUPT CODE REGISTER

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0
bit 15							bit 8

U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
—	ICODE6	ICODE5	ICODE4	ICODE3	ICODE2	ICODE1	ICODE0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-13   **Unimplemented:** Read as '0'

bit 12-8   **FILHIT<4:0>:** Filter Hit Number bits
               10000-11111 = Reserved
               01111 = Filter 15
               •
               •
               •
               00001 = Filter 1
               00000 = Filter 0

bit 7   **Unimplemented:** Read as '0'

bit 6-0   **ICODE<6:0>:** Interrupt Flag Code bits
               1000101-1111111 = Reserved
               1000100 = FIFO almost full interrupt
               1000011 = Receiver overflow interrupt
               1000010 = Wake-up interrupt
               1000001 = Error interrupt
               1000000 = No interrupt
               •
               •
               •
               0010000-0111111 = Reserved
               0001111 = RB15 buffer interrupt
               •
               •
               •
               0001001 = RB9 buffer interrupt
               0001000 = RB8 buffer interrupt
               0000111 = TRB7 buffer interrupt
               0000110 = TRB6 buffer interrupt
               0000101 = TRB5 buffer interrupt
               0000100 = TRB4 buffer interrupt
               0000011 = TRB3 buffer interrupt
               0000010 = TRB2 buffer interrupt
               0000001 = TRB1 buffer interrupt
               0000000 = TRB0 buffer interrupt

22.2 CTMU Control Registers

REGISTER 22-1: CTMUCON1: CTMU CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN[1]	CTTRIG
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **CTMUEN:** CTMU Enable bit

1 = Module is enabled
0 = Module is disabled

bit 14   **Unimplemented:** Read as '0'

bit 13   **CTMUSIDL:** CTMU Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12   **TGEN:** Time Generation Enable bit

1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11   **EDGEN:** Edge Enable bit

1 = Hardware modules are used to trigger edges (TMRx, CTEDx, etc.)
0 = Software is used to trigger edges (manual set of EDGxSTAT)

bit 10   **EDGSEQEN:** Edge Sequence Enable bit

1 = Edge 1 event must occur before Edge 2 event can occur
0 = No edge sequence is needed

bit 9   **IDISSEN:** Analog Current Source Control bit[1]

1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8   **CTTRIG:** ADC Trigger Control bit

1 = CTMU triggers ADC start of conversion
0 = CTMU does not trigger ADC start of conversion

bit 7-0   **Unimplemented:** Read as '0'

Note 1: The ADC module Sample-and-Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitance measurement must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

REGISTER 23-2:   AD1CON2: ADC1 CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
VCFG2	VCFG1	VCFG0	—	—	CSCNA	CHPS1	CHPS0
bit 15							bit 8

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13   **VCFG<2:0>:** Converter Voltage Reference Configuration bits

Value	V_{REFH}	V_{REFL}
000	A_{VDD}	A_{VSS}
001	External V_{REF}+	A_{VSS}
010	A_{VDD}	External V_{REF}-
011	External V_{REF}+	External V_{REF}-
1xx	A_{VDD}	A_{VSS}

bit 12-11   **Unimplemented:** Read as '0'

bit 10   **CSCNA:** Input Scan Select bit

1 = Scans inputs for CH0+ during Sample MUXA
0 = Does not scan inputs

bit 9-8   **CHPS<1:0>:** Channel Select bits

In 12-bit mode (AD21B = 1), the CHPS<1:0> bits are Unimplemented and are Read as '0':
1x = Converts CH0, CH1, CH2 and CH3
01 = Converts CH0 and CH1
00 = Converts CH0

bit 7   **BUFS:** Buffer Fill Status bit (only valid when BUFM = 1)

1 = ADC is currently filling the second half of the buffer; the user application should access data in the first half of the buffer
0 = ADC is currently filling the first half of the buffer; the user application should access data in the second half of the buffer

bit 6-2   **SMPI<4:0>:** Increment Rate bits

When ADDMAEN = 0:
x1111 = Generates interrupt after completion of every 16th sample/conversion operation
x1110 = Generates interrupt after completion of every 15th sample/conversion operation
•
•
•
x0001 = Generates interrupt after completion of every 2nd sample/conversion operation
x0000 = Generates interrupt after completion of every sample/conversion operation
When ADDMAEN = 1:
11111 = Increments the DMA address after completion of every 32nd sample/conversion operation
11110 = Increments the DMA address after completion of every 31st sample/conversion operation
•
•
•
00001 = Increments the DMA address after completion of every 2nd sample/conversion operation
00000 = Increments the DMA address after completion of every sample/conversion operation

REGISTER 23-8: **AD1CSSL: ADC1 INPUT SCAN SELECT REGISTER LOW**[1,2]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **CSS<15:0>:** ADC1 Input Scan Selection bits
           1 = Selects ANx for input scan
           0 = Skips ANx for input scan

Note 1: On devices with less than 16 analog inputs, all AD1CSSL bits can be selected by the user. However, inputs selected for scan, without a corresponding input on the device, convert V_{REFL}.

    2: CSSx = ANx, where x = 0-15.

TABLE 30-9: **DC CHARACTERISTICS: WATCHDOG TIMER DELTA CURRENT (ΔIWDT)[1]**

DC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40°C \leq TA \leq +85°C$ for Industrial $-40°C \leq TA \leq +125°C$ for Extended	
Parameter No.	Typ.	Max.	Units	Conditions	
DC61d	8	—	μA	-40°C	
DC61a	10	—	μA	+25°C	3.3V
DC61b	12	—	μA	+85°C	
DC61c	13	—	μA	+125°C	

Note 1: The ΔIWDT current is the additional current consumed when the module is enabled. This current should be added to the base IPD current. All parameters are characterized but not tested during manufacturing.

TABLE 30-10: **DC CHARACTERISTICS: DOZE CURRENT (IDOZE)**

DC CHARACTERISTICS					Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40°C \leq TA \leq +85°C$ for Industrial $-40°C \leq TA \leq +125°C$ for Extended		
Parameter No.	Typ.	Max.	Doze Ratio	Units	Conditions		
Doze Current (IDOZE)[1]							
DC73a[2]	35	—	1:2	mA	-40°C	3.3V	FOSC = 140 MHz
DC73g	20	30	1:128	mA			
DC70a[2]	35	—	1:2	mA	+25°C	3.3V	FOSC = 140 MHz
DC70g	20	30	1:128	mA			
DC71a[2]	35	—	1:2	mA	+85°C	3.3V	FOSC = 140 MHz
DC71g	20	30	1:128	mA			
DC72a[2]	28	—	1:2	mA	+125°C	3.3V	FOSC = 120 MHz
DC72g	15	30	1:128	mA			

Note 1: IDOZE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDOZE measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- CPU is executing `while(1)` statement
- JTAG is disabled

2: Parameter is characterized but not tested in manufacturing.

30.2 AC Characteristics and Timing Parameters

This section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X AC characteristics and timing parameters.

TABLE 30-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C $\leq$ TA $\leq$ +85°C for Industrial -40°C $\leq$ TA $\leq$ +125°C for Extended Operating voltage VDD range as described in **Section 30.1 "DC Characteristics"**.

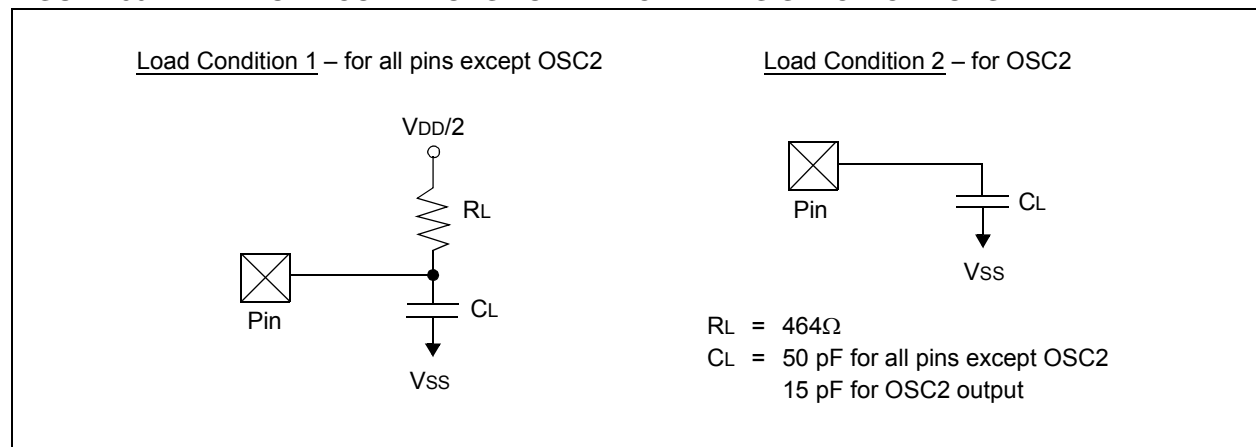**FIGURE 30-1:   LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**

Load Condition 1 – for all pins except OSC2

Load Condition 2 – for OSC2

VDD/2

RL

Pin

CL

Vss

Pin

CL

Vss

RL = 464Ω
CL = 50 pF for all pins except OSC2
         15 pF for OSC2 output

TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO50	C_{OSCO}	OSC2 Pin	—	—	15	pF	In XT and HS modes, when external clock is used to drive OSC1
DO56	C_{IO}	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	C_B	SCLx, SDAx	—	—	400	pF	In I²C™ mode

TABLE 30-24: TIMER2 AND TIMER4 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic[1]		Min.	Typ.	Max.	Units	Conditions
TB10	TtxH	TxCK High Time	Synchronous mode	Greater of: 20 or (TCY + 20)/N	—	—	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB11	TtxL	TxCK Low Time	Synchronous mode	Greater of: 20 or (TCY + 20)/N	—	—	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB15	TtxP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 TCY + 40)/N	—	—	ns	N = prescale value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 TCY + 40	—	1.75 TCY + 40	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

TABLE 30-25: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic[1]		Min.	Typ.	Max.	Units	Conditions
TC10	TtxH	TxCK High Time	Synchronous	TCY + 20	—	—	ns	Must also meet Parameter TC15
TC11	TtxL	TxCK Low Time	Synchronous	TCY + 20	—	—	ns	Must also meet Parameter TC15
TC15	TtxP	TxCK Input Period	Synchronous, with prescaler	2 TCY + 40	—	—	ns	N = prescale value (1, 8, 64, 256)
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 TCY + 40	—	1.75 TCY + 40	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

TABLE 30-49: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	Symbol	Characteristic[4]		Min.[1]	Max.	Units	Conditions
IM10	$T_{LO:SCL}$	Clock Low Time	100 kHz mode	TCY/2 (BRG + 2)	—	μs	
			400 kHz mode	TCY/2 (BRG + 2)	—	μs	
			1 MHz mode[2]	TCY/2 (BRG + 2)	—	μs	
IM11	$T_{HI:SCL}$	Clock High Time	100 kHz mode	TCY/2 (BRG + 2)	—	μs	
			400 kHz mode	TCY/2 (BRG + 2)	—	μs	
			1 MHz mode[2]	TCY/2 (BRG + 2)	—	μs	
IM20	$T_{F:SCL}$	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode[2]	—	100	ns	
IM21	$T_{R:SCL}$	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode[2]	—	300	ns	
IM25	$T_{SU:DAT}$	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode[2]	40	—	ns	
IM26	$T_{HD:DAT}$	Data Input Hold Time	100 kHz mode	0	—	μs	
			400 kHz mode	0	0.9	μs	
			1 MHz mode[2]	0.2	—	μs	
IM30	$T_{SU:STA}$	Start Condition Setup Time	100 kHz mode	TCY/2 (BRG + 2)	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	TCY/2 (BRG + 2)	—	μs	
			1 MHz mode[2]	TCY/2 (BRG + 2)	—	μs	
IM31	$T_{HD:STA}$	Start Condition Hold Time	100 kHz mode	TCY/2 (BRG + 2)	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	TCY/2 (BRG +2)	—	μs	
			1 MHz mode[2]	TCY/2 (BRG + 2)	—	μs	
IM33	$T_{SU:STO}$	Stop Condition Setup Time	100 kHz mode	TCY/2 (BRG + 2)	—	μs	
			400 kHz mode	TCY/2 (BRG + 2)	—	μs	
			1 MHz mode[2]	TCY/2 (BRG + 2)	—	μs	
IM34	$T_{HD:STO}$	Stop Condition Hold Time	100 kHz mode	TCY/2 (BRG + 2)	—	μs	
			400 kHz mode	TCY/2 (BRG + 2)	—	μs	
			1 MHz mode[2]	TCY/2 (BRG + 2)	—	μs	
IM40	$T_{AA:SCL}$	Output Valid From Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode[2]	—	400	ns	
IM45	$T_{BF:SDA}$	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode[2]	0.5	—	μs	
IM50	CB	Bus Capacitive Loading		—	400	pF	
IM51	T_{PGD}	Pulse Gobbler Delay		65	390	ns	**(Note 3)**

Note 1: BRG is the value of the I2C™ Baud Rate Generator. Refer to **"Inter-Integrated Circuit (I2C™)"** (DS70330) in the "*dsPIC33/PIC24 Family Reference Manual".* Please see the Microchip web site for the latest family reference manual sections.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: Typical value for this parameter is 130 ns.

4: These parameters are characterized, but not tested in manufacturing.

**64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body
with 5.40 x 5.40 Exposed Pad [QFN]**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at
http://www.microchip.com/packaging
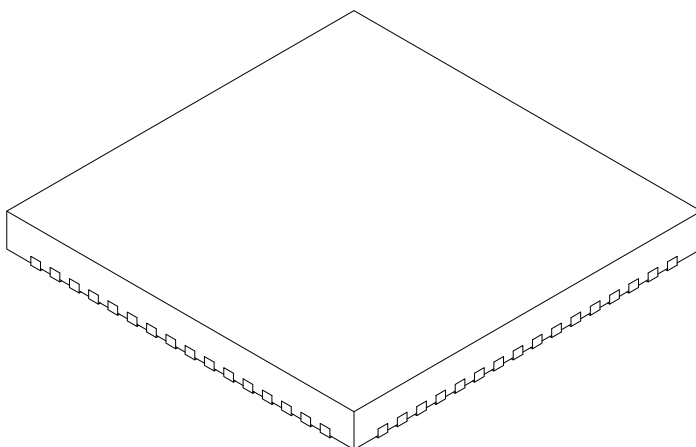
	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	64		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	9.00 BSC		
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D	9.00 BSC		
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
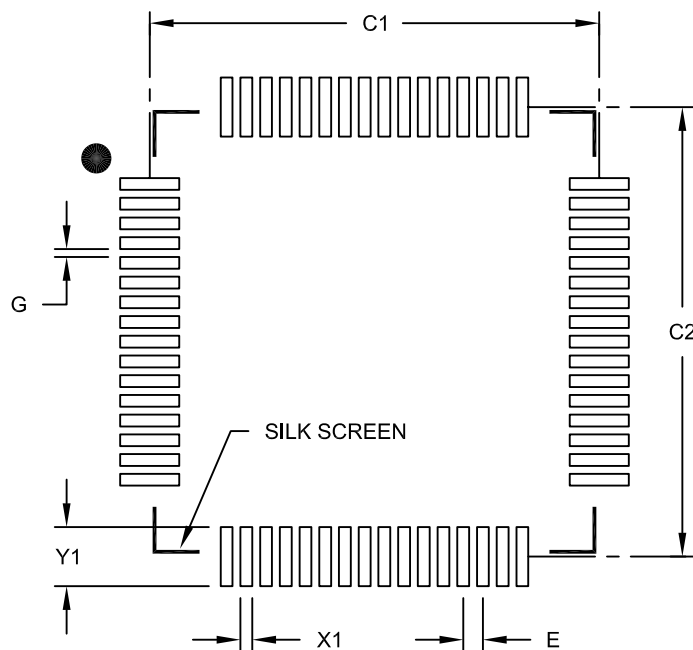
RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B