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Details

E·XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64mc504-e-pt

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3.8 Arithmetic Logic Unit (ALU)

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X ALU is 16 bits wide, and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the <u>SR register. The C and DC</u> Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157) for information on the SR bits affected by each instruction.

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.8.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier, the ALU supports unsigned, signed, or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.8.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.9 DSP Engine (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulatorto-accumulator operations that require no additional data. These instructions are ADD, SUB and NEG.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or integer DSP multiply (IF)
- · Signed, unsigned or mixed-sign DSP multiply (US)
- · Conventional or convergent rounding (RND)
- · Automatic saturation on/off for ACCA (SATA)
- Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACCSAT)

	OOMMAN									
Instruction	Algebraic Operation	ACC Write Back								
CLR	A = 0	Yes								
ED	$A = (x - y)^2$	No								
EDAC	$A = A + (x - y)^2$	No								
MAC	$A = A + (x \bullet y)$	Yes								
MAC	$A = A + x^2$	No								
MOVSAC	No change in A	Yes								
MPY	$A = x \bullet y$	No								
MPY	$A = x^2$	No								
MPY.N	$A = -x \bullet y$	No								
MSC	$A = A - x \bullet y$	Yes								

TABLE 3-2: DSP INSTRUCTIONS SUMMARY

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP64GP50X, dsPIC33EP64MC20X/50X AND PIC24EP64GP/MC20X DEVICES



Note: Memory areas are not shown to scale.

4.4.3 DATA MEMORY ARBITRATION AND BUS MASTER PRIORITY

EDS accesses from bus masters in the system are arbitrated.

The arbiter for data memory (including EDS) arbitrates between the CPU, the DMA and the ICD module. In the event of coincidental access to a bus by the bus masters, the arbiter determines which bus master access has the highest priority. The other bus masters are suspended and processed after the access of the bus by the bus master with the highest priority.

By default, the CPU is Bus Master 0 (M0) with the highest priority and the ICD is Bus Master 4 (M4) with the lowest priority. The remaining bus master (DMA Controller) is allocated to M3 (M1 and M2 are reserved and cannot be used). The user application may raise or lower the priority of the DMA Controller to be above that of the CPU by setting the appropriate bits in the EDS Bus Master Priority Control (MSTRPR) register. All bus masters with raised priorities will maintain the same priority relationship relative to each other (i.e., M1 being highest and M3 being lowest, with M2 in between). Also, all the bus masters with priorities below

FIGURE 4-18: ARBITER ARCHITECTURE

that of the CPU maintain the same priority relationship relative to each other. The priority schemes for bus masters with different MSTRPR values are tabulated in Table 4-62.

This bus master priority control allows the user application to manipulate the real-time response of the system, either statically during initialization or dynamically in response to real-time events.

TABLE 4-62:	DATA MEMORY BUS
	ARBITER PRIORITY

Briority	MSTRPR<15:0> Bit Setting ⁽¹⁾				
Phoney	0x0000	0x0020			
M0 (highest)	CPU	DMA			
M1	Reserved	CPU			
M2	Reserved	Reserved			
M3	DMA	Reserved			
M4 (lowest)	ICD	ICD			

Note 1: All other values of MSTRPR<15:0> are reserved.



REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)

- bit 3 SPI1MD: SPI1 Module Disable bit 1 = SPI1 module is disabled
 - 0 = SPI1 module is enabled
- bit 2 Unimplemented: Read as '0'
- bit 1 C1MD: ECAN1 Module Disable bit⁽²⁾ 1 = ECAN1 module is disabled 0 = ECAN1 module is enabled
- bit 0 AD1MD: ADC1 Module Disable bit 1 = ADC1 module is disabled 0 = ADC1 module is enabled
- Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
 - 2: This bit is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	—	—	—	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				U1RXR<6:0	>		
bit 7							bit 0

REGISTER 11-10: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 Unimplemented: Read as '0' bit 6-0 U1RXR<6:0>: Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121

REGISTER 11-11: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_		_	—	_	—	_
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				U2RXR<6:0>	>		
bit 7							bit 0
Legend:							

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 Unimplemented: Read as '0'

^{0000000 =} Input tied to Vss

REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)

bit 6-4	SYNCSRC<2:0>: Synchronous Source Selection bits ⁽¹⁾ 111 = Reserved
	•
	• 100 = Reserved 011 = PTGO17 ⁽²⁾ 010 = PTGO16 ⁽²⁾ 001 = Reserved 000 = SYNCI1 input from PPS
bit 3-0	<pre>SEVTPS<3:0>: PWMx Special Event Trigger Output Postscaler Select bits⁽¹⁾ 1111 = 1:16 Postscaler generates Special Event Trigger on every sixteenth compare match event</pre>
	0001 = 1:2 Postscaler generates Special Event Trigger on every second compare match event 0000 = 1:1 Postscaler generates Special Event Trigger on every compare match event

- **Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.
 - 2: See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
			PTPE	R<15:8>			
bit 15							bit 8
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
			PTPE	:R<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable bi	t	U = Unimpler	mented bit, read	d as '0'	

'0' = Bit is cleared

x = Bit is unknown

REGISTER 16-3: PTPER: PWMx PRIMARY MASTER TIME BASE PERIOD REGISTER

bit 15-0 **PTPER<15:0>:** Primary Master Time Base (PMTMR) Period Value bits

'1' = Bit is set

REGISTER 16-4: SEVTCMP: PWMx PRIMARY SPECIAL EVENT COMPARE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SEVTO	CMP<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SEVT	CMP<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	it	U = Unimplemented bit, read as '0'			
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is			x = Bit is unkı	nown			

bit 15-0 SEVTCMP<15:0>: Special Event Compare Count Value bits

-n = Value at POR

REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER (CONTINUED)

- bit 2 INDEX: Status of INDXx Input Pin After Polarity Control
 - 1 = Pin is at logic '1'
 - 0 = Pin is at logic '0'
- bit 1 QEB: Status of QEBx Input Pin After Polarity Control And SWPAB Pin Swapping 1 = Pin is at logic '1' 0 = Pin is at logic '0'
- bit 0 **QEA:** Status of QEAx Input Pin After Polarity Control And SWPAB Pin Swapping 1 = Pin is at logic '1'
 - 0 = Pin is at logic '0'

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	_	—	—	BCL	GCSTAT	ADD10
bit 15					•		bit 8
R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF
bit 7							bit 0
Legend:		C = Clearab	le bit	HS = Hardwa	re Settable bit	HSC = Hardware S	ettable/Clearable bit
R = Readabl	e bit	W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at	-n = Value at POR '1' = Bit is set		0' = Bit is cleared x = Bit is unknown				

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

bit 15	ACKSTAT: Acknowledge Status bit (when operating as I^2C^{TM} master, applicable to master transmit operation)
	1 = NACK received from slave 0 = ACK received from slave
	Hardware is set or clear at the end of slave Acknowledge.
bit 14	TRSTAT: Transmit Status bit (when operating as I^2C master, applicable to master transmit operation) 1 = Master transmit is in progress (8 bits + ACK)
	0 = Master transmit is not in progress Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
bit 13-11	Unimplemented: Read as '0'
bit 10	BCL: Master Bus Collision Detect bit
	1 = A bus collision has been detected during a master operation0 = No bus collision detected
	Hardware is set at detection of a bus collision.
bit 9	GCSTAT: General Call Status bit
	1 = General call address was received
	0 = General call address was not received
1.1.0	Hardware is set when address matches general call address. Hardware is clear at Stop detection.
DIT 8	ADD10: 10-Bit Address Status bit
	I = 10-bit address was matched 0 = 10-bit address was not matched
	Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
bit 7	IWCOL: I2Cx Write Collision Detect bit
~	1 = An attempt to write to the I2CxTRN register failed because the I^2 C module is busy 0 = No collision
	Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
bit 6	I2COV: I2Cx Receive Overflow Flag bit
	 1 = A byte was received while the I2CxRCV register was still holding the previous byte 0 = No overflow
	Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
bit 5	D_A: Data/Address bit (when operating as I ² C slave)
	1 = Indicates that the last byte received was data
	 Indicates that the last byte received was a device address Hardware is clear at a device address match. Hardware is set by reception of a slave byte.
bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware is set or clear when a Start, Repeated Start or Stop is detected.

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles ⁽²⁾	Status Flags Affected
72	SL	SL f		f = Left Shift f	1	1	C,N,OV,Z
		SL	f,WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL	Ws,Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL	Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL	Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z
73	SUB	SUB	_{Acc} (1)	Subtract Accumulators	1	1	OA,OB,OAB, SA,SB,SAB
		SUB	f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB	f,WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB	#lit10,Wn	Wn = Wn - lit10	1	1	C,DC,N,OV,Z
		SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		SUB	Wb,#lit5,Wd	Wd = Wb – lit5	1	1	C,DC,N,OV,Z
74	SUBB	SUBB	f	$f = f - WREG - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	f,WREG	WREG = $f - WREG - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	#lit10,Wn	$Wn = Wn - lit10 - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	Wb,Ws,Wd	$Wd = Wb - Ws - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	Wb,#lit5,Wd	$Wd = Wb - lit5 - (\overline{C})$	1	1	C,DC,N,OV,Z
75	SUBR	SUBR	f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	f,WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	Wb,Ws,Wd	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
76	SUBBR	SUBBR	f	$f = WREG - f - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBBR	f,WREG	WREG = WREG – f – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR	Wb,Ws,Wd	$Wd = Ws - Wb - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBBR	Wb,#lit5,Wd	$Wd = lit5 - Wb - (\overline{C})$	1	1	C,DC,N,OV,Z
77	SWAP	SWAP.b	Wn	Wn = nibble swap Wn	1	1	None
		SWAP	Wn	Wn = byte swap Wn	1	1	None
78	TBLRDH	TBLRDH	Ws,Wd	Read Prog<23:16> to Wd<7:0>	1	5	None
79	TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	5	None
80	TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
81	TBLWTL	TBLWTL Ws,Wd		Write Ws to Prog<15:0>	1	2	None
82	ULNK	ULNK		Unlink Frame Pointer	1	1	SFA
83	XOR	XOR	f	f = f .XOR. WREG	1	1	N,Z
		XOR	f,WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N,Z
84	ZE	ZE	Ws,Wnd	Wnd = Zero-extend Ws	1	1	C,Z,N

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias	40°C to +125°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to Vss ⁽³⁾	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when $VDD \ge 3.0V^{(3)}$	0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when $VDD < 3.0V^{(3)}$	-0.3V to +3.6V
Maximum current out of Vss pin	
Maximum current into VDD pin ⁽²⁾	
Maximum current sunk/sourced by any 4x I/O pin	
Maximum current sunk/sourced by any 8x I/O pin	25 mA
Maximum current sunk by all ports ^(2,4)	200 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
 - 2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).
 - 3: See the "Pin Diagrams" section for the 5V tolerant pins.
 - 4: Exceptions are: dsPIC33EPXXXGP502, dsPIC33EPXXXMC202/502 and PIC24EPXXXGP/MC202 devices, which have a maximum sink/source capability of 130 mA.

FIGURE 30-7: OUTPUT COMPARE x MODULE (OCx) TIMING CHARACTERISTICS



TABLE 30-27: OUTPUT COMPARE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS				$\begin{array}{llllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions	
OC10	TccF	OCx Output Fall Time	—			ns	See Parameter DO32	
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter DO31	

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-8: OCx/PWMx MODULE TIMING CHARACTERISTICS



TABLE 30-28: OCx/PWMx MODE TIMING REQUIREMENTS

AC CHAF	AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$			
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions
OC15	TFD	Fault Input to PWMx I/O Change	—	_	Tcy + 20	ns	
OC20	TFLT	Fault Input Pulse Width	Tcy + 20		—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.



FIGURE 30-19: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS







АС СНА	RACTERI	STICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$			
Param. No. Symbol Characteristic ⁽³⁾				Min.	Max.	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7		μS	
			400 kHz mode	1.3	_	μS	
			1 MHz mode ⁽¹⁾	0.5	_	μS	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	-	μS	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μS	Device must operate at a minimum of 10 MHz
			1 MHz mode ⁽¹⁾	0.5		μS	
IS20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be from
		Fall Time	400 kHz mode	20 + 0.1 CB	300	ns	10 to 400 pF
			1 MHz mode ⁽¹⁾	—	100	ns	
IS21	TR:SCL	SDAx and SCLx	100 kHz mode	—	1000	ns	CB is specified to be from
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF
			1 MHz mode ⁽¹⁾	—	300	ns	
IS25	25 TSU:DAT	Data Input Setup Time	100 kHz mode	250		ns	
			400 kHz mode	100		ns	
			1 MHz mode ⁽¹⁾	100		ns	
IS26	26 THD:DAT	Data Input Hold Time	100 kHz mode	0		μS	
			400 kHz mode	0	0.9	μS	
			1 MHz mode ⁽¹⁾	0	0.3	μS	
IS30	30 Tsu:sta	Start Condition Setup Time	100 kHz mode	4.7		μS	Only relevant for Repeated
			400 kHz mode	0.6		μS	Start condition
			1 MHz mode ⁽¹⁾	0.25	—	μS	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	μS	After this period, the first
			400 kHz mode	0.6	—	μS	clock pulse is generated
			1 MHz mode ⁽¹⁾	0.25	—	μS	
IS33	TSU:STO	Stop Condition	100 kHz mode	4.7	—	μS	
		Setup Time	400 kHz mode	0.6	—	μS	
			1 MHz mode ⁽¹⁾	0.6	—	μS	
IS34	THD:STO	Stop Condition	100 kHz mode	4	—	μS	
		Hold Time	400 kHz mode	0.6	—	μS	
			1 MHz mode ⁽¹⁾	0.25		μS	
IS40	TAA:SCL	Output Valid	100 kHz mode	0	3500	ns	
		From Clock	400 kHz mode	0	1000	ns	
			1 MHz mode ⁽¹⁾	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μS	Time the bus must be free
			400 kHz mode	1.3	—	μS	perore a new transmission
	<u> </u>		1 MHz mode ⁽¹⁾	0.5	—	μS	Call Stall
IS50	Св	Bus Capacitive Lo	ading	—	400	pF	
IS51	TPGD	Pulse Gobbler Delay		65	390	ns	(Note 2)

TABLE 30-50: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

2: Typical value for this parameter is 130 ns.

3: These parameters are characterized, but not tested in manufacturing.



FIGURE 30-38: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SSRCG = 0, SAMC<4:0> = 00010)



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28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch E		0.65 BSC		
Optional Center Pad Width	W2			4.70
Optional Center Pad Length				4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (X28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A

Revision D (December 2011)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

TABLE A-3: MAJOR SECTION UPDATES

Section Name	Update Description
"16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High- Speed PWM, Op amps, and Advanced Analog"	Removed the Analog Comparators column and updated the Op amps/Comparators column in Table 1 and Table 2.
Section 21.0 "Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)"	Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1).
Section 30.0 "Electrical Characteristics"	Updated the VBOR specifications and/or its related note in the following electrical characteristics tables: • Table 30-1 • Table 30-4 • Table 30-12 • Table 30-14 • Table 30-15 • Table 30-16 • Table 30-56 • Table 30-57 • Table 30-58 • Table 30-59 • Table 30-60

Revision H (August 2013)

This revision includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-6.

TABLE A-6:	MAJOR SECTION UPDATES
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Section Name	Update Description
Cover Section	Adds Peripheral Pin Select (PPS) to allow Digital Function Remapping and Change
	Notification Interrupts to Input/Output section
	Adds heading information to 64-Pin TQFP
Section 4.0 "Memory	Corrects Reset values for ANSELE, TRISF, TRISC, ANSELC and TRISA
Organization"	Corrects address range from 0x2FFF to 0x7FFF
	 Corrects DSRPAG and DSWPAG (now 3 hex digits)
	 Changes Call Stack Frame from <15:1> to PC<15:0>
	Word length in Figure 4-20 is changed to 50 words for clarity
Section 5.0 "Flash Program Memory"	Corrects descriptions of NVM registers
Section 9.0 "Oscillator	Removes resistor from Figure 9-1
Configuration"	Adds Fast RC Oscillator with Divide-by-16 (FRCDIV16) row to Table 9-1
	Removes incorrect information from ROI bit in Register 9-2
Section 14.0 "Input Capture"	Changes 31 user-selectable Trigger/Sync interrupts to 19 user-selectable Trigger/ Sync interrupts
	Corrects ICTSEL<12:10> bits (now ICTSEL<2:0>)
Section 17.0 "Quadrature Encoder Interface (QEI)	Corrects QCAPEN bit description
Module	
(dsPIC33EPXXXMC20X/50X	
Devices Only)"	
Section 19.0 "Inter-	Adds note to clarify that 100kbit/sec operation of I ² C is not possible at high processor
Integrated Circuit™ (I ² C™)"	speeds
Section 22.0 "Charge Time Measurement Unit (CTMU)"	Clarifies Figure 22-1 to accurately reflect peripheral behavior
Section 23.0 "10-Bit/12-Bit Analog-to-Digital Converter (ADC)"	Correct Figure 23-1 (changes CH123x to CH123Sx)
Section 24.0 "Peripheral Trigger Generator (PTG) Module"	 Adds footnote to Register 24-1 (In order to operate with CVRSS=1, at least one of the comparator modules must be enabled.
Section 25.0 "Op Amp/ Comparator Module"	• Adds note to Figure 25-3 (In order to operate with CVRSS=1, at least one of the comparator modules must be enabled)
	 Adds footnote to Register 25-2 (COE is not available when OPMODE (CMxCON<10>) = 1)
Section 27.0 "Special Features"	Corrects the bit description for FNOSC<2:0>
Section 30.0 "Electrical	Corrects 512K part power-down currents based on test data
Characteristics"	Corrects WDT timing limits based on LPRC oscillator tolerance
Section 31.0 "High-	Adds Table 31-5 (DC Characteristics: Idle Current (IIDLE)
Temperature Electrical Characteristics"	