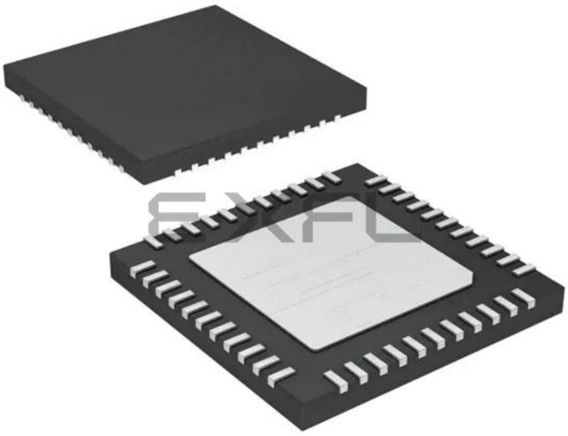
E·XFL

Microchip Technology - DSPIC33EP64MC504-I/ML Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

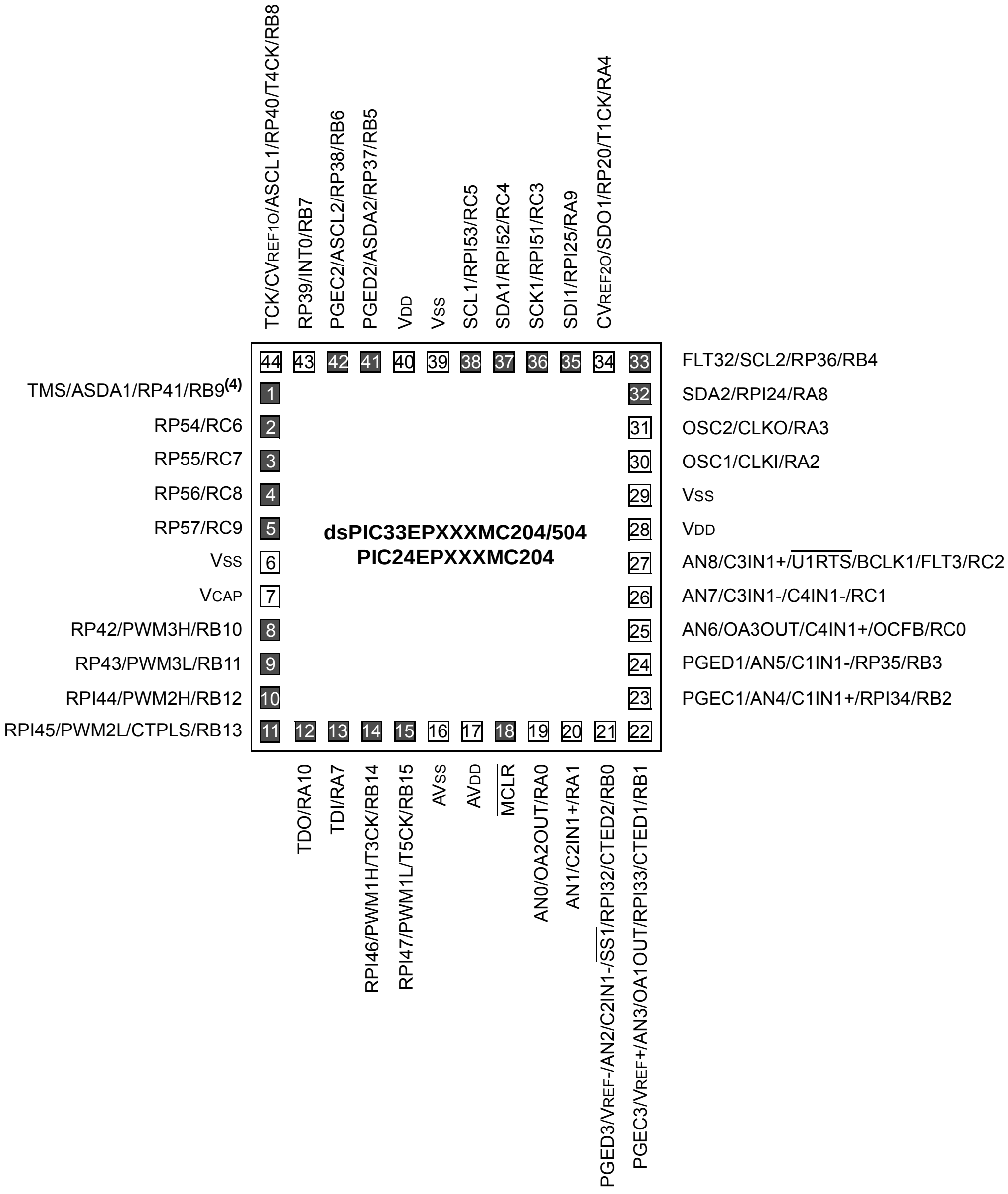
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64mc504-i-ml

Pin Diagrams (Continued)

44-Pin VTLA(1,2,3)

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

FIGURE 2-5: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER

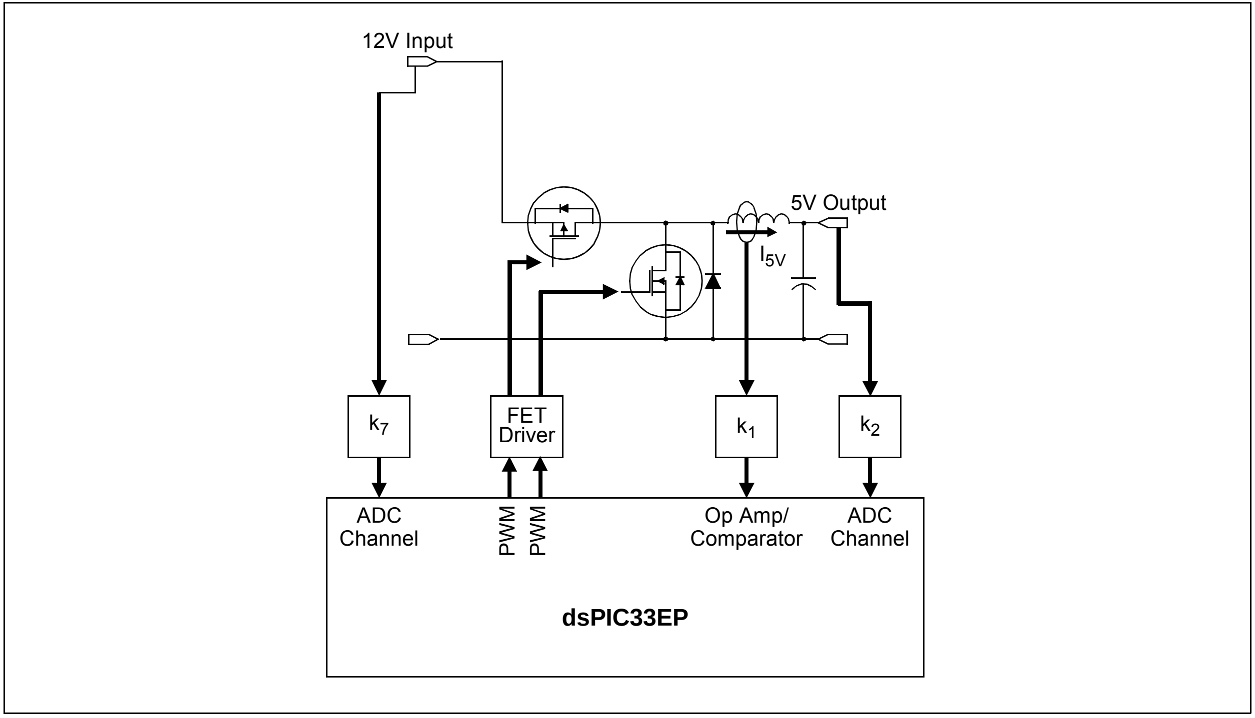


FIGURE 2-6: MULTIPHASE SYNCHRONOUS BUCK CONVERTER

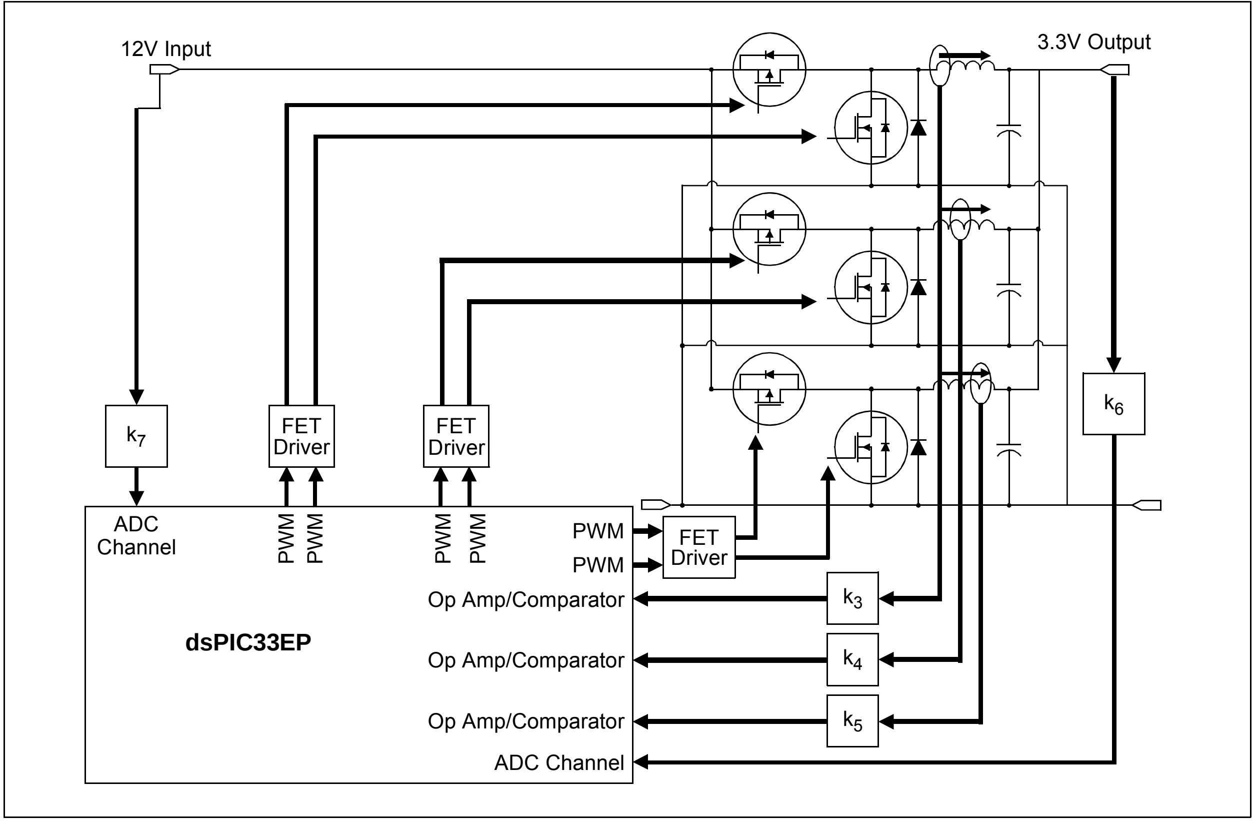


TABLE 4-8: TIMER1 THROUGH TIMER5 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register																`xxxx`
PR1	0102	Period Register 1																`FFFF`
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		—	TSYNC	TCS	—	`0000`
TMR2	0106	Timer2 Register																`xxxx`
TMR3HLD	0108	Timer3 Holding Register (for 32-bit timer operations only)																`xxxx`
TMR3	010A	Timer3 Register																`xxxx`
PR2	010C	Period Register 2																`FFFF`
PR3	010E	Period Register 3																`FFFF`
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		T32	—	TCS	—	`0000`
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		—	—	TCS	—	`0000`
TMR4	0114	Timer4 Register																`xxxx`
TMR5HLD	0116	Timer5 Holding Register (for 32-bit operations only)																`xxxx`
TMR5	0118	Timer5 Register																`xxxx`
PR4	011A	Period Register 4																`FFFF`
PR5	011C	Period Register 5																`FFFF`
T4CON	011E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		T32	—	TCS	—	`0000`
T5CON	0120	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS<1:0>		—	—	TCS	—	`0000`

Legend: `x` = unknown value on Reset, — = unimplemented, read as ‘`0`’. Reset values are shown in hexadecimal.

REGISTER 8-7: DMAxPAD: DMA CHANNEL x PERIPHERAL ADDRESS REGISTER[1]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0	**PAD<15:0>:** Peripheral Address Register bits

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-8: DMAxCNT: DMA CHANNEL x TRANSFER COUNT REGISTER[1]

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CNT<13:8>[2]					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNT<7:0>[2]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14	**Unimplemented:** Read as ‘0’
bit 13-0	**CNT<13:0>:** DMA Transfer Count Register bits[2]

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

2: The number of DMA transfers = CNT<13:0> + 1.

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11.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code, or a complete redesign, may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the label, “RPn” or “RPIn”, in their full pin designation, where “n” is the remappable pin number. “RP” is used to designate pins that support both remappable input and output functions, while “RPI” indicates pins that support remappable input functions only.

11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^{2}C™ and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

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TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)

Input Name[1]	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INT1R<6:0>
External Interrupt 2	INT2	RPINR1	INT2R<6:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<6:0>
Input Capture 1	IC1	RPINR7	IC1R<6:0>
Input Capture 2	IC2	RPINR7	IC2R<6:0>
Input Capture 3	IC3	RPINR8	IC3R<6:0>
Input Capture 4	IC4	RPINR8	IC4R<6:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<6:0>
PWM Fault 1[3]	FLT1	RPINR12	FLT1R<6:0>
PWM Fault 2[3]	FLT2	RPINR12	FLT2R<6:0>
QEI1 Phase A[3]	QEA1	RPINR14	QEA1R<6:0>
QEI1 Phase B[3]	QEB1	RPINR14	QEB1R<6:0>
QEI1 Index[3]	INDX1	RPINR15	INDX1R<6:0>
QEI1 Home[3]	HOME1	RPINR15	HOM1R<6:0>
UART1 Receive	U1RX	RPINR18	U1RXR<6:0>
UART2 Receive	U2RX	RPINR19	U2RXR<6:0>
SPI2 Data Input	SDI2	RPINR22	SDI2R<6:0>
SPI2 Clock Input	SCK2	RPINR22	SCK2R<6:0>
SPI2 Slave Select	$\overline{\text{SS2}}$	RPINR23	SS2R<6:0>
CAN1 Receive[2]	C1RX	RPINR26	C1RXR<6:0>
PWM Sync Input 1[3]	SYNCI1	RPINR37	SYNCI1R<6:0>
PWM Dead-Time Compensation 1[3]	DTCMP1	RPINR38	DTCMP1R<6:0>
PWM Dead-Time Compensation 2[3]	DTCMP2	RPINR39	DTCMP2R<6:0>
PWM Dead-Time Compensation 3[3]	DTCMP3	RPINR39	DTCMP3R<6:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

2: This input source is available on dsPIC33EPXXXGP/MC50X devices only.

3: This input source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

15.2 Output Compare Control Registers

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	ENFLTB
bit 15							bit 8

R/W-0	U-0	R/W-0, HSC	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0
ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **OCSIDL:** Output Compare x Stop in Idle Mode Control bit

1 = Output Compare x Halts in CPU Idle mode
0 = Output Compare x continues to operate in CPU Idle mode

bit 12-10 **OCTSEL<2:0>:** Output Compare x Clock Select bits

111 = Peripheral clock (FP)
110 = Reserved
101 = PTGOx clock[(2)]
100 = T1CLK is the clock source of the OCx (only the synchronous clock is supported)
011 = T5CLK is the clock source of the OCx
010 = T4CLK is the clock source of the OCx
001 = T3CLK is the clock source of the OCx
000 = T2CLK is the clock source of the OCx

bit 9 **Unimplemented:** Read as ‘0’

bit 8 **ENFLTB:** Fault B Input Enable bit

1 = Output Compare Fault B input (OCFB) is enabled
0 = Output Compare Fault B input (OCFB) is disabled

bit 7 **ENFLTA:** Fault A Input Enable bit

1 = Output Compare Fault A input (OCFA) is enabled
0 = Output Compare Fault A input (OCFA) is disabled

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **OCFLTB:** PWM Fault B Condition Status bit

1 = PWM Fault B condition on OCFB pin has occurred
0 = No PWM Fault B condition on OCFB pin has occurred

bit 4 **OCFLTA:** PWM Fault A Condition Status bit

1 = PWM Fault A condition on OCFA pin has occurred
0 = No PWM Fault A condition on OCFA pin has occurred

Note 1: OCxR and OCxRS are double-buffered in PWM mode only.

2: Each Output Compare x module (OCx) has one PTG clock source. See **Section 24.0 “Peripheral Trigger Generator (PTG) Module”** for more information.
PTGO4 = OC1
PTGO5 = OC2
PTGO6 = OC3
PTGO7 = OC4

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32
bit 15							bit 8

R/W-0	R/W-0, HS	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **FLTMD:** Fault Mode Select bit

1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTx bit is cleared in software and a new PWM period starts
0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts

bit 14 **FLTOUT:** Fault Out bit

1 = PWM output is driven high on a Fault
0 = PWM output is driven low on a Fault

bit 13 **FLTTRIEN:** Fault Output State Select bit

1 = OCx pin is tri-stated on a Fault condition
0 = OCx pin I/O state is defined by the FLTOUT bit on a Fault condition

bit 12 **OCINV:** Output Compare x Invert bit

1 = OCx output is inverted
0 = OCx output is not inverted

bit 11-9 **Unimplemented:** Read as ‘0’

bit 8 **OC32:** Cascade Two OCx Modules Enable bit (32-bit operation)

1 = Cascade module operation is enabled
0 = Cascade module operation is disabled

bit 7 **OCTRIG:** Output Compare x Trigger/Sync Select bit

1 = Triggers OCx from the source designated by the SYNCSELx bits
0 = Synchronizes OCx with the source designated by the SYNCSELx bits

bit 6 **TRIGSTAT:** Timer Trigger Status bit

1 = Timer source has been triggered and is running
0 = Timer source has not been triggered and is being held clear

bit 5 **OCTRIS:** Output Compare x Output Pin Direction Select bit

1 = OCx is tri-stated
0 = Output Compare x module drives the OCx pin

Note 1: Do not use the OCx module as its own Synchronization or Trigger source.

2: When the OCy module is turned OFF, it sends a trigger out signal. If the OCx module uses the OCy module as a Trigger source, the OCy module must be unselected as a Trigger source prior to disabling it.

3: Each Output Compare x module (OCx) has one PTG Trigger/Synchronization source. See **Section 24.0 “Peripheral Trigger Generator (PTG) Module”** for more information.
PTGO0 = OC1
PTGO1 = OC2
PTGO2 = OC3
PTGO3 = OC4

19.1 I²C Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

19.1.1 KEY RESOURCES

- **"Inter-Integrated Circuit (I²C)"** (DS70330) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

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REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 3 **S:** Start bit

`1` = Indicates that a Start (or Repeated Start) bit has been detected last
`0` = Start bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.

bit 2 **R_W:** Read/Write Information bit (when operating as I^{2}C slave)

`1` = Read – Indicates data transfer is output from the slave
`0` = Write – Indicates data transfer is input to the slave
Hardware is set or clear after reception of an I^{2}C device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit

`1` = Receive is complete, I2CxRCV is full
`0` = Receive is not complete, I2CxRCV is empty
Hardware is set when I2CxRCV is written with a received byte. Hardware is clear when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit

`1` = Transmit in progress, I2CxTRN is full
`0` = Transmit is complete, I2CxTRN is empty
Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of a data transmission.

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REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0
bit 7							bit 0

Legend:	C = Writable bit, but only ‘0’ can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **RXOVF<15:0>:** Receive Buffer n Overflow bits
`1` = Module attempted to write to a full buffer (set by module)
`0` = No overflow condition (cleared by user software)

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16
bit 7							bit 0

Legend:	C = Writable bit, but only ‘0’ can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **RXOVF<31:16>:** Receive Buffer n Overflow bits
`1` = Module attempted to write to a full buffer (set by module)
`0` = No overflow condition (cleared by user software)

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REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER (CONTINUED)

bit 1 **C2OUT:** Comparator 2 Output Status bit(2)
When CPOL = 0:
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1:
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$

bit 0 **C1OUT:** Comparator 1 Output Status bit(2)
When CPOL = 0:
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1:
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$

Note 1: Reflects the value of the of the CEVT bit in the respective Op Amp/Comparator Control register, CMxCON<9>.

2: Reflects the value of the COUT bit in the respective Op Amp/Comparator Control register, CMxCON<8>.

27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

TABLE 27-3: USER ID WORDS REGISTER MAP

File Name	Address	Bits 23-16	Bits 15-0
FUID0	0x800FF8	—	UID0
FUID1	0x800FFA	—	UID1
FUID2	0x800FFC	—	UID2
FUID3	0x800FFE	—	UID3

Legend: — = unimplemented, read as '1'.

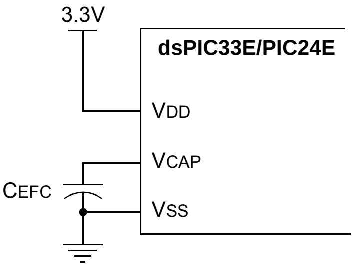
27.3 On-Chip Voltage Regulator

All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in **Section 30.0 "Electrical Characteristics"**.

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR[1,2,3]



Note 1: These are typical operating voltages. Refer to Table 30-5 located in **Section 30.1 "DC Characteristics"** for the full operating ranges of VDD and VCAP.

2: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

3: Typical VCAP pin voltage = 1.8V when VDD ≥ VDDMIN.

27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 30-22 of **Section 30.0 "Electrical Characteristics"** for specific TFSCM values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

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TABLE 30-14: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	10,000	—	—	E/W	-40°C to +125°C
D131	VPR	VDD for Read	3.0	—	3.6	V	
D132b	VPEW	VDD for Self-Timed Write	3.0	—	3.6	V	
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C
D135	IDDP	Supply Current during Programming(2)	—	10	—	mA	
D136	IPEAK	Instantaneous Peak Current During Start-up	—	—	150	mA	
D137a	TPE	Page Erase Time	17.7	—	22.9	ms	TPE = 146893 FRC cycles, TA = +85°C (See **Note 3)**
D137b	TPE	Page Erase Time	17.5	—	23.1	ms	TPE = 146893 FRC cycles, TA = +125°C (See **Note 3)**
D138a	TWW	Word Write Cycle Time	41.7	—	53.8	µs	TWW = 346 FRC cycles, TA = +85°C (See **Note 3)**
D138b	TWW	Word Write Cycle Time	41.2	—	54.4	µs	TWW = 346 FRC cycles, TA = +125°C (See **Note 3)**

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

2: Parameter characterized but not tested in manufacturing.

3: Other conditions: FRC = 7.37 MHz, TUN<5:0> = `011111` (for Minimum), TUN<5:0> = `100000` (for Maximum). This parameter depends on the FRC accuracy (see Table 30-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). For complete details on calculating the Minimum and Maximum time, see **Section 5.3 “Programming Operations”**.

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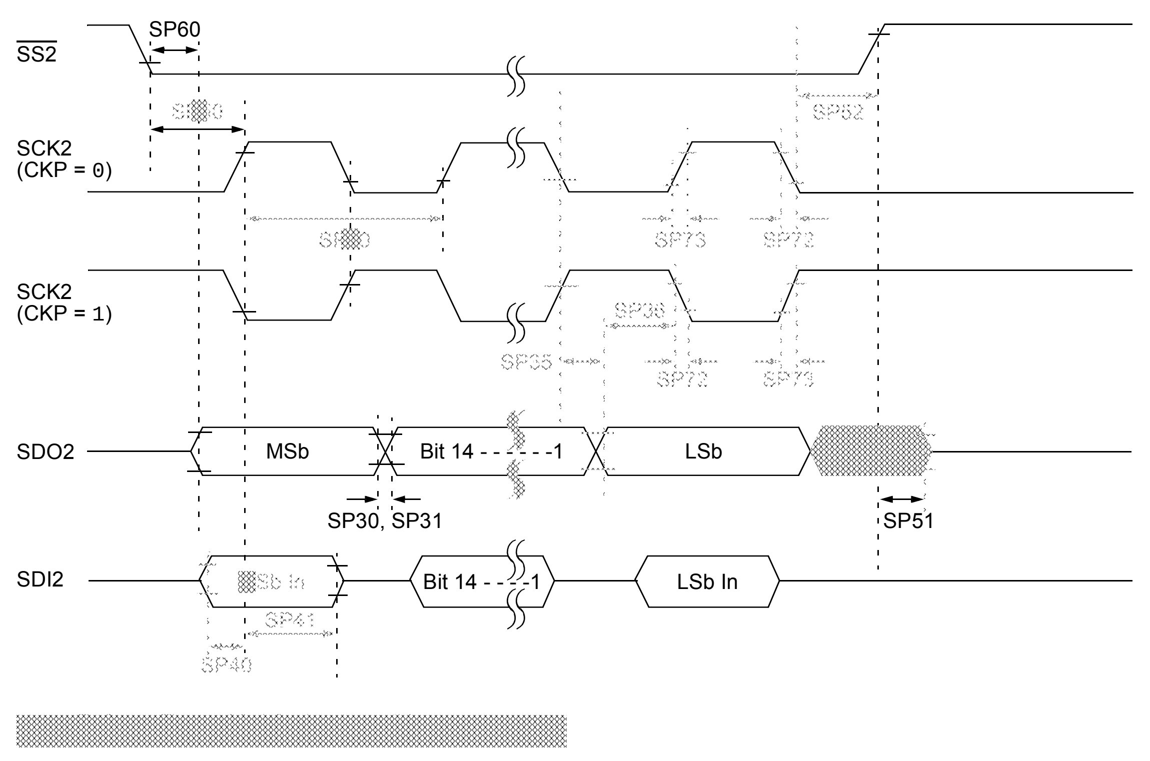
FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



[redacted]

TABLE 30-45: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic[1]**	**Min.**	**Typ.[2]**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK1 Input Frequency	—	—	Lesser of FP or 15	MHz	**(Note 3)**
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{\text{SS1}}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{\text{SS1}}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	**(Note 4)**
SP52	TscH2ssH TscL2ssH	$\overline{\text{SS1}}$ ↑ after SCK1 Edge	1.5 TCY + 40	—	—	ns	**(Note 4)**
SP60	TssL2doV	SDO1 Data Output Valid after $\overline{\text{SS1}}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

TABLE 30-49: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Symbol**	**Characteristic(4)**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TCY/2 (BRG + 2)	—	µs	
			400 kHz mode	TCY/2 (BRG + 2)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 2)	—	µs	
IM11	THI:SCL	Clock High Time	100 kHz mode	TCY/2 (BRG + 2)	—	µs	
			400 kHz mode	TCY/2 (BRG + 2)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 2)	—	µs	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(2)	40	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(2)	0.2	—	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TCY/2 (BRG + 2)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TCY/2 (BRG + 2)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 2)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TCY/2 (BRG + 2)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	TCY/2 (BRG +2)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 2)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TCY/2 (BRG + 2)	—	µs	
			400 kHz mode	TCY/2 (BRG + 2)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 2)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TCY/2 (BRG + 2)	—	µs	
			400 kHz mode	TCY/2 (BRG + 2)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 2)	—	µs	
IM40	TAA:SCL	Output Valid From Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode(2)	—	400	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(2)	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	400	pF	
IM51	TPGD	Pulse Gobbler Delay		65	390	ns	**(Note 3)**

Note 1: BRG is the value of the I^{2}C™ Baud Rate Generator. Refer to **"Inter-Integrated Circuit (I^{2}C™)"** (DS70330) in the "*dsPIC33/PIC24 Family Reference Manual".* Please see the Microchip web site for the latest family reference manual sections.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: Typical value for this parameter is 130 ns.

4: These parameters are characterized, but not tested in manufacturing.

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TABLE 31-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V** **(unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +150°C			
Parameter No.	**Typical**	**Max**	**Units**	**Conditions**		
Power-Down Current (IPD)						
HDC60e	1400	2500	μA	+150°C	3.3V	Base Power-Down Current **(Notes 1, 3)**
HDC61c	15	—	μA	+150°C	3.3V	Watchdog Timer Current: ΔIWDT **(Notes 2, 4)**

Note 1: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled to VSS. WDT, etc., are all switched off and VREGS (RCON<8>) = 1.

2: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

3: These currents are measured on the device containing the most memory in this family.

4: These parameters are characterized, but are not tested in manufacturing.

TABLE 31-5: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V** **(unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +150°C			
Parameter No.	**Typical**	**Max**	**Units**	**Conditions**		
HDC44e	12	30	mA	+150°C	3.3V	40 MIPS

TABLE 31-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V** **(unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +150°C			
Parameter No.	**Typical**	**Max**	**Units**	**Conditions**		
HDC20	9	15	mA	+150°C	3.3V	10 MIPS
HDC22	16	25	mA	+150°C	3.3V	20 MIPS
HDC23	30	50	mA	+150°C	3.3V	40 MIPS

TABLE 31-7: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

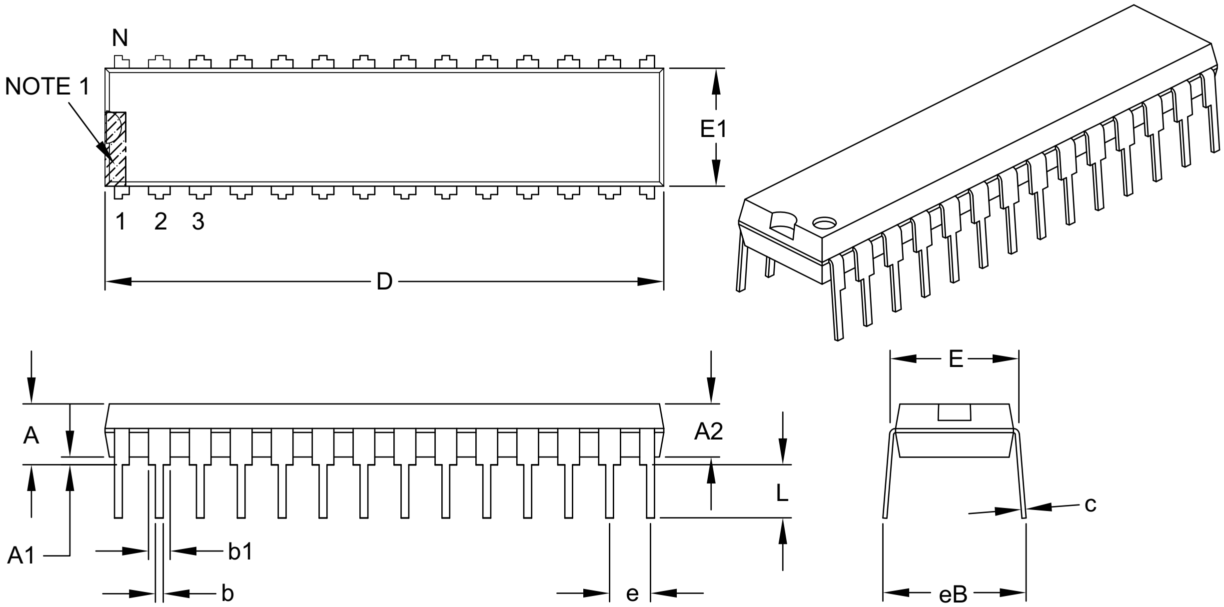
DC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V** **(unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +150°C				
Parameter No.	**Typical**	**Max**	**Doze Ratio**	**Units**	**Conditions**		
HDC72a	24	35	1:2	mA	+150°C	3.3V	40 MIPS
HDC72f[(1)]	14	—	1:64	mA			
HDC72g[(1)]	12	—	1:128	mA			

Note 1: Parameters with Doze ratios of 1:64 and 1:128 are characterized, but are not tested in manufacturing.

33.2 Package Details

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

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Revision F (November 2012)

Removed “Preliminary” from data sheet footer.

Revision G (March 2013)

This revision includes the following global changes:

- changes “$\overline{\text{FLTx}}$” pin function to “FLTx” on all occurrences
- adds **Section 31.0 “High-Temperature Electrical Characteristics”** for high-temperature (+150°C) data

This revision also includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-5.

TABLE A-5: MAJOR SECTION UPDATES

Section Name	Update Description
Cover Section	• Changes internal oscillator specification to 1.0% • Changes I/O sink/source values to 12 mA or 6 mA • Corrects 44-pin VTLA pin diagram (pin 32 now shows as 5V tolerant)
Section 4.0 “Memory Organization”	• Deletes references to Configuration Shadow registers • Corrects the spelling of the JTAGIP and PTGWDTIP bits throughout • Corrects the Reset value of all IOCON registers as C000h • Adds footnote to Table 4-42 to indicate the absence of Comparator 3 in 28-pin devices
Section 6.0 “Resets”	• Removes references to cold and warm Resets, and clarifies the initial configuration of the device clock source on all Resets
Section 7.0 “Interrupt Controller”	• Corrects the definition of GIE as “Global Interrupt Enable” (not “General”)
Section 9.0 “Oscillator Configuration”	• Clarifies the behavior of the CF bit when cleared in software • Removes POR behavior footnotes from all control registers • Corrects the tuning range of the TUN<5:0> bits in Register 9-4 to an overall range ±1.5%
Section 13.0 “Timer2/3 and Timer4/5”	• Clarifies the presence of the ADC Trigger in 16-bit Timer3 and Timer5, as well as the 32-bit timers
Section 15.0 “Output Compare”	• Corrects the first trigger source for SYNCSEL<4:0> (OCxCON2<4:0>) as OCxRS match
Section 16.0 “High-Speed PWM Module”	• Clarifies the source of the PWM interrupts in Figure 16-1 • Corrects the Reset states of IOCONx<15:14> in Register 16-13 as ‘11’
Section 17.0 “Quadrature Encoder Interface (QEI) Module”	• Clarifies the operation of the IMV<1:0> bits (QEICON<9:8>) with updated text and additional notes • Corrects the first prescaler value for QFVDIV<2:0> (QEI1OC<13:11>), now 1:128
Section 23.0 “10-Bit/12-Bit Analog-to-Digital Converter (ADC)”	• Adds note to Figure 23-1 that Op Amp 3 is not available in 28-pin devices • Changes “sample clock” to “sample trigger” in AD1CON1 (Register 23-1) • Clarifies footnotes on op amp usage in Registers 23-5 and 23-6
Section 25.0 “Op Amp/ Comparator Module”	• Adds Note text to indicate that Comparator 3 is unavailable in 28-pin devices • Splits Figure 25-1 into two figures for clearer presentation (Figure 25-1 for Op amp/ Comparators 1 through 3, Figure 25-2 for Comparator 4). Subsequent figures are renumbered accordingly. • Corrects reference description in xxxxx (now ($AV_{DD}+AV_{SS}$)/2) • Changes CMSTAT<15> in Register 25-1 to “PSIDL”
Section 27.0 “Special Features”	• Corrects the addresses of all Configuration bytes for 512 Kbyte devices

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