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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Active
dsPIC
16-Bit
70 MIPs
CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
35
64KB (22K x 24)
FLASH
-
4K x 16
3V ~ 3.6V
A/D 9x10b/12b
Internal
-40°C ~ 85°C (TA)
Surface Mount
48-UFQFN Exposed Pad
48-UQFN (6x6)
https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64mc504-i-mv

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R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR		US1 ⁽¹⁾	US0 ⁽¹⁾	EDT ^(1,2)	DL2 ⁽¹⁾	DL1 ⁽¹⁾	DL0 ⁽¹⁾
bit 15							bit 8
							
R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA(1)	SATB	SATDW ⁽¹⁾	ACCSAT(1)	IPL3(3)	SFA	RND ⁽¹⁾	IF ⁽¹⁾
bit 7							bit 0
Legend:		C - Clearable	hit				
R = Reada	hle hit	W = Writable	hit	U = Unimple	mented hit read	1 as '0'	
-n = Value	at POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
			1				
bit 15	VAR: Variable	e Exception Pro	ocessing Later	ncy Control bit			
	1 = Variable e	exception proce	essing latency	is enabled			
	0 = Fixed exc	eption process	ing latency is	enabled			
bit 14	Unimplemen	ted: Read as '	0'				
bit 13-12	US<1:0>: DS	P Multiply Uns	igned/Signed (Control bits ⁽¹⁾			
	11 = Reserve	ed nine multiplies	are mixed sign	,			
	01 = DSP eng	gine multiplies	are unsigned	1			
	00 = DSP eng	gine multiplies	are signed				
bit 11	EDT: Early DO	D Loop Termina	ation Control bi	it(1,2)			
	1 = Terminate 0 = No effect	es executing DO	loop at end o	f current loop	iteration		
bit 10-8	DL<2:0>: DO	Loop Nesting I	Level Status bi	ts ⁽¹⁾			
	111 = 7 do lo	ops are active					
	•						
	•						
	001 = 1 DO IO	on is active					
	000 = 0 DO lo	ops are active					
bit 7	SATA: ACCA	Saturation En	able bit ⁽¹⁾				
	1 = Accumula 0 = Accumula	ator A saturatio ator A saturatio	n is enabled n is disabled				
bit 6	SATB: ACCB	Saturation En	able bit ⁽¹⁾				
	1 = Accumula	ator B saturatio	n is enabled				
	0 = Accumula	ator B saturatio	n is disabled				
bit 5	SATDW: Data	a Space Write f	from DSP Eng	ine Saturation	Enable bit ⁽¹⁾		
	1 = Data Space	ce write satura ce write satura	tion is enabled tion is disabled	1			
bit 4	ACCSAT: Acc	cumulator Satu	ration Mode S	elect bit ⁽¹⁾			
	1 = 9.31 satu	ration (super sa	aturation)				
	0 = 1.31 satu	ration (normal	saturation)				
bit 3	IPL3: CPU In	terrupt Priority	Level Status b	oit 3 (3)			
	1 = CPU Inter	rrupt Priority Le	evel is greater	than 7			
	0 = CPU inter	riupt Priority Le	evel is / or less	5			
Note 1: 2:	This bit is available This bit is always r	e on dsPIC33E read as '0'.	PXXXMC20X/	50X and dsPI	C33EPXXXGP	50X devices on	ly.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER

3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

TABLE 4	-1:	CPU C	ORE RE	GISTE	R MAP F	OR dsF	PIC33EP	XXXMC	20X/50X	AND d	sPIC33I	EPXXX	GP50X	DEVICE	S ONL	(CON	TINUE	D)
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	Ν	OV	Z	С	0000
CORCON	0044	VAR	_	US<	1:0>	EDT		DL<2:0>		SATA	SATB	SATDW	ACCSAT	IPL3	SFA	RND	IF	0020
MODCON	0046	XMODEN	YMODEN	√ — — BWM<3:0> YWM<3:0> XWM<3:0>								0000						
XMODSRT	0048	XMODSRT<15:0>								_	0000							
XMODEND	004A		XMODEND<15:0>								_	0001						
YMODSRT	004C							YMC	DSRT<15:0	>								0000
YMODEND	004E							YMC	DEND<15:0)>								0001
XBREV	0050	BREN							XBF	REV<14:0>								0000
DISICNT	0052	_	— — DISICNT<13:0>									0000						
TBLPAG	0054		_	_	_	_	_	_	_				TBLPA	G<7:0>				0000
MSTRPR	0058								MSTRPR<	:15:0>								0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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5.2 RTSP Operation

RTSP allows the user application to erase a single page of memory and to program two instruction words at a time. See the General Purpose and Motor Control Family tables (Table 1 and Table 2, respectively) for the page sizes of each device.

For more information on erasing and programming Flash memory, refer to "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual".

5.3 **Programming Operations**

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

For erase and program times, refer to Parameters D137a and D137b (Page Erase Time), and D138a and D138b (Word Write Cycle Time) in Table 30-14 in **Section 30.0 "Electrical Characteristics"**.

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of program Flash memory at a time on every other word address boundary (0x000002, 0x000006, 0x00000A, etc.). To do this, it is necessary to erase the page that contains the desired address of the location the user wants to change.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPS.

Refer to **Flash Programming**" (DS70609) in the "*dsPIC33/PIC24 Family Reference Manual*" for details and codes examples on programming using RTSP.

5.4 Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

5.4.1 KEY RESOURCES

- "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

5.5 Control Registers

Four SFRs are used to erase and write the program Flash memory: NVMCON, NVMKEY, NVMADRH and NVMADRL.

The NVMCON register (Register 5-1) enables and initiates Flash memory erase and write operations.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRH and NVMADRL. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word for programming operations or the selected page for erase operations.

The NVMADRH register is used to hold the upper 8 bits of the EA, while the NVMADRL register is used to hold the lower 16 bits of the EA.

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 3	SLEEP: Wake-up from Sleep Flag bit 1 = Device has been in Sleep mode 0 = Device has not been in Sleep mode
bit 2	IDLE: Wake-up from Idle Flag bit
	1 = Device was in Idle mode0 = Device was not in Idle mode
bit 1	BOR: Brown-out Reset Flag bit 1 = A Brown-out Reset has occurred 0 = A Brown-out Reset has not occurred
bit 0	POR: Power-on Reset Flag bit 1 = A Power-on Reset has occurred 0 = A Power-on Reset has not occurred

- **Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
 - 2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
GIE	DISI	SWTRAP		_	_	_	—
bit 15				·			bit 8
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
		_	_	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0
Legend:	L:1		L:1			(0)	
R = Readable	DIT	vv = vvritable	DIT		mented bit, read	as '0'	
-n = value at I	POR	"1" = Bit is set		$0^{\circ} = Bit is cle$	eared	x = Bit is unkr	nown
hit 15		ntorrunt Enable	, hit				
DIL 15		and associate	d IF hits are e	nahled			
	0 = Interrupts	are disabled,	but traps are s	still enabled			
bit 14	DISI: DISI Ir	nstruction Statu	s bit				
	1 = DISI ins	truction is activ	e				
	0 = DISI ins i	truction is not a	ictive				
bit 13	SWTRAP: So	oftware Trap St	atus bit				
	1 = Software	trap is enabled	4				
hit 12-3		ted. Read as '	 				
bit 2	INT2FP: Exte	ernal Interrupt 2	∘ PEdge Detect	Polarity Selec	et bit		
	1 = Interrupt	on negative ed	ae				
	0 = Interrupt	on positive edg	le				
bit 1	INT1EP: Exte	ernal Interrupt ?	Edge Detect	Polarity Selec	ct bit		
	1 = Interrupt	on negative ed	ge				
	0 = Interrupt	on positive edg	e				
bit 0	INTOEP: Exte	ernal Interrupt () Edge Detect	Polarity Selec	ct bit		
	\perp = interrupt	on negative ed	ye Ie				

REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	—	—	—	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				U1RXR<6:0	>		
bit 7							bit 0

REGISTER 11-10: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 Unimplemented: Read as '0' bit 6-0 U1RXR<6:0>: Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) 1111001 = Input tied to RPI121

REGISTER 11-11: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_		_	—	_	—	_
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				U2RXR<6:0>	>		
bit 7							bit 0
Legend:							

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 Unimplemented: Read as '0'

^{0000000 =} Input tied to Vss

NOTES:

14.2 Input Capture Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	= Hardware Clearable bit HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-14	Unimplemented: Read as '0'
bit 13	ICSIDL: Input Capture Stop in Idle Control bit
	1 = Input capture will Halt in CPU Idle mode
	0 = Input capture will continue to operate in CPU Idle mode
bit 12-10	ICTSEL<2:0>: Input Capture Timer Select bits
	111 = Peripheral clock (FP) is the clock source of the ICx
	110 = Reserved
	101 = Reserved
	100 - 11 CLR is the clock source of the ICx (only the synchronous clock is supported) 011 = T5CLK is the clock source of the ICx
	010 = T4CLK is the clock source of the ICx
	001 = T2CLK is the clock source of the ICx
	000 = T3CLK is the clock source of the ICx
bit 9-7	Unimplemented: Read as '0'
bit 6-5	ICI<1:0>: Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
	11 = Interrupt on every fourth capture event
	10 = Interrupt on every third capture event
	01 = Interrupt on every second capture event
hit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
bit 4	1 = Input capture buffer overflow occurred
	0 = No input capture buffer overflow occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	1 = Input capture buffer is not empty, at least one more capture value can be read
	0 = Input capture buffer is empty
bit 2-0	ICM<2:0>: Input Capture Mode Select bits
	111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
	110 = Unused (module is disabled)
	101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
	100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
	011 = Capture mode, every falling edge (Simple Capture mode)
	001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
	000 = Input capture module is turned off

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			TRGC	/IP<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			TRGC	MP<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as			d as '0'				
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown		nown	

REGISTER 16-14: TRIGX: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER

bit 15-0 TRGCMP<15:0>: Trigger Control Value bits

When the primary PWMx functions in local time base, this register contains the compare values that can trigger the ADC module.

REGISTER 16-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER⁽¹⁾

- bit 7-3 FLTSRC<4:0>: Fault Control Signal Source Select for PWM Generator # bits 11111 = Fault 32 (default) 11110 = Reserved . . 01100 = Reserved 01011 = Comparator 4 01010 = Op Amp/Comparator 3
 - 01001 = Op Amp/Comparator 2
 - 01000 = Op Amp/Comparator 1
 - 00111 = Reserved
 - 00110 = Reserved
 - 00101 = Reserved
 - 00100 = Reserved
 - 00011 = Fault 4
 - 00010 = Fault 3
 - 00001 = Fault 2 00000 = Fault 1
- bit 2 ELTROL Fault Delarity for DWM Concrete

bit 2 **FLTPOL:** Fault Polarity for PWM Generator # bit⁽²⁾

- 1 = The selected Fault source is active-low
- 0 = The selected Fault source is active-high
- bit 1-0 FLTMOD<1:0>: Fault Mode for PWM Generator # bits
 - 11 = Fault input is disabled
 - 10 = Reserved
 - 01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (cycle)
 - 00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (latched condition)
- **Note 1:** If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.
 - **2:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

17.1 QEI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

17.1.1 KEY RESOURCES

- "Quadrature Encoder Interface" (DS70601) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

20.1 UART Helpful Tips

- 1. In multi-node, direct-connect UART networks, receive inputs UART react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
 - a) If URXINV = 0, use a pull-up resistor on the RX pin.
 - b) If URXINV = 1, use a pull-down resistor on the RX pin.
- 2. The first character received on a wake-up from Sleep mode caused by activity on the UxRX pin of the UARTx module will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid; this is to be expected.

20.2 UART Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
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	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

20.2.1 KEY RESOURCES

- "UART" (DS70582) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
_	—	ТХВО	TXBP	RXBP	TXWAR	RXWAR	EWARN
bit 15							bit 8
R/C-0	R/C-0	R/C-0	U-0	R/C-0	R/C-0	R/C-0	R/C-0
IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF
bit 7							bit 0
Legend:	Jend: C = Writable bit, but only '0' can be written to clear the bit						
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							

'0' = Bit is cleared

x = Bit is unknown

REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER

'1' = Bit is set

bit 15-14	Unimplemented: Read as '0'
bit 13	TXBO: Transmitter in Error State Bus Off bit
	1 = Transmitter is in Bus Off state
	0 = Transmitter is not in Bus Off state
bit 12	TXBP: Transmitter in Error State Bus Passive bit
	1 = Transmitter is in Bus Passive state
	0 = Transmitter is not in Bus Passive state
bit 11	RXBP: Receiver in Error State Bus Passive bit
	1 = Receiver is in Bus Passive state
	0 = Receiver is not in Bus Passive state
bit 10	TXWAR: Transmitter in Error State Warning bit
	1 = Transmitter is in Error Warning state
	0 = Transmitter is not in Error Warning state
bit 9	RXWAR: Receiver in Error State Warning bit
	1 = Receiver is in Error Warning state
	0 = Receiver is not in Error Warning state
bit 8	EWARN: Transmitter or Receiver in Error State Warning bit
	1 = Transmitter or receiver is in Error Warning state
	0 = Transmitter or receiver is not in Error Warning state
bit 7	IVRIF: Invalid Message Interrupt Flag bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 6	WAKIF: Bus Wake-up Activity Interrupt Flag bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 5	ERRIF: Error Interrupt Flag bit (multiple sources in CxINTF<13:8>)
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 4	Unimplemented: Read as '0'
bit 3	FIFOIF: FIFO Almost Full Interrupt Flag bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 2	RBOVIF: RX Buffer Overflow Interrupt Flag bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred

-n = Value at POR

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8
R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0

REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

RXOVF4

bit 7			bit 0
Legend:	C = Writable bit, but or	nly '0' can be written to clear the bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	

RXOVF3

RXOVF2

R = Readable bit	vv = vvritable bit	U = Unimplemented bit, read	as 0
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 RXOVF<15:0>: Receive Buffer n Overflow bits

RXOVF6

RXOVF7

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

RXOVF5

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15-0 RXOVF<31:16>: Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

RXOVF0

RXOVF1

REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)

bit 4-0	CH0SA<4:0>: Channel 0 Positive Input Select for Sample MUXA bits ⁽¹⁾									
	11111 = Open; use this selection with CTMU capacitive and time measurement									
	11110 = Channel 0 positive input is connected to the CTMU temperature measurement diode (CTMU TEMP)									
	11101 - Reserved									
	11011 = Reserved									
	11010 = Channel 0 positive input is the output of OA3/AN6 ^(2,3)									
	11001 = Channel 0 positive input is the output of $OA2/AN0^{(2)}$									
	10110 = Channel U positive input is the output of OA1/AN3 ⁽²⁾									
	•									
	•									
	•									
	10000 = Reserved									
	01111 = Channel 0 positive input is AN15 ^(1,3)									
	01110 = Channel 0 positive input is AN14 ^(1,3)									
	01101 = Channel 0 positive input is AN13 ^(1,3)									
	•									
	•									
	• (1 2)									
	00010 = Channel 0 positive input is AN2 ^(1,3)									
	00001 = Channel 0 positive input is AN1(1,3)									
	00000 = Channel 0 positive input is AN0(',3)									

- **Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.
 - 2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.
 - 3: See the "Pin Diagrams" section for the available analog channels for each device.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER

U-0	U-0	U-0 U-0 U-0 R/W-0		R/W-0	R/W-0	RW-0	
—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0
bit 15							bit 8

| R/W-0 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SELSRCB3 | SELSRCB2 | SELSRCB1 | SELSRCB0 | SELSRCA3 | SELSRCA2 | SELSRCA1 | SELSRCA0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 Unimplemented: Read as '0'

bit 11-8	SELSRCC<3:0>: Mask C Input Select bits
	1111 = FLT4
	1110 = FLT2
	1101 = PTGO19
	1100 = PTGO18
	1011 = Reserved
	1010 = Reserved
	1001 = Reserved
	1000 = Reserved
	0111 = Reserved
	0110 = Reserved
	0101 = PWM3H
	0100 = PWM3L
	0011 = PWM2H
	0010 = PWM2L
· · · .	
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0111 = Reserved
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0111 = Reserved 0110 = Reserved 0111 = PW/M3H
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 1000 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3I
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1000 = Reserved 0111 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0101 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2I
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1000 = Reserved 0101 = Reserved 0111 = Reserved 0110 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H
bit 7-4	SELSRCB<3:0>: Mask B Input Select bits 1111 = FLT4 1110 = FLT2 1101 = PTGO19 1100 = PTGO18 1011 = Reserved 1010 = Reserved 1001 = Reserved 0101 = Reserved 0111 = Reserved 0111 = Reserved 0110 = PWM3H 0100 = PWM3L 0011 = PWM2H 0010 = PWM2L 0001 = PWM1H 0000 = PWM1L

File Name	Address	Device Memory Size (Kbytes)	Bits 23-8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0057EC	32									
	00AFEC	64									
	0157EC	128	1 _			_					
	02AFEC	256									
	0557EC	512									
Reserved	0057EE	32									
	00AFEE	64									
	0157EE	128	1 _	_	_	_	_	_	_	_	_
	02AFEE	256									
	0557EE	512									
FICD	0057F0	32									
	00AFF0	64									
	0157F0	128	1 _	Reserved ⁽³⁾	_	JTAGEN	Reserved ⁽²⁾	Reserved ⁽³⁾	_	ICS<	1:0>
	02AFF0	256	-								-
	0557F0	512	-								
FPOR	0057F2	32									
-	00AFF2	64	-						ed(3)		
	0157F2	128	1 <u> </u>	WDTV	VIN<1:0>	ALTI2C2	ALTI2C1	Reserved ⁽³⁾		_	_
	02AFF2	256	-		-		-				
	0557F2	512									
FWDT	0057F4	32									
	00AFF4	64	-								
	0157F4	128	1 _	FWDTEN	WINDIS	PLLKEN	WDTPRE		WDTPOST<3:0>		
	02AFF4	256	-								
	0557F4	512	-								
FOSC	0057F6	32									
	00AFF6	64									
	0157F6	128	_	FCKS	SM<1.0>	IOI 1WAY	_	_	OSCIOENC	POSCMD<1:0>	ID<1.0>
	02AFF6	256							USCIOFING		
	0557F6	512									
FOSCSEL	0057F8	32									
	00AFF8	64									
	0157F8	128	_	IESO		_	_	_	F	NOSC<2.0>	
	02AFF8	256		.200							
	0557E8	512	-								
FGS	0057FA	32									
	00AFFA	64	-								
	0157FA	128	1 _	_	_	_	_	_	_	GCP	GWRP
	02AFFA	256	-							001	oma
	0557EA	512	-								
Reserved	0057EC	32									
1 COCIVCU	00AFEC	64	-								
	0157EC	128						_	_	_	
		256	-								
	0557EC	512									
Reserved	057FFF	32									
1 Coel Ved		64									
		128				_					_
		256									
	055755	512									

TABLE 27-1: CONFIGURATION BYTE REGISTER MAP

Legend: — = unimplemented, read as '1'.

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

2: This bit is reserved and must be programmed as '0'.

3: These bits are reserved and must be programmed as '1'.

30.2 AC Characteristics and Timing Parameters

This section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X AC characteristics and timing parameters.

TABLE 30-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC

	Standard Operating Conditions: 3.0V to 3.6V					
	(unless otherwise stated)					
	Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial					
AC CHARACTERISTICS	$-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
	Operating voltage VDD range as described in Section 30.1 "DC					
	Characteristics".					

FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions
DO50	Cosco	OSC2 Pin	_	—	15	pF	In XT and HS modes, when external clock is used to drive OSC1
DO56	Сю	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	Св	SCLx, SDAx	_		400	pF	In I ² C™ mode

FIGURE 30-17: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS



TABLE 30-36:SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)TIMING REQUIREMENTS

АС СНА	RACTERIST	ICS	Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial1000 states to 105^{\circ}O for State							
	i	<i>"</i>	$-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended							
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions			
SP10	FscP	Maximum SCK2 Frequency	—	—	9	MHz	-40°C to +125°C (Note 3)			
SP20	TscF	SCK2 Output Fall Time	_	_		ns	See Parameter DO32 (Note 4)			
SP21	TscR	SCK2 Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)			
SP30	TdoF	SDO2 Data Output Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)			
SP31	TdoR	SDO2 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)			
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns				
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_	_	ns				
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30			ns				
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30			ns				

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- **3:** The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.
- 4: Assumes 50 pF load on all SPI2 pins.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Microchip Tradema Architecture — Flash Memory Fam Program Memory S Product Group — Pin Count — Tape and Reel Flag Temperature Range Package Pattern	rk ily ize (Kb (if app	dsPI	C 33 EP 64 MC5 04 T 1/PT - XXX	Examples: dsPIC33EP64MC504-I/PT: dsPIC33, Enhanced Performance, 64-Kbyte Program Memory, Motor Control, 44-Pin, Industrial Temperature, TQFP package.
Architecture:	33 24	= =	16-bit Digital Signal Controller 16-bit Microcontroller	
Flash Memory Family:	EP	=	Enhanced Performance	
Product Group:	GP MC	= =	General Purpose family Motor Control family	
Pin Count:	02 03 04 06	= = =	28-pin 36-pin 44-pin 64-pin	
Temperature Range:	l E	= =	-40°C to+85°C (Industrial) -40°C to+125°C (Extended)	
Package:	ML MR MV PT SO SP SS TL TL		Plastic Quad, No Lead Package - (44-pin) 8x8 mm body (QFN) Plastic Quad, No Lead Package - (28-pin) 6x6 mm body (QFN-S) Plastic Quad, No Lead Package - (64-pin) 9x9 mm body (QFN) Thin Quad, No Lead Package - (64-pin) 9x9 mm body (UQFN) Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP) Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP) Plastic Small Outline, Wide - (28-pin) 7.50 mm body (SOIC) Skinny Plastic Dual In-Line - (28-pin) 300 mil body (SPDIP) Plastic Smink Small Outline - (28-pin) 5.30 mm body (SOP) Very Thin Leadless Array - (36-pin) 5x5 mm body (VTLA) Very Thin Leadless Array - (44-pin) 6x6 mm body (VTLA)	