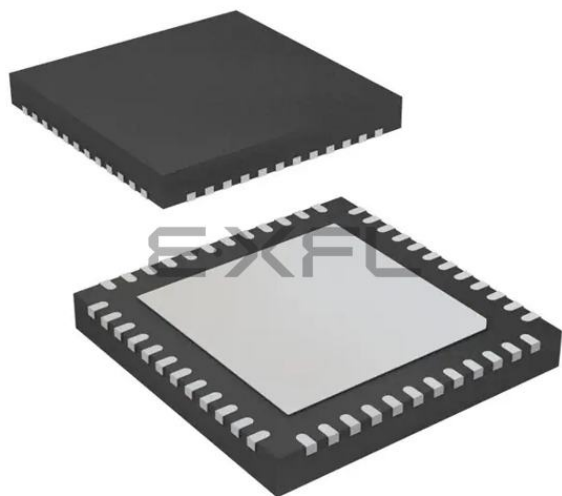




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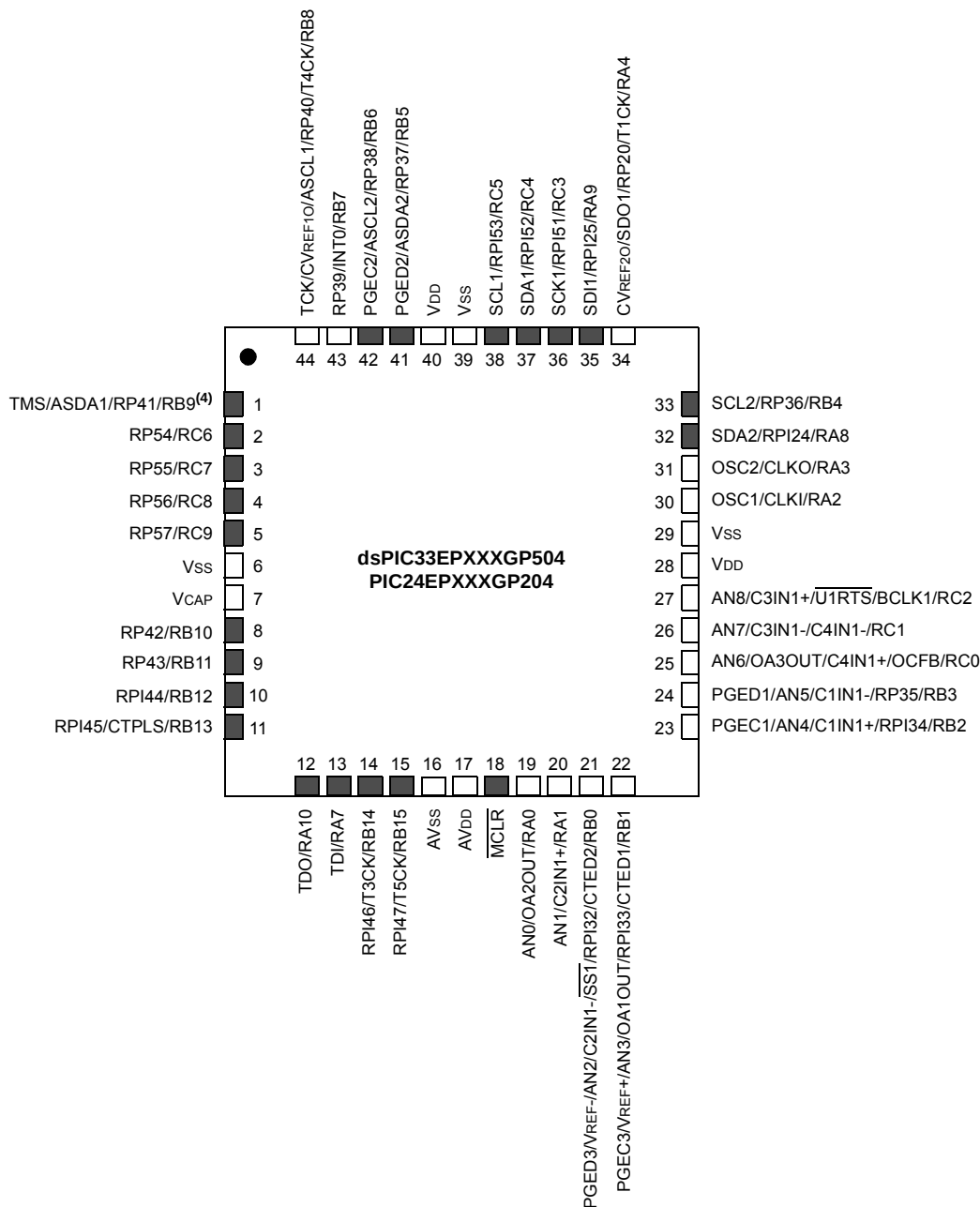
Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64mc504t-i-mv

Pin Diagrams (Continued)

44-Pin QFN^(1,2,3)

■ = Pins are up to 5V tolerant



- Note**
- 1: The RPN/RPI pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See **Section 11.0 “I/O Ports”** for more information.
 - 3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
 - 4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name ⁽⁴⁾	Pin Type	Buffer Type	PPS	Description
C1IN1- C1IN2- C1IN1+ OA1OUT C1OUT	I I I O O	Analog Analog Analog Analog —	No No No No Yes	Op Amp/Comparator 1 Negative Input 1. Comparator 1 Negative Input 2. Op Amp/Comparator 1 Positive Input 1. Op Amp 1 output. Comparator 1 output.
C2IN1- C2IN2- C2IN1+ OA2OUT C2OUT	I I I O O	Analog Analog Analog Analog —	No No No No Yes	Op Amp/Comparator 2 Negative Input 1. Comparator 2 Negative Input 2. Op Amp/Comparator 2 Positive Input 1. Op Amp 2 output. Comparator 2 output.
C3IN1- C3IN2- C3IN1+ OA3OUT C3OUT	I I I O O	Analog Analog Analog Analog —	No No No No Yes	Op Amp/Comparator 3 Negative Input 1. Comparator 3 Negative Input 2. Op Amp/Comparator 3 Positive Input 1. Op Amp 3 output. Comparator 3 output.
C4IN1- C4IN1+ C4OUT	I I O	Analog Analog —	No No Yes	Comparator 4 Negative Input 1. Comparator 4 Positive Input 1. Comparator 4 output.
CVREF10 CVREF20	O O	Analog Analog	No No	Op amp/comparator voltage reference output. Op amp/comparator voltage reference divided by 2 output.
PGED1 PGEC1 PGED2 PGEC2 PGED3 PGEC3	I/O I I/O I I/O I	ST ST ST ST ST ST	No No No No No No	Data I/O pin for Programming/Debugging Communication Channel 1. Clock input pin for Programming/Debugging Communication Channel 1. Data I/O pin for Programming/Debugging Communication Channel 2. Clock input pin for Programming/Debugging Communication Channel 2. Data I/O pin for Programming/Debugging Communication Channel 3. Clock input pin for Programming/Debugging Communication Channel 3.
MCLR	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AVSS	P	P	No	Ground reference for analog modules. This pin must be connected at all times.
VDD	P	—	No	Positive supply for peripheral logic and I/O pins.
VCAP	P	—	No	CPU logic filter capacitor connection.
VSS	P	—	No	Ground reference for logic and I/O pins.
VREF+	I	Analog	No	Analog voltage reference (high) input.
VREF-	I	Analog	No	Analog voltage reference (low) input.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
PPS = Peripheral Pin Select TTL = TTL input buffer

- Note 1:** This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
- Note 2:** This pin is available on dsPIC33EPXXXGP/MC50X devices only.
- Note 3:** This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 “High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”** for more information.
- Note 4:** Not all pins are available in all packages variants. See the “Pin Diagrams” section for pin availability.
- Note 5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

3.8 Arithmetic Logic Unit (ALU)

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X ALU is 16 bits wide, and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the “16-bit MCU and DSC Programmer's Reference Manual” (DS70157) for information on the SR bits affected by each instruction.

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.8.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier, the ALU supports unsigned, signed, or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.8.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.9 DSP Engine (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtractor (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are ADD, SUB and NEG.

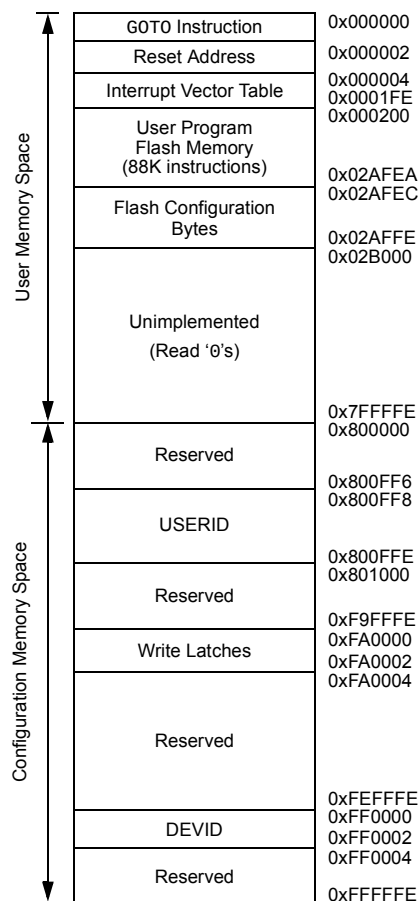
The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or integer DSP multiply (IF)
- Signed, unsigned or mixed-sign DSP multiply (US)
- Conventional or convergent rounding (RND)
- Automatic saturation on/off for ACCA (SATA)
- Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACCSAT)

TABLE 3-2: DSP INSTRUCTIONS SUMMARY

Instruction	Algebraic Operation	ACC Write Back
CLR	$A = 0$	Yes
ED	$A = (x - y)^2$	No
EDAC	$A = A + (x - y)^2$	No
MAC	$A = A + (x \cdot y)$	Yes
MAC	$A = A + x^2$	No
MOVSAC	No change in A	Yes
MPY	$A = x \cdot y$	No
MPY	$A = x^2$	No
MPY.N	$A = -x \cdot y$	No
MSC	$A = A - x \cdot y$	Yes

FIGURE 4-4: PROGRAM MEMORY MAP FOR dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X AND PIC24EP256GP/MC20X DEVICES



Note: Memory areas are not shown to scale.

TABLE 4-27: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC204/504 AND PIC24EPXXXGP/MC204 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP35R<5:0>						—	—	RP20R<5:0>						0000
RPOR1	0682	—	—	RP37R<5:0>						—	—	RP36R<5:0>						0000
RPOR2	0684	—	—	RP39R<5:0>						—	—	RP38R<5:0>						0000
RPOR3	0686	—	—	RP41R<5:0>						—	—	RP40R<5:0>						0000
RPOR4	0688	—	—	RP43R<5:0>						—	—	RP42R<5:0>						0000
RPOR5	068A	—	—	RP55R<5:0>						—	—	RP54R<5:0>						0000
RPOR6	068C	—	—	RP57R<5:0>						—	—	RP56R<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-28: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC206/506 AND PIC24EPXXXGP/MC206 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP35R<5:0>						—	—	RP20R<5:0>						0000
RPOR1	0682	—	—	RP37R<5:0>						—	—	RP36R<5:0>						0000
RPOR2	0684	—	—	RP39R<5:0>						—	—	RP38R<5:0>						0000
RPOR3	0686	—	—	RP41R<5:0>						—	—	RP40R<5:0>						0000
RPOR4	0688	—	—	RP43R<5:0>						—	—	RP42R<5:0>						0000
RPOR5	068A	—	—	RP55R<5:0>						—	—	RP54R<5:0>						0000
RPOR6	068C	—	—	RP57R<5:0>						—	—	RP56R<5:0>						0000
RPOR7	068E	—	—	RP97R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR8	0690	—	—	RP118R<5:0>						—	—	—	—	—	—	—	—	0000
RPOR9	0692	—	—	—	—	—	—	—	—	—	—	RP120R<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-29: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets		
RPINR0	06A0	—	INT1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>								0000	
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>								0000	
RPINR7	06AE	—	IC2R<6:0>								—	IC1R<6:0>								0000
RPINR8	06B0	—	IC4R<6:0>								—	IC3R<6:0>								0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>								0000	
RPINR12	06B8	—	FLT2R<6:0>								—	FLT1R<6:0>								0000
RPINR14	06BC	—	QEB1R<6:0>								—	QEA1R<6:0>								0000
RPINR15	06BE	—	HOME1R<6:0>								—	INDX1R<6:0>								0000
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>								0000	
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>								0000	
RPINR22	06CC	—	SCK2INR<6:0>								—	SDI2R<6:0>								0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>								0000	
RPINR26	06D4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000		
RPINR37	06EA	—	SYNCI1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR38	06EC	—	DTCMP1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR39	06EE	—	DTCMP3R<6:0>								—	DTCMP2R<6:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-30: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets		
RPINR0	06A0	—	INT1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>								0000	
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>								0000	
RPINR7	06AE	—	IC2R<6:0>								—	IC1R<6:0>								0000
RPINR8	06B0	—	IC4R<6:0>								—	IC3R<6:0>								0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>								0000	
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>								0000	
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>								0000	
RPINR22	06CC	—	SCK2INR<6:0>								—	SDI2R<6:0>								0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>								0000	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	RQCOL3	RQCOL2	RQCOL1	RQCOL0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **RQCOL3:** DMA Channel 3 Transfer Request Collision Flag bit
 1 = User force and interrupt-based request collision is detected
 0 = No request collision is detected

bit 2 **RQCOL2:** DMA Channel 2 Transfer Request Collision Flag bit
 1 = User force and interrupt-based request collision is detected
 0 = No request collision is detected

bit 1 **RQCOL1:** DMA Channel 1 Transfer Request Collision Flag bit
 1 = User force and interrupt-based request collision is detected
 0 = No request collision is detected

bit 0 **RQCOL0:** DMA Channel 0 Transfer Request Collision Flag bit
 1 = User force and interrupt-based request collision is detected
 0 = No request collision is detected

REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	—	—	—	—	CMPMD	—	—
bit 15						bit 8	
R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
CRCMD	—	—	—	—	—	I2C2MD	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10 **CMPMD:** Comparator Module Disable bit
1 = Comparator module is disabled
0 = Comparator module is enabled
- bit 9-8 **Unimplemented:** Read as '0'
- bit 7 **CRCMD:** CRC Module Disable bit
1 = CRC module is disabled
0 = CRC module is enabled
- bit 6-2 **Unimplemented:** Read as '0'
- bit 1 **I2C2MD:** I2C2 Module Disable bit
1 = I2C2 module is disabled
0 = I2C2 module is enabled
- bit 0 **Unimplemented:** Read as '0'

REGISTER 10-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15						bit 8	
U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
—	—	—	—	REFOMD	CTMUMD	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-4 **Unimplemented:** Read as '0'
- bit 3 **REFOMD:** Reference Clock Module Disable bit
1 = Reference clock module is disabled
0 = Reference clock module is enabled
- bit 2 **CTMUMD:** CTMU Module Disable bit
1 = CTMU module is disabled
0 = CTMU module is enabled
- bit 1-0 **Unimplemented:** Read as '0'

11.0 I/O PORTS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “I/O Ports” (DS70598) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

Many of the device pins are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

11.1 Parallel I/O (PIO) Ports

Generally, a parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port

has ownership of the output data and control signals of the I/O pin. The logic also prevents “loop through,” in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

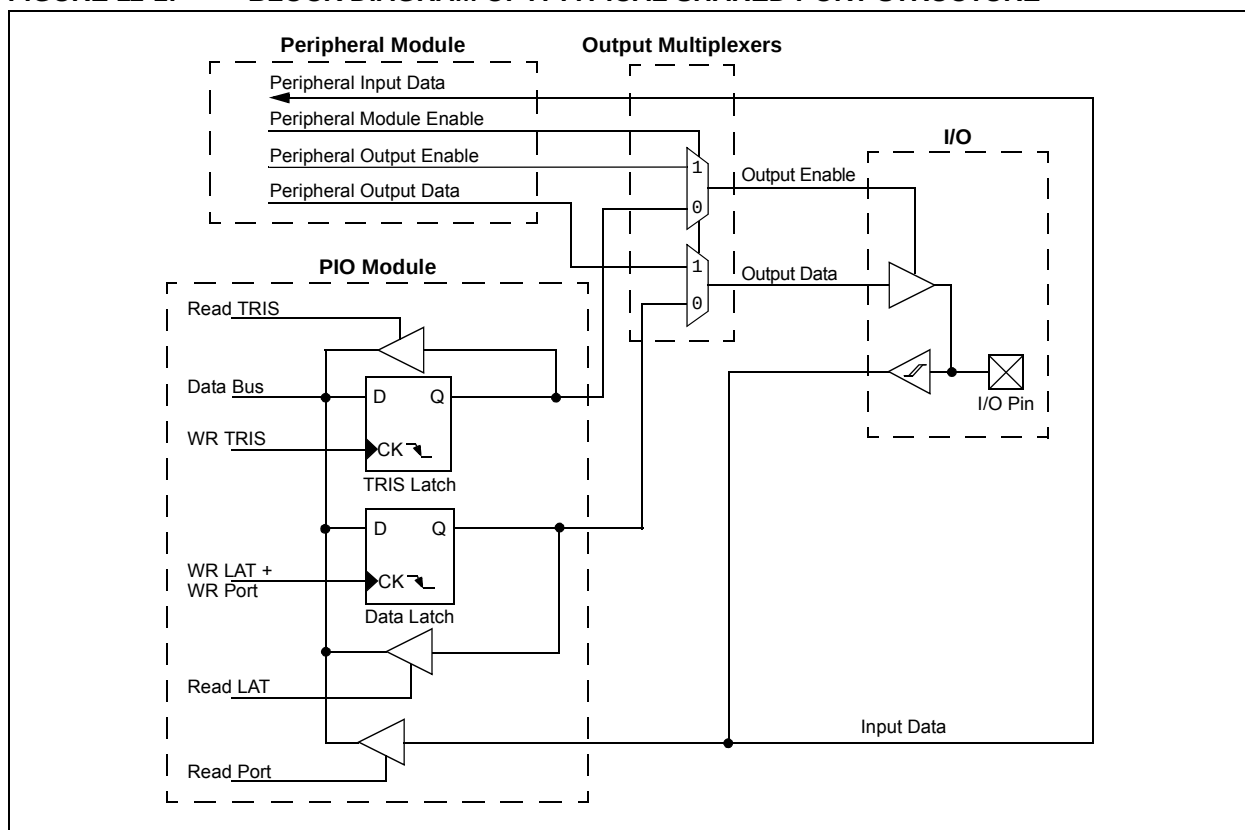
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have eight registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a ‘1’, then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the Latch register (LATx) read the latch. Writes to the Latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device is disabled. This means the corresponding LATx and TRISx registers and the port pin are read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



REGISTER 16-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER⁽¹⁾

- bit 7-3 **FLTSRC<4:0>**: Fault Control Signal Source Select for PWM Generator # bits
11111 = Fault 32 (**default**)
11110 = Reserved
.
.
.
01100 = Reserved
01011 = Comparator 4
01010 = Op Amp/Comparator 3
01001 = Op Amp/Comparator 2
01000 = Op Amp/Comparator 1
00111 = Reserved
00110 = Reserved
00101 = Reserved
00100 = Reserved
00011 = Fault 4
00010 = Fault 3
00001 = Fault 2
00000 = Fault 1
- bit 2 **FLTPOL**: Fault Polarity for PWM Generator # bit⁽²⁾
1 = The selected Fault source is active-low
0 = The selected Fault source is active-high
- bit 1-0 **FLTMOD<1:0>**: Fault Mode for PWM Generator # bits
11 = Fault input is disabled
10 = Reserved
01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (cycle)
00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (latched condition)

- Note 1:** If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.
- 2:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

19.1 I²C Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464
--

19.1.1 KEY RESOURCES

- **“Inter-Integrated Circuit (I²C)”** (DS70330) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

24.0 PERIPHERAL TRIGGER GENERATOR (PTG) MODULE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **“Peripheral Trigger Generator (PTG)”** (DS70669) in the *“dsPIC33/PIC24 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

24.1 Module Introduction

The Peripheral Trigger Generator (PTG) provides a means to schedule complex high-speed peripheral operations that would be difficult to achieve using software. The PTG module uses 8-bit commands, called “Steps”, that the user writes to the PTG Queue registers (PTGQUE0-PTGQUE7), which perform operations, such as wait for input signal, generate output trigger and wait for timer.

The PTG module has the following major features:

- Multiple clock sources
- Two 16-bit general purpose timers
- Two 16-bit general limit counters
- Configurable for rising or falling edge triggering
- Generates processor interrupts to include:
 - Four configurable processor interrupts
 - Interrupt on a Step event in Single-Step mode
 - Interrupt on a PTG Watchdog Timer time-out
- Able to receive trigger signals from these peripherals:
 - ADC
 - PWM
 - Output Compare
 - Input Capture
 - Op Amp/Comparator
 - INT2
- Able to trigger or synchronize to these peripherals:
 - Watchdog Timer
 - Output Compare
 - Input Capture
 - ADC
 - PWM
 - Op Amp/Comparator

26.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Programmable Cyclic Redundancy Check (CRC)**” (DS70346) of the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The programmable CRC generator offers the following features:

- User-programmable (up to 32nd order) polynomial CRC equation
- Interrupt output
- Data FIFO

The programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-programmable CRC polynomial equation, up to 32 bits
- Programmable shift direction (little or big-endian)
- Independent data and polynomial lengths
- Configurable interrupt output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 26-1. A simple version of the CRC shift engine is shown in Figure 26-2.

FIGURE 26-1: CRC BLOCK DIAGRAM

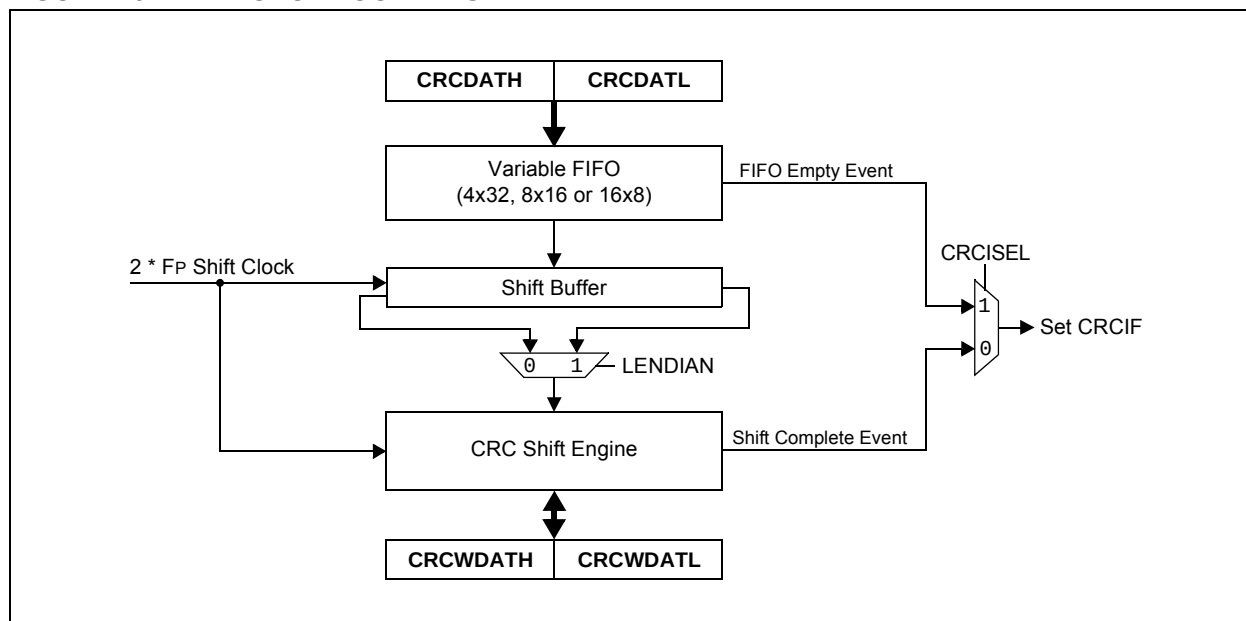


FIGURE 30-3: I/O TIMING CHARACTERISTICS

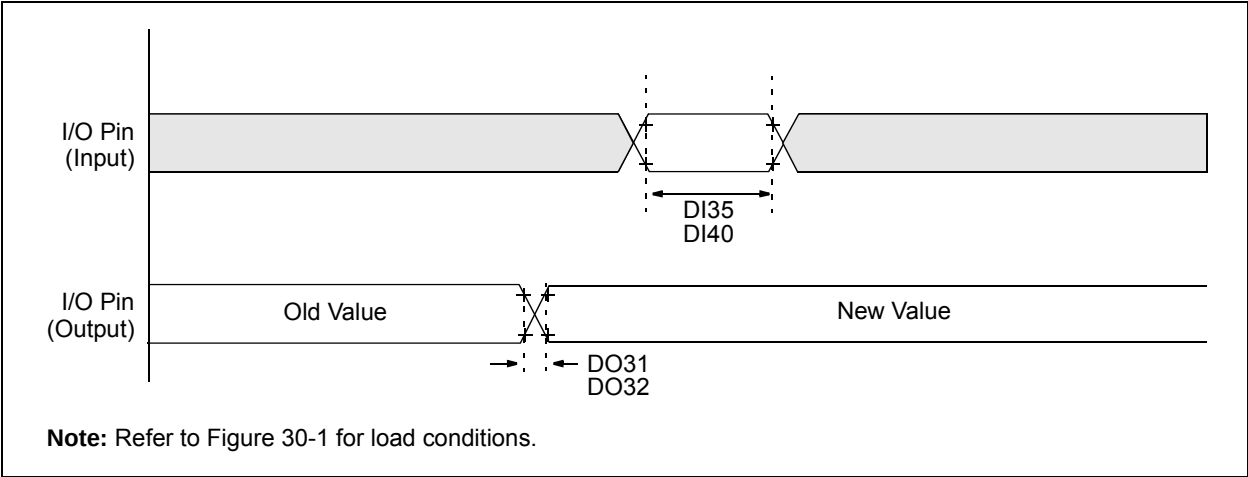
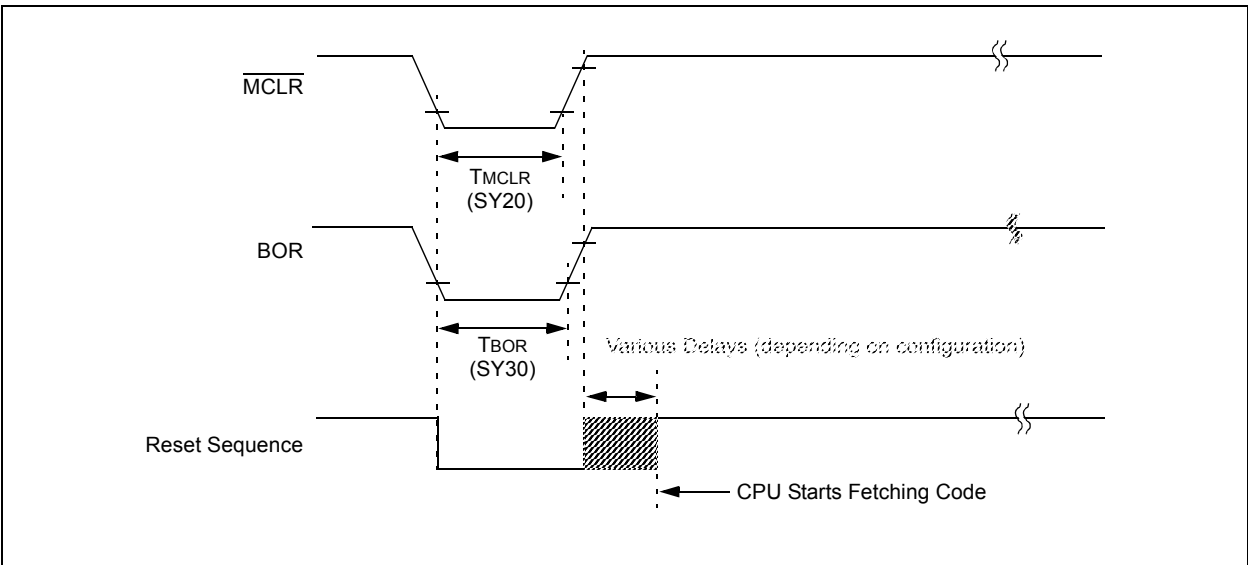


TABLE 30-21: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Param No.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
DO31	TioR	Port Output Rise Time	—	5	10	ns	
DO32	TioF	Port Output Fall Time	—	5	10	ns	
DI35	TINP	INTx Pin High or Low Time (input)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	Tcy	

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

FIGURE 30-4: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS



**FIGURE 30-29: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)
TIMING CHARACTERISTICS**

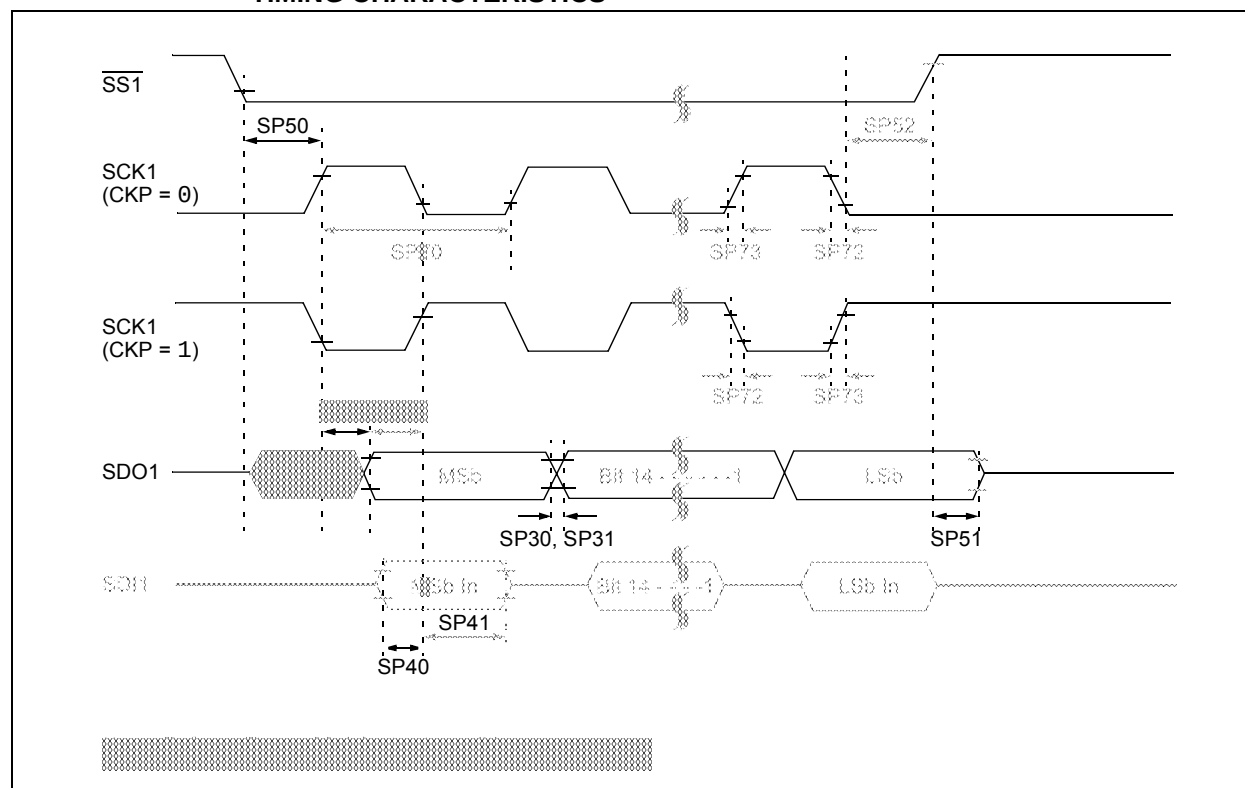


TABLE 31-8: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
HDO10	VOL	Output Low Voltage 4x Sink Driver Pins ⁽²⁾	—	—	0.4	V	$I_{OL} \leq 5 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
		Output Low Voltage 8x Sink Driver Pins ⁽³⁾	—	—	0.4	V	$I_{OL} \leq 8 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
HDO20	VOH	Output High Voltage 4x Source Driver Pins ⁽²⁾	2.4	—	—	V	$I_{OH} \geq -10 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
		Output High Voltage 8x Source Driver Pins ⁽³⁾	2.4	—	—	V	$I_{OH} \geq 15 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
HDO20A	VOH1	Output High Voltage 4x Source Driver Pins ⁽²⁾	1.5	—	—	V	$I_{OH} \geq -3.9 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
			2.0	—	—		$I_{OH} \geq -3.7 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
			3.0	—	—		$I_{OH} \geq -2 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
		Output High Voltage 8x Source Driver Pins ⁽³⁾	1.5	—	—	V	$I_{OH} \geq -7.5 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
			2.0	—	—		$I_{OH} \geq -6.8 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
			3.0	—	—		$I_{OH} \geq -3 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)

Note 1: Parameters are characterized, but not tested.

2: Includes all I/O pins that are not 8x Sink Driver pins (see below).

3: Includes the following pins:

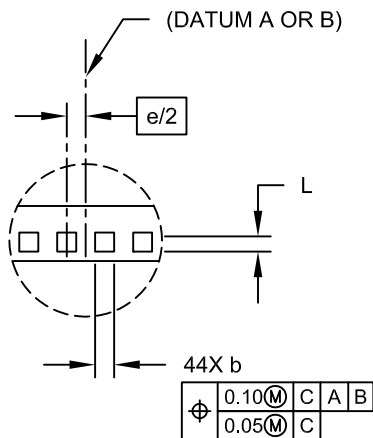
For devices with less than 64 pins: RA3, RA4, RA9, RB<15:7> and RC3

For 64-pin devices: RA4, RA9, RB<15:7>, RC3 and RC15

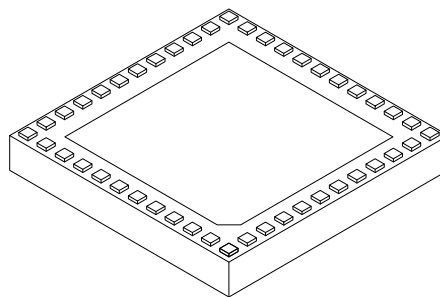
NOTES:

44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



DETAIL A



	Units	MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N	44		
Number of Pins per Side	ND	12		
Number of Pins per Side	NE	10		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.025	-	0.075
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	4.40	4.55	4.70
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	4.40	4.55	4.70
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-157C Sheet 2 of 2

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