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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

⊡XFI

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128gp202-i-mm

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Name ⁽⁴⁾	Pin Type	Buffer Type	PPS	Description
C1IN1-	Ι	Analog	No	Op Amp/Comparator 1 Negative Input 1.
C1IN2-	I	Analog	No	Comparator 1 Negative Input 2.
C1IN1+	I	Analog	No	Op Amp/Comparator 1 Positive Input 1.
OA1OUT	0	Analog	No	Op Amp 1 output.
C10UT	0		Yes	Comparator 1 output.
C2IN1-	Ι	Analog	No	Op Amp/Comparator 2 Negative Input 1.
C2IN2-	I.	Analog	No	Comparator 2 Negative Input 2.
C2IN1+	I.	Analog	No	Op Amp/Comparator 2 Positive Input 1.
OA2OUT	0	Analog	No	Op Amp 2 output.
C2OUT	0	—	Yes	Comparator 2 output.
C3IN1-	I	Analog	No	Op Amp/Comparator 3 Negative Input 1.
C3IN2-	I	Analog	No	Comparator 3 Negative Input 2.
C3IN1+	I	Analog	No	Op Amp/Comparator 3 Positive Input 1.
OA3OUT	0	Analog	No	Op Amp 3 output.
C3OUT	0		Yes	Comparator 3 output.
C4IN1-	I	Analog	No	Comparator 4 Negative Input 1.
C4IN1+	I	Analog	No	Comparator 4 Positive Input 1.
C4OUT	0	—	Yes	Comparator 4 output.
CVREF10	0	Analog	No	Op amp/comparator voltage reference output.
CVREF20	0	Analog	No	Op amp/comparator voltage reference divided by 2 output.
PGED1	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 1.
PGEC1	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 1.
PGED2	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 2.
PGEC2		SI	No	Clock input pin for Programming/Debugging Communication Channel 2.
PGED3	1/0	SI	NO	Data I/O pin for Programming/Debugging Communication Channel 3.
PGEC3	1	51	NO	Clock input pin for Programming/Debugging Communication Channel 3.
MCLR	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	Р	Р	No	Positive supply for analog modules. This pin must be connected at all times.
AVss	Р	Р	No	Ground reference for analog modules. This pin must be connected at all times.
Vdd	Р		No	Positive supply for peripheral logic and I/O pins.
VCAP	Р		No	CPU logic filter capacitor connection.
Vss	Р		No	Ground reference for logic and I/O pins.
VREF+	Ι	Analog	No	Analog voltage reference (high) input.
VREF-	Ι	Analog	No	Analog voltage reference (low) input.
Legend: CMOS = C	MOS co	ompatible	e input	or output Analog = Analog input P = Power
ST = Schmi	tt Trigg	jer input v	with Cl	MOS levels O = Output I = Input

TABLE 1-1:	PINOUT I/O DESCRIPTIONS	(CONTINUED)
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Note 1: This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This pin is available on dsPIC33EPXXXGP/MC50X devices only.

PPS = Peripheral Pin Select

3: This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)" for more information.

TTL = TTL input buffer

4: Not all pins are available in all packages variants. See the "Pin Diagrams" section for pin availability.

5: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

FIGURE 2-5: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER







3.6 CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

3.6.1 KEY RESOURCES

- "CPU" (DS70359) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

TABLE 4-24: CRC REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	it 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit							Bit 0	All Resets				
CRCCON1	0640	CRCEN	—	CSIDL		V	WORD<4:()>		CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	-	—	0000
CRCCON2	0642	_	_	_		D	WIDTH<4:0)>		_	_	_		F	PLEN<4:0>			0000
CRCXORL	0644								X<15:1	>							_	0000
CRCXORH	0646								X	<31:16>								0000
CRCDATL	0648								CRC Data	Input Low V	Vord							0000
CRCDATH	064A		CRC Data Input High Word 000							0000								
CRCWDATL	064C		CRC Result Low Word 0000								0000							
CRCWDATH	064E		CRC Result High Word 0000							0000								

Legend: — = unimplemented, read as '0'. Shaded bits are not used in the operation of the programmable CRC module.

TABLE 4-25: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC202/502 AND PIC24EPXXXGP/MC202 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	_	—			RP35F	R<5:0>			—	—			RP20F	R<5:0>			0000
RPOR1	0682	_	_			RP37F	२<5:0>			—	_			RP36F	२<5:0>			0000
RPOR2	0684	_	_			RP39F	२<5:0>			—	_		RP38R<5:0>					
RPOR3	0686	_	_		RP41R<5:0>			—	_	RP40R<5:0>						0000		
RPOR4	0688	_	—		RP43R<5:0>			_	_			RP42F	२<5:0>			0000		

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-26: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC203/503 AND PIC24EPXXXGP/MC203 DEVICES ONLY DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	_			RP35	R<5:0>			_	_			RP20	R<5:0>			0000
RPOR1	0682	_	_			RP37	२<5:0>			_	_			RP36	२<5:0>			0000
RPOR2	0684	_	_			RP39	२<5:0>			_	_			RP38	२<5:0>			0000
RPOR3	0686	_	_			RP41	२<5:0>			_	_			RP40	२<5:0>			0000
RPOR4	0688	_	_			RP43	२<5:0>			_	_			RP42	२<5:0>			0000
RPOR5	068A	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
RPOR6	068C			-	—	_		—			_	RP56R<5:0>					0000	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-46: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	TRISA12	TRISA11	TRISA10	TRISA9	TRISA8	TRISA7	—	—	TRISA4	-	—	TRISA1	TRISA0	1F93
PORTA	0E02	_	_	_	RA12	RA11	RA10	RA9	RA8	RA7	_	_	RA4	_	_	RA1	RA0	0000
LATA	0E04	_	_	_	LATA12	LATA11	LATA10	LATA9	LATA8	LATA7	_	_	LATA4	_	_	LA1TA1	LA0TA0	0000
ODCA	0E06	_	_	_	ODCA12	ODCA11	ODCA10	ODCA9	ODCA8	ODCA7	_	_	ODCA4	_	_	ODCA1	ODCA0	0000
CNENA	0E08	_	_	_	CNIEA12	CNIEA11	CNIEA10	CNIEA9	CNIEA8	CNIEA7	_	_	CNIEA4	_	_	CNIEA1	CNIEA0	0000
CNPUA	0E0A	_	_	_	CNPUA12	CNPUA11	CNPUA10	CNPUA9	CNPUA8	CNPUA7	_	_	CNPUA4	_	_	CNPUA1	CNPUA0	0000
CNPDA	0E0C	_	_	_	CNPDA12	CNPDA11	CNPDA10	CNPDA9	CNPDA8	CNPDA7	_	_	CNPDA4	_	_	CNPDA1	CNPDA0	0000
ANSELA	0E0E	_	_	—	ANSA12	ANSA11	—	_	_	—		—	ANSA4	-	_	ANSA1	ANSA0	1813

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-47: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	_	_	_	_	-	_	_	ANSB8		—	-		ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-48: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	TRISC15	_	TRISC13	TRISC12	TRISC11	TRISC10	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	BFFF
PORTC	0E22	RC15	-	RC13	RC12	RC11	RC10	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	0E24	LATC15		LATC13	LATC12	LATC11	LATC10	LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
ODCC	0E26	ODCC15	_	ODCC13	ODCC12	ODCC11	ODCC10	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000
CNENC	0E28	CNIEC15	_	CNIEC13	CNIEC12	CNIEC11	CNIEC10	CNIEC9	CNIEC8	CNIEC7	CNIEC6	CNIEC5	CNIEC4	CNIEC3	CNIEC2	CNIEC1	CNIEC0	0000
CNPUC	0E2A	CNPUC15	_	CNPUC13	CNPUC12	CNPUC11	CNPUC10	CNPUC9	CNPUC8	CNPUC7	CNPUC6	CNPUC5	CNPUC4	CNPUC3	CNPUC2	CNPUC1	CNPUC0	0000
CNPDC	0E2C	CNPDC15	_	CNPDC13	CNPDC12	CNPDC11	CNPDC10	CNPDC9	CNPDC8	CNPDC7	CNPDC6	CNPDC5	CNPDC4	CNPDC3	CNPDC2	CNPDC1	CNPDC0	0000
ANSELC	0E2E		-	-	—	ANSC11	_		_	—	—	_		—	ANSC2	ANSC1	ANSC0	0807

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.3 DATA MEMORY ARBITRATION AND BUS MASTER PRIORITY

EDS accesses from bus masters in the system are arbitrated.

The arbiter for data memory (including EDS) arbitrates between the CPU, the DMA and the ICD module. In the event of coincidental access to a bus by the bus masters, the arbiter determines which bus master access has the highest priority. The other bus masters are suspended and processed after the access of the bus by the bus master with the highest priority.

By default, the CPU is Bus Master 0 (M0) with the highest priority and the ICD is Bus Master 4 (M4) with the lowest priority. The remaining bus master (DMA Controller) is allocated to M3 (M1 and M2 are reserved and cannot be used). The user application may raise or lower the priority of the DMA Controller to be above that of the CPU by setting the appropriate bits in the EDS Bus Master Priority Control (MSTRPR) register. All bus masters with raised priorities will maintain the same priority relationship relative to each other (i.e., M1 being highest and M3 being lowest, with M2 in between). Also, all the bus masters with priorities below

FIGURE 4-18: ARBITER ARCHITECTURE

that of the CPU maintain the same priority relationship relative to each other. The priority schemes for bus masters with different MSTRPR values are tabulated in Table 4-62.

This bus master priority control allows the user application to manipulate the real-time response of the system, either statically during initialization or dynamically in response to real-time events.

TABLE 4-62:	DATA MEMORY BUS
	ARBITER PRIORITY

Briority	MSTRPR<15:0	> Bit Setting ⁽¹⁾					
Phoney	0x0000	0x0020					
M0 (highest)	CPU	DMA					
M1	Reserved	CPU					
M2	Reserved	Reserved					
M3	DMA	Reserved					
M4 (lowest)	ICD	ICD					

Note 1: All other values of MSTRPR<15:0> are reserved.



In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receives a request to transfer data, a simple fixed priority scheme based on channel number, dictates which channel completes the transfer and which channel, or channels, are left pending. Each DMA channel moves a block of data, after which, it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA Controller provides these functional capabilities:

- Four DMA channels
- Register Indirect with Post-Increment Addressing mode
- Register Indirect without Post-Increment Addressing mode

- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU interrupt after half or full block transfer complete
- Byte or word transfers
- · Fixed priority channel arbitration
- Manual (software) or automatic (peripheral DMA requests) transfer initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two SRAM start addresses after each block transfer is complete)
- DMA request for each channel can be selected from any supported interrupt source
- Debug support features

The peripherals that can utilize DMA are listed in Table 8-1.

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
INT0 – External Interrupt 0	00000000	—	—
IC1 – Input Capture 1	0000001	0x0144 (IC1BUF)	—
IC2 – Input Capture 2	00000101	0x014C (IC2BUF)	_
IC3 – Input Capture 3	00100101	0x0154 (IC3BUF)	—
IC4 – Input Capture 4	00100110	0x015C (IC4BUF)	—
OC1 – Output Compare 1	00000010	_	0x0906 (OC1R) 0x0904 (OC1RS)
OC2 – Output Compare 2	00000110	_	0x0910 (OC2R) 0x090E (OC2RS)
OC3 – Output Compare 3	00011001	_	0x091A (OC3R) 0x0918 (OC3RS)
OC4 – Output Compare 4	00011010	_	0x0924 (OC4R) 0x0922 (OC4RS)
TMR2 – Timer2	00000111	—	—
TMR3 – Timer3	00001000	—	—
TMR4 – Timer4	00011011	_	—
TMR5 – Timer5	00011100	—	—
SPI1 Transfer Done	00001010	0x0248 (SPI1BUF)	0x0248 (SPI1BUF)
SPI2 Transfer Done	00100001	0x0268 (SPI2BUF)	0x0268 (SPI2BUF)
UART1RX – UART1 Receiver	00001011	0x0226 (U1RXREG)	—
UART1TX – UART1 Transmitter	00001100	—	0x0224 (U1TXREG)
UART2RX – UART2 Receiver	00011110	0x0236 (U2RXREG)	—
UART2TX – UART2 Transmitter	00011111	—	0x0234 (U2TXREG)
ECAN1 – RX Data Ready	00100010	0x0440 (C1RXD)	
ECAN1 – TX Data Request	01000110	—	0x0442 (C1TXD)
ADC1 – ADC1 Convert Done	00001101	0x0300 (ADC1BUF0)	_

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—	—	—		—	—	—			
bit 15							bit 8		
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0		
		<u> </u>		RQCOL3	RQCOL2	RQCOL1	RQCOL0		
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'					
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown			
bit 15-4	Unimplemen	ted: Read as '	י)						
bit 3	RQCOL3: DM	IA Channel 3 T	ransfer Requ	est Collision Fl	lag bit				
	1 = User forc	e and interrupt	-based reques	st collision is d	etected				
	0 = No reque	est collision is d	etected						
bit 2	RQCOL2: DM	IA Channel 2 T	ransfer Requ	est Collision Fl	lag bit				
	1 = User force and interrupt-based request collision is detected								
	0 = No reque	est collision is d	etected						
bit 1	RQCOL1: DMA Channel 1 Transfer Request Collision Flag bit								
	1 = User forc 0 = No reque	e and interrupt st collision is d	-based reques etected	st collision is d	etected				
bit 0	RQCOL0: DM	1A Channel 0 T	ransfer Requ	est Collision Fl	lag bit				
	1 = User forc	e and interrupt	-based reques	st collision is d	etected				

REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER

0 = No request collision is detected

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
		_	_	_	_	_	PLLDIV8
bit 15		·					bit 8
R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
PLLDIV7	PLLDIV6	PLLDIV5	PLLDIV4	PLLDIV3	PLLDIV2	PLLDIV1	PLLDIV0
bit 7		·					bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	
bit 15-9	Unimplemen	ted: Read as '	0'				
bit 8-0	PLLDIV<8:0	>: PLL Feedba	ck Divisor bits	(also denoted	as 'M', PLL mu	ltiplier)	
	111111111	= 513					
	•						
	•						
	•						
	000110000:	= 50 (default)					
	•						
	•						
	•						
	00000010:	= 4					
	000000001	= 3 = 2					
	000000000000	-					

REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER

12.0 TIMER1

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated in Asynchronous Counter mode from an external clock source
- The external clock input (T1CK) can optionally be synchronized to the internal device clock and the clock synchronization is performed after the prescaler
- A block diagram of Timer1 is shown in Figure 12-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- · Gated Timer mode
- Synchronous Counter mode
- · Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit setting for different operating modes are given in the Table 12-1.

Mode	TCS	TGATE	TSYNC
Timer	0	0	x
Gated Timer	0	1	х
Synchronous Counter	1	x	1
Asynchronous Counter	1	x	0

TABLE 12-1: TIMER MODE SETTINGS

FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM





FIGURE 13-3: TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)

3: Timery is a Type C timer (y = 3 and 5).

Timerx/y Resources 13.1

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/
	wwwproducts/Devices.aspx?d
	DocName=en555464

KEY RESOURCES 13.1.1

- "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- · Software Libraries
- · Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

16.2 PWM Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

16.2.1 KEY RESOURCES

- "High-Speed PWM" (DS70645) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER (CONTINUED)

- bit 1 **RBIF:** RX Buffer Interrupt Flag bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 0 **TBIF:** TX Buffer Interrupt Flag bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 21-17: CxRXFnEID: ECANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x R/W-x		R/W-x
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
bit 7							bit 0

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 15-0 EID<15:0>: Extended Identifier bits

1 = Message address bit, EIDx, must be '1' to match filter

0 = Message address bit, EIDx, must be '0' to match filter

REGISTER 21-18: CxFMSKSEL1: ECANx FILTER 7-0 MASK SELECTION REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
F7MSK<1:0>		F6MSK<1:0>		F5MS	K<1:0>	F4MS	K<1:0>	
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
F3M	SK<1:0>	F2MSI	K<1:0>	F1MS	K<1:0>	F0MS	K<1:0>	
bit 7							bit 0	
Legend:								
R = Readabl	le bit	W = Writable	bit	U = Unimplen	nented bit, rea	d as '0'		
-n = Value at	t POR	'1' = Bit is set	:	'0' = Bit is clea	ared	x = Bit is unkr	x = Bit is unknown	
bit 15-14	F7MSK<1:0: 11 = Reserve 10 = Accepta 01 = Accepta 00 = Accepta	>: Mask Source ed ance Mask 2 re ance Mask 1 re ance Mask 0 re	for Filter 7 bi gisters contair gisters contair gisters contair	ts n mask n mask n mask				
bit 13-12	F6MSK<1:0	>: Mask Source	for Filter 6 bi	ts (same values	as bits<15:14	! >)		
bit 11-10	F5MSK<1:0	>: Mask Source	for Filter 5 bi	ts (same values	as bits<15:14	! >)		
bit 9-8	F4MSK<1:0	>: Mask Source	for Filter 4 bi	ts (same values	as bits<15:14	! >)		
bit 7-6	F3MSK<1:0:	>: Mask Source	for Filter 3 bi	ts (same values	s as bits<15:14	l>)		
bit 5-4	F2MSK<1:0	>: Mask Source	for Filter 2 bi	ts (same values	s as bits<15:14	! >)		
bit 3-2	F1MSK<1:0	>: Mask Source	for Filter 1 bi	ts (same values	s as bits<15:14	ł>)		
bit 1-0	F0MSK<1:0:	Hask Source	for Filter 0 bi	ts (same values	s as bits<15:14	! >)		

23.2 ADC Helpful Tips

- 1. The SMPIx control bits in the AD1CON2 register:
 - a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
 - b) When the CSCNA bit in the AD1CON2 registers is set to '1', this determines when the ADC analog scan channel list, defined in the AD1CSSL/AD1CSSH registers, starts over from the beginning.
 - c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
 - d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA.
- 2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMPIx bits and the condition described in 1c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
- 3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer (i.e., ADC1BUF0) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA Controller, before the next ADC conversion is complete to avoid overwriting the previous value.
- 4. The DONE bit (AD1CON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (AD1CON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.

5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for ANO, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUXA selections use ANO-AN2. Carefully study the ADC block diagram to determine the configuration that will best suit your application. Configuration examples are available in the "Analog-to-Digital Converter (ADC)" (DS70621) section in the "dsPIC33/ PIC24 Family Reference Manual".

23.3 ADC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
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23.3.1 KEY RESOURCES

- "Analog-to-Digital Converter (ADC)" (DS70621) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER (CONTINUED)

- PTGITM<1:0>: PTG Input Trigger Command Operating Mode bits⁽¹⁾
 - 11 = Single level detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
 - 10 = Single level detect with Step delay executed on exit of command
 - 01 = Continuous edge detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
 - 00 = Continuous edge detect with Step delay executed on exit of command
- Note 1: These bits apply to the PTGWHI and PTGWLO commands only.

bit 1-0

- **2:** This bit is only used with the PTGCTRL step command software trigger option.
- **3:** Use of the PTG Single-Step mode is reserved for debugging tools only.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
	_				—			
bit 15							bit 8	
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	
bit 7							bit 0	
Logondi								
R = Reada	able hit	W = Writable	hit	= Inimpler	mented hit read	ae 'O'		
-n = Value	at POR	(1) = Rit is set	bit	'0' = Bit is cle	ared	x = Rit is unkr	nown	
II Value		1 Bit lo oot					lowin	
bit 15-7	Unimplemen	nted: Read as '	0'					
bit 6-4	CFSEL<2:0>	Comparator I	-ilter Input Clo	ck Select bits				
	111 = T5CLK	(1) (1)						
	110 = T4CLK	< ⁽²⁾						
	101 = T3CLK	<(1) <(2)						
	100 = 12CLP	ved						
	010 = SYNC	01 ⁽³⁾						
	001 = Fosc ⁽⁴	4)						
	000 = FP ⁽⁴⁾							
bit 3	CFLTREN: C	Comparator Filte	er Enable bit					
	1 = Digital filt	er is enabled						
hit 2-0		Comparator F	ilter Clock Div	ide Select hits				
511 2-0	111 = Clock	Divide 1.128						
	110 = Clock	Divide 1:64						
	101 = Clock	Divide 1:32						
	100 = Clock	100 = Clock Divide 1:16						
	011 = Clock	Divide 1:8						
	001 = Clock	Divide 1:2						
	000 = Clock	Divide 1:1						
Note 1:	See the Type C Ti	mer Block Diac	ram (Figure 1	3-2).				
2:	See the Type B Tir	mer Block Diag	ram (Figure 1	ý 3-1).				

REGISTER 25-6: CMxFLTR: COMPARATOR x FILTER CONTROL REGISTER

- 3: See the High-Speed PWMx Module Register Interconnection Diagram (Figure 16-2).
 - 4: See the Oscillator System Diagram (Figure 9-1).

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions		
SY00	Τρυ	Power-up Period	—	400	600	μS			
SY10	Tost	Oscillator Start-up Time	_	1024 Tosc			Tosc = OSC1 period		
SY12	Twdt	Watchdog Timer Time-out Period	0.81	0.98	1.22	ms	WDTPRE = 0, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21 (see Table 30-20) at +85°C		
			3.26	3.91	4.88	ms	WDTPRE = 1, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21 (see Table 30-20) at +85°C		
SY13	Tioz	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	0.68	0.72	1.2	μS			
SY20	TMCLR	MCLR Pulse Width (low)	2	—	_	μS			
SY30	TBOR	BOR Pulse Width (low)	1	_	_	μS			
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	500	900	μS	-40°C to +85°C		
SY36	TVREG	Voltage Regulator Standby-to-Active mode Transition Time	—	_	30	μS			
SY37	Toscdfrc	FRC Oscillator Start-up Delay	46	48	54	μS			
SY38	TOSCDLPRC	LPRC Oscillator Start-up Delay	—	—	70	μS			

TABLE 30-22:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMERTIMING REQUIREMENTS

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

FIGURE 30-17: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS



TABLE 30-36:SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
SP10	FscP	Maximum SCK2 Frequency	—	—	9	MHz	-40°C to +125°C (Note 3)
SP20	TscF	SCK2 Output Fall Time	_	_		ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK2 Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_		ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30			ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30			ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- **3:** The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.
- 4: Assumes 50 pF load on all SPI2 pins.

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