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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128gp202-i-sp

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Pin Diagrams (Continued)



Pin Diagrams (Continued)



REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5	IPL<2:0>: CPU Interrupt Priority Level Status bits ^(2,3) 111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled 110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12) 011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10) 001 = CPU Interrupt Priority Level is 1 (9) 000 = CPU Interrupt Priority Level is 0 (8)
bit 4	RA: REPEAT Loop Active bit 1 = REPEAT loop in progress 0 = REPEAT loop not in progress
bit 3	N: MCU ALU Negative bit 1 = Result was negative 0 = Result was non-negative (zero or positive)
bit 2	 OV: MCU ALU Overflow bit This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state. 1 = Overflow occurred for signed arithmetic (in this arithmetic operation) 0 = No overflow occurred
bit 1	 Z: MCU ALU Zero bit 1 = An operation that affects the Z bit has set it at some time in the past 0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)
bit 0	C: MCU ALU Carry/Borrow bit 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred
Note 1: 2:	This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only. The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority

- Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
 3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- 4: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.





TABLE 4-52: PORTG REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	0E60			—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6				—	—		03C0
PORTG	0E62	_	_	_	_	_	_	RG9	RG8	RG7	RG6	_	_	_	_	_	_	xxxx
LATG	0E64	_	_	_	_	_	_	LATG9	LATG8	LATG7	LATG6	_	_	_	_	_	_	xxxx
ODCG	0E66			—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6				—	—		0000
CNENG	0E68	_	_	_	_	_	_	CNIEG9	CNIEG8	CNIEG7	CNIEG6	_	_	_	_	_	_	0000
CNPUG	0E6A	_	_	_	_	_	_	CNPUG9	CNPUG8	CNPUG7	CNPUG6	_	_	_	_	_	_	0000
CNPDG	0E6C	_	_	_	_	_	_	CNPDG9	CNPDG8	CNPDG7	CNPDG6	_	_		—	—	_	0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-53: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00		—	—			TRISA10	TRISA9	TRISA8	TRISA7			TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	079F
PORTA	0E02		—	_			RA10	RA9	RA8	RA7			RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04		—	—	-	-	LATA10	LATA9	LATA8	LATA7	_	-	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	_	_	_	_	_	ODCA10	ODCA9	ODCA8	ODCA7	_	_	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08		—	—			CNIEA10	CNIEA9	CNIEA8	CNIEA7			CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	_	_	_	_	_	CNPUA10	CNPUA9	CNPUA8	CNPUA7	_	_	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	_	_	_	_	_	CNPDA10	CNPDA9	CNPDA8	CNPDA7	_	_	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	_	_	_	_	_	_	_	_	_	_	_	ANSA4	_	_	ANSA1	ANSA0	0013

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-54: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	-	—	—	—	—	—	—	ANSB8	-	—	-	_	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-55: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	—	—	—	—	—	-	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	03FF
PORTC	0E22	—	_	—	—	—		RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	0E24	—	—	—	—	—		LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
ODCC	0E26	_	_	_	_	_	_	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000
CNENC	0E28	—	—	—	—	—	-	CNIEC9	CNIEC8	CNIEC7	CNIEC6	CNIEC5	CNIEC4	CNIEC3	CNIEC2	CNIEC1	CNIEC0	0000
CNPUC	0E2A	_	_	_	_	_	_	CNPUC9	CNPUC8	CNPUC7	CNPUC6	CNPUC5	CNPUC4	CNPUC3	CNPUC2	CNPUC1	CNPUC0	0000
CNPDC	0E2C	_	_	_	_	_	_	CNPDC9	CNPDC8	CNPDC7	CNPDC6	CNPDC5	CNPDC4	CNPDC3	CNPDC2	CNPDC1	CNPDC0	0000
ANSELC	0E2E	_	_	_	_	_	_	_		_		_	_	_	ANSC2	ANSC1	ANSC0	0007

Legend: x = unknown value on Reset, --- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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8.1 DMA Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

8.1.1 KEY RESOURCES

- Section 22. "Direct Memory Access (DMA)" (DS70348) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- · Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

8.2 DMAC Registers

Each DMAC Channel x (where x = 0 through 3) contains the following registers:

- 16-Bit DMA Channel Control register (DMAxCON)
- 16-Bit DMA Channel IRQ Select register (DMAxREQ)
- 32-Bit DMA RAM Primary Start Address register (DMAxSTA)
- 32-Bit DMA RAM Secondary Start Address register (DMAxSTB)
- 16-Bit DMA Peripheral Address register (DMAxPAD)
- 14-Bit DMA Transfer Count register (DMAxCNT)

Additional status registers (DMAPWC, DMARQC, DMAPPS, DMALCA and DSADR) are common to all DMAC channels. These status registers provide information on write and request collisions, as well as on last address and channel access information.

The interrupt flags (DMAxIF) are located in an IFSx register in the interrupt controller. The corresponding interrupt enable control bits (DMAxIE) are located in an IECx register in the interrupt controller, and the corresponding interrupt priority control bits (DMAxIP) are located in an IPCx register in the interrupt controller.

12.2 Timer1 Control Register

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	
TON ⁽¹⁾	—	TSIDL	—	_	—	—	—	
bit 15							bit 8	
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	
	TGATE	TCKPS1	TCKPS0	_	TSYNC ⁽¹⁾	TCS ⁽¹⁾	—	
bit 7							bit 0	
Legend:								
R = Readab	ole bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'		
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own	
		(1)						
bit 15	TON: Timer1	On bit ⁽¹⁾						
	1 = Starts 16-	bit Limer1 bit Timer1						
bit 1/	Unimplement	ted: Pead as '	ı'					
bit 13		1 Stop in Idle N	/ode hit					
DIC 15	1 = Discontinu	i stop in lae k	eration when a	device enters l	dle mode			
	0 = Continues	module opera	tion in Idle mo	ode				
bit 12-7	Unimplement	ted: Read as ')'					
bit 6	TGATE: Time	r1 Gated Time	Accumulation	Enable bit				
	When TCS =	<u>1:</u> prod						
	When TCS =	0. 0.						
	1 = Gated tim	<u>e</u> accumulatior	n is enabled					
	0 = Gated tim	e accumulatior	n is disabled					
bit 5-4	TCKPS<1:0>	: Timer1 Input	Clock Prescal	e Select bits				
	11 = 1:256							
	10 = 1:64 01 = 1:8							
	01 = 1.0 00 = 1.1							
bit 3	Unimplement	ted: Read as ')'					
bit 2	TSYNC: Time	er1 External Clo	ock Input Sync	chronization Se	elect bit ⁽¹⁾			
	When TCS =	1:						
	1 = Synchroni	izes external cl	ock input					
	0 = Does not	synchronize ex	ternal clock in	nput				
	This bit is jand	<u>ored</u> .						
bit 1	TCS: Timer1 (Clock Source S	Select bit ⁽¹⁾					
	1 = External c	lock is from pir	n, T1CK (on th	ne rising edge)				
	0 = Internal cl	ock (FP)		5 5-7				
bit 0	Unimplement	ted: Read as ')'					
Note 1: \	When Timer1 is enabled in External Synchronous Counter mode (TCS = 1, TSYNC = 1, TON = 1), any attempts by user software to write to the TMR1 register are ignored.							

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

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16.3 PWMx Control Registers

REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU ⁽¹⁾	SYNCPOL ⁽¹⁾	SYNCOEN ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN ⁽¹⁾	SYNCSRC2 ⁽¹⁾	SYNCSRC1 ⁽¹⁾	SYNCSRC0 ⁽¹⁾	SEVTPS3(1)	SEVTPS2 ⁽¹⁾	SEVTPS1 ⁽¹⁾	SEVTPS0 ⁽¹⁾
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	PTEN: PWMx Module Enable bit
	 1 = PWMx module is enabled 0 = PWMx module is disabled
bit 14	Unimplemented: Read as '0'
bit 13	PTSIDL: PWMx Time Base Stop in Idle Mode bit
	 1 = PWMx time base halts in CPU Idle mode 0 = PWMx time base runs in CPU Idle mode
bit 12	SESTAT: Special Event Interrupt Status bit
	 1 = Special event interrupt is pending 0 = Special event interrupt is not pending
bit 11	SEIEN: Special Event Interrupt Enable bit
	1 = Special event interrupt is enabled
	0 = Special event interrupt is disabled
bit 10	EIPU: Enable Immediate Period Updates bit ⁽¹⁾
	 1 = Active Period register is updated immediately 0 = Active Period register updates occur on PWMx cycle boundaries
bit 9	SYNCPOL: Synchronize Input and Output Polarity bit ⁽¹⁾
	1 = SYNCI1/SYNCO1 polarity is inverted (active-low)
	0 = SYNCI1/SYNCO1 is active-high
bit 8	SYNCOEN: Primary Time Base Sync Enable bit ⁽¹⁾
	1 = SYNCO1 output is enabled
L:1 7	0 = SYNCOT output is disabled
DIT /	SYNCEN: External Time Base Synchronization Enable bit
	1 = External synchronization of primary time base is enabled
Note 1:	These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user
	application must program the period register with a value that is slightly larger than the expected period of

the external synchronization input signal.

2: See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

·									
R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
PENH	PENL	POLH	POLL	PMOD1 ⁽¹⁾	PMOD0 ⁽¹⁾	OVRENH	OVRENL		
bit 15 bit 8									
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC		
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'					
-n = Value at F	POR	'1' = Bit is set '0' = Bit is cleared			eared	x = Bit is unknown			
bit 15	PENH: PWM	(H Output Pin (Ownership bit						
	1 = PWMx mc	dule controls I	PWMxH pin WMx⊟ pin						
hit 11									
DIL 14	1 = DM/Mx mc	adula controla l							
	1 = PWWX IIIC 0 = GPIO model	dule controls P	WMxL pin						
hit 13		H Output Pin I	Polarity bit						
	1 = PWMxH r	in is active-low	/						
	0 = PWMxH p	oin is active-hig	h						
bit 12	POLL: PWMx	L Output Pin F	olarity bit						
	1 = PWMxL pin is active-low								
	0 = PWMxL p	in is active-hig	h						
bit 11-10	PMOD<1:0>:	PWMx # I/O P	in Mode bits ⁽¹)					
	11 = Reserve	d; do not use							
	10 = PWMx I/	O pin pair is in	the Push-Pul	I Output mode					
	01 = PWWx I/ 00 = PWMx I/	O pin pair is in O pin pair is in	the Complem	nt Output mod entary Output	mode				
hit 9	OVPENH: Override Enable for PW/MyH Pin bit								
	1 = OVRDAT<1> controls output on PWMyH nin								
	0 = PWMx ge	nerator control	s PWMxH pin						
bit 8	OVRENL: Ov	erride Enable f	or PWMxL Pi	n bit					
	1 = OVRDAT	<0> controls ou	Itput on PWM	xL pin					
	0 = PWMx ge	nerator control	s PWMxL pin						
bit 7-6	OVRDAT<1:0	>: Data for PW	/MxH, PWMxl	L Pins if Overr	ide is Enabled b	its			
	If OVERENH	= 1, PWMxH is	s driven to the	state specifie	d by OVRDAT<	1>.			
	If OVERENL :	= 1, PWMxL is	driven to the	state specified	l by OVRDAT<0	>.			
bit 5-4	FLTDAT<1:0>	Data for PW	MxH and PWI	MxL Pins if FL	TMOD is Enable	ed bits			
	If Fault is activ	ve, PWMxH is	driven to the s	state specified	by FLTDAT<1>				
hit 2 0		VE, FVVIVIXL IS (UY FLIDAISUS.	hita			
UIL 3-2	LUAI <1:0>			IXL PILIS IT ULN					
If current-limit is active. PWMxL is driven to the state specified by CLDAT<12.									
Note 1: The	ese bits should i	not be changed	d after the PW	Mx module is	enabled (PTEN	= 1).			

REGISTER 16-13: IOCONx: PWMx I/O CONTROL REGISTER⁽²⁾

2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Quadrature Encoder Interface (QEI)" (DS70601) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI module include:

- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 16-Bit Velocity Counter
- 32-Bit Position Initialization/Capture/Compare High register
- 32-Bit Position Compare Low register
- x4 Quadrature Count mode
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Internal Timer mode

Figure 17-1 illustrates the QEI block diagram.

REGISTER 18-1: SPIx STAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 1 SPITBF: SPIx Transmit Buffer Full Status bit
 - 1 = Transmit not yet started, SPIxTXB is full
 - 0 = Transmit started, SPIxTXB is empty

Standard Buffer mode:

Automatically set in hardware when core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer mode:

Automatically set in hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 SPIRBF: SPIx Receive Buffer Full Status bit

1 = Receive is complete, SPIxRXB is full

0 = Receive is incomplete, SPIxRXB is empty

Standard Buffer mode:

Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

Enhanced Buffer mode:

Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

NOTES:

REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2 (CONTINUED)

bit 1 BUFM: Buffer Fill Mode Select bit			
	 1 = Starts the buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on next interrupt 0 = Always starts filling the buffer from the start address. 		
bit 0	ALTS: Alternate Input Sample Mode Select bit		

1 = Uses channel input selects for Sample MUXA on first sample and Sample MUXB on next sample 0 = Always uses channel input selects for Sample MUXA

25.1.2 OP AMP CONFIGURATION B

Figure 25-7 shows a typical inverting amplifier circuit with the output of the op amp (OAxOUT) externally routed to a separate analog input pin (ANy) on the device. This op amp configuration is slightly different in terms of the op amp output and the ADC input connection, therefore, RINT1 is not included in the transfer function. However, this configuration requires the designer to externally route the op amp output (OAxOUT) to another analog input pin (ANy). See Table 30-53 in **Section 30.0 "Electrical Characteristics"** for the typical value of RINT1. Table 30-60 and Table 30-61 in **Section 30.0 "Electrical Characteristics"** describe the minimum sample time (TSAMP) requirements for the ADC module in this configuration.

Figure 25-7 also defines the equation to be used to calculate the expected voltage at point VOAxOUT. This is the typical inverting amplifier equation.

25.2 Op Amp/Comparator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser:
	http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

25.2.1 KEY RESOURCES

- "Op Amp/Comparator" (DS70357) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- · Application Notes
- Software Libraries
- · Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools



FIGURE 25-7: OP AMP CONFIGURATION B

REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER (CONTINUED)

- bit 5 Unimplemented: Read as '0'
- bit 4 **CREF:** Comparator Reference Select bit (VIN+ input)⁽¹⁾
 - 1 = VIN+ input connects to internal CVREFIN voltage
 - 0 = VIN+ input connects to C4IN1+ pin
- bit 3-2 Unimplemented: Read as '0'
- bit 1-0 CCH<1:0>: Comparator Channel Select bits⁽¹⁾
 - 11 = VIN- input of comparator connects to OA3/AN6
 - 10 = VIN- input of comparator connects to OA2/AN0
 - 01 = VIN- input of comparator connects to OA1/AN3
 - 00 = VIN- input of comparator connects to C4IN1-
- Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.

TABLE 30-39:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency			15	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—		_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—		_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—		—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—		_	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30		_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120		_	ns	
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	_	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	_	_	ns	(Note 4)

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

FIGURE 30-24: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS

TABLE 30-43:SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	_		10	MHz	(Note 3)
SP20	TscF	SCK1 Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK1 Output Rise Time	—	—	_	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	_	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—		ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	_	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30			ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- **3:** The minimum clock period for SCK1 is 100 ns. The clock generated in Master mode must not violate this specification.
- **4:** Assumes 50 pF load on all SPI1 pins.

33.1 Package Marking Information (Continued)

Section Name	Update Description
Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"	Updated the High-Speed PWM Module Register Interconnection Diagram (see Figure 16-2). Added the TRGCONx and TRIGx registers (see Register 16-12 and Register 16-14, respectively).
Section 21.0 "Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)"	Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1).
Section 22.0 "Charge Time Measurement Unit (CTMU)"	Updated the IRNG<1:0> bit value definitions and added Note 2 in the CTMU Current Control Register (see Register 22-3).
Section 25.0 "Op amp/ Comparator Module"	Updated the Op amp/Comparator I/O Operating Modes Diagram (see Figure 25-1). Updated the User-programmable Blanking Function Block Diagram (see Figure 25-3). Updated the Digital Filter Interconnect Block Diagram (see Figure 25-4). Added Section 25.1 "Op amp Application Considerations" . Added Note 2 to the Comparator Control Register (see Register 25-2). Updated the bit definitions in the Comparator Mask Gating Control Register (see Register 25-5).
Section 27.0 "Special Features"	Updated the FICD Configuration Register, updated Note 1, and added Note 3 in the Configuration Byte Register Map (see Table 27-1). Added Section 27.2 "User ID Words" .
Section 30.0 "Electrical Characteristics"	 Updated the following Absolute Maximum Ratings: Maximum current out of Vss pin Maximum current into VDD pin Added Note 1 to the Operating MIPS vs. Voltage (see Table 30-1).
	Updated all Idle Current (IIDLE) Typical and Maximum DC Characteristics values (see Table 30-7).
	Updated all Doze Current (IDOZE) Typical and Maximum DC Characteristics values (see Table 30-9).
	Added Note 2, removed Parameter CM24, updated the Typical values Parameters CM10, CM20, CM21, CM32, CM41, CM44, and CM45, and updated the Minimum values for CM40 and CM41, and the Maximum value for CM40 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14).
	Updated Note 2 and the Typical value for Parameter VR310 in the Op amp/ Comparator Reference Voltage Settling Time Specifications (see Table 30-15).
	Added Note 1, removed Parameter VRD312, and added Parameter VRD314 to the Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16).
	Updated the Minimum, Typical, and Maximum values for Internal LPRC Accuracy (see Table 30-22).
	Updated the Minimum, Typical, and Maximum values for Parameter SY37 in the Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer Timing Requirements (see Table 30-24).
	The Maximum Data Rate values were updated for the SPI2 Maximum Data/Clock Rate Summary (see Table 30-35)

TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)