What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
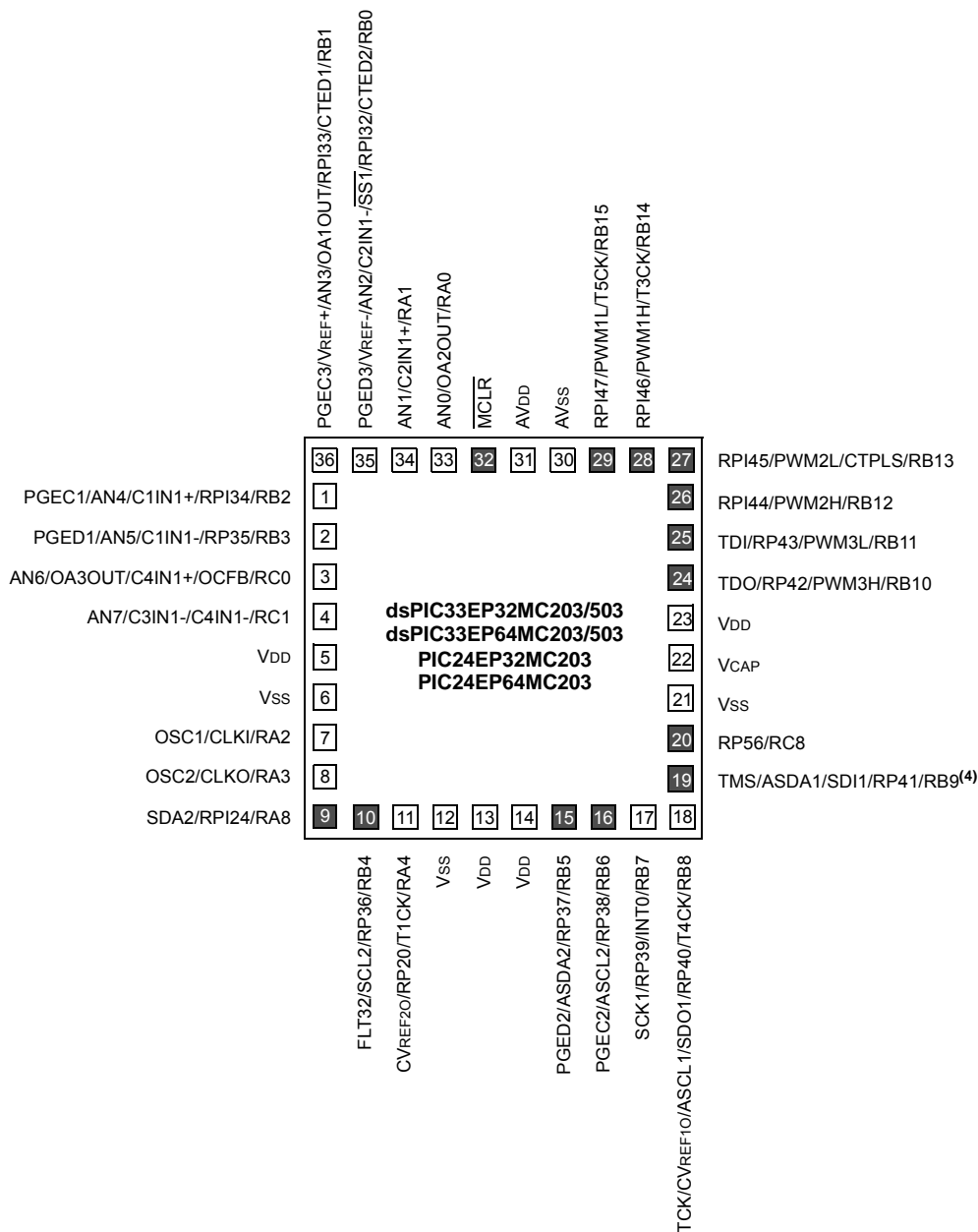
Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128gp202-i-ss

Pin Diagrams (Continued)

36-Pin VTLA[1,2,3]

■ = Pins are up to 5V tolerant

Top pins (36–27):
- 36: PGEC3/VREF+/AN3/OA1OUT/RPI33/CTED1/RB1
- 35: PGED3/VREF-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0
- 34: AN1/C2IN1+/RA1
- 33: AN0/OA2OUT/RA0
- 32: MCLR
- 31: AVDD
- 30: AVSS
- 29: RPI47/PWM1L/T5CK/RB15
- 28: RPI46/PWM1H/T3CK/RB14

Left pins:
- PGEC1/AN4/C1IN1+/RPI34/RB2 — 1
- PGED1/AN5/C1IN1-/RP35/RB3 — 2
- AN6/OA3OUT/C4IN1+/OCFB/RC0 — 3
- AN7/C3IN1-/C4IN1-/RC1 — 4
- VDD — 5
- VSS — 6
- OSC1/CLKI/RA2 — 7
- OSC2/CLKO/RA3 — 8
- SDA2/RPI24/RA8 — 9

Device:
**dsPIC33EP32MC203/503
dsPIC33EP64MC203/503
PIC24EP32MC203
PIC24EP64MC203**

Right pins:
- 27 — RPI45/PWM2L/CTPLS/RB13
- 26 — RPI44/PWM2H/RB12
- 25 — TDI/RP43/PWM3L/RB11
- 24 — TDO/RP42/PWM3H/RB10
- 23 — VDD
- 22 — VCAP
- 21 — VSS
- 20 — RP56/RC8
- 19 — TMS/ASDA1/SDI1/RP41/RB9[4]

Bottom pins (10–18):
- 10: FLT32/SCL2/RP36/RB4
- 11: CVREF2O/RP20/T1CK/RA4
- 12: VSS
- 13: VDD
- 14: VDD
- 15: PGED2/ASDA2/RP37/RB5
- 16: PGEC2/ASCL2/RP38/RB6
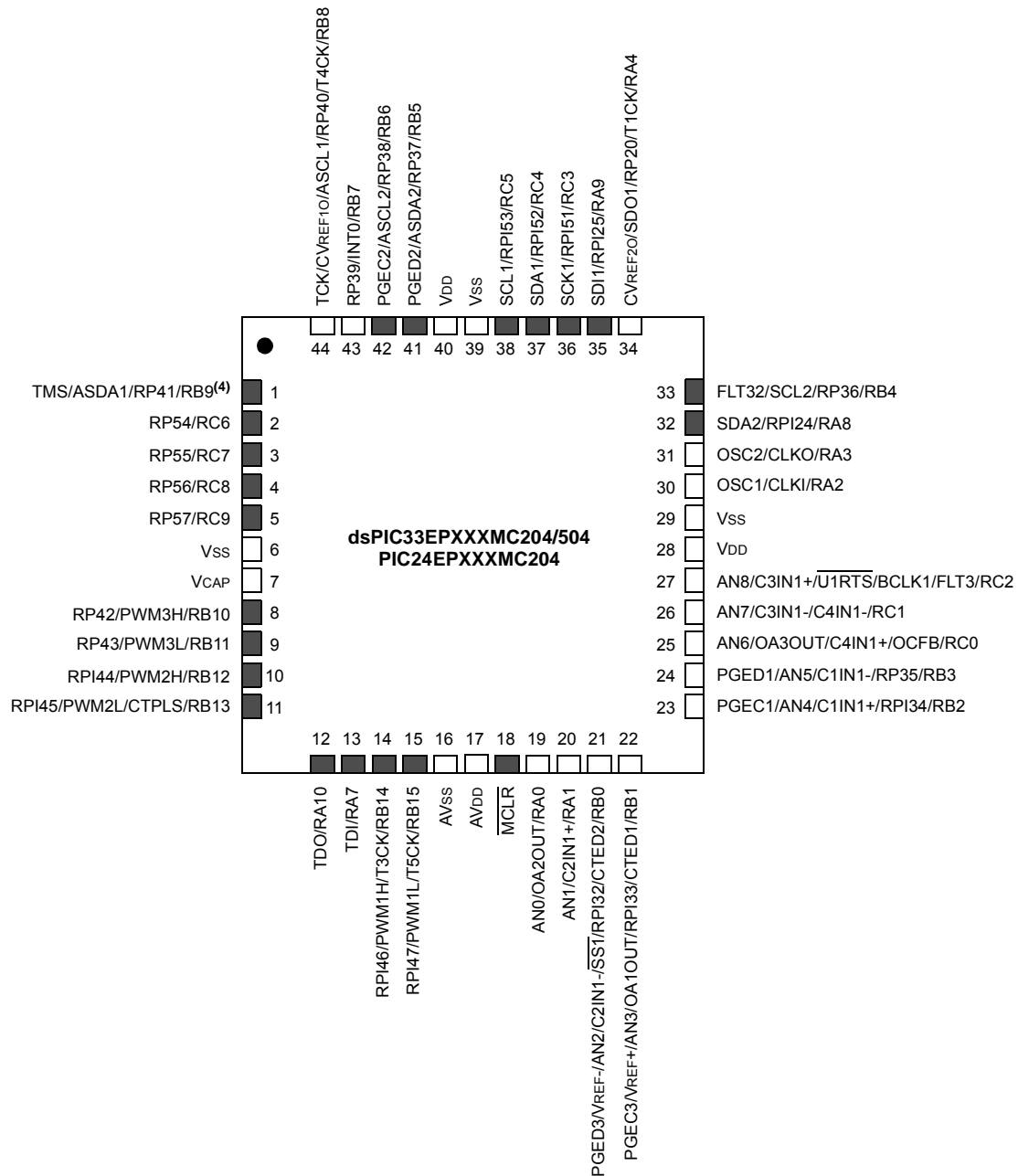- 17: SCK1/RP39/INT0/RB7
- 18: TCK/CVREF1O/ASCL1/SDO1/RP40/T4CK/RB8

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

Pin Diagrams (Continued)

44-Pin QFN[1,2,3]

■ = Pins are up to 5V tolerant

Top pins (44–34):
- 44: TCK/CV$_{REF1O}$/ASCL1/RP40/T4CK/RB8
- 43: RP39/INT0/RB7
- 42: PGEC2/ASCL2/RP38/RB6
- 41: PGED2/ASDA2/RP37/RB5
- 40: V$_{DD}$
- 39: V$_{SS}$
- 38: SCL1/RPI53/RC5
- 37: SDA1/RPI52/RC4
- 36: SCK1/RPI51/RC3
- 35: SDI1/RPI25/RA9
- 34: CV$_{REF2O}$/SDO1/RP20/T1CK/RA4

Device: **dsPIC33EPXXXMC204/504**
PIC24EPXXXMC204

Left pins (1–11):
- 1: TMS/ASDA1/RP41/RB9[4]
- 2: RP54/RC6
- 3: RP55/RC7
- 4: RP56/RC8
- 5: RP57/RC9
- 6: V$_{SS}$
- 7: V$_{CAP}$
- 8: RP42/PWM3H/RB10
- 9: RP43/PWM3L/RB11
- 10: RPI44/PWM2H/RB12
- 11: RPI45/PWM2L/CTPLS/RB13

Right pins (33–23):
- 33: FLT32/SCL2/RP36/RB4
- 32: SDA2/RPI24/RA8
- 31: OSC2/CLKO/RA3
- 30: OSC1/CLKI/RA2
- 29: V$_{SS}$
- 28: V$_{DD}$
- 27: AN8/C3IN1+/$\overline{U1RTS}$/BCLK1/FLT3/RC2
- 26: AN7/C3IN1-/C4IN1-/RC1
- 25: AN6/OA3OUT/C4IN1+/OCFB/RC0
- 24: PGED1/AN5/C1IN1-/RP35/RB3
- 23: PGEC1/AN4/C1IN1+/RPI34/RB2

Bottom pins (12–22):
- 12: TDO/RA10
- 13: TDI/RA7
- 14: RPI46/PWM1H/T3CK/RB14
- 15: RPI47/PWM1L/T5CK/RB15
- 16: AV$_{SS}$
- 17: AV$_{DD}$
- 18: $\overline{MCLR}$
- 19: AN0/OA2OUT/RA0
- 20: AN1/C2IN1+/RA1
- 21: PGED3/V$_{REF-}$/AN2/C2IN1-/$\overline{SS1}$/RPI32/CTED2/RB0
- 22: PGEC3/V$_{REF+}$/AN3/OA1OUT/RPI33/CTED1/RB1

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to V$_{SS}$ externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

3.5 Programmer's Model

The programmer's model for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X is shown in Figure 3-2. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X devices contain control registers for Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only), Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only) and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory mapped, as shown in Table 4-1.

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Register(s) Name	Description
W0 through W15	Working Register Array
ACCA, ACCB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
DSRPAG	Extended Data Space (EDS) Read Page Register
DSWPAG	Extended Data Space (EDS) Write Page Register
RCOUNT	REPEAT Loop Count Register
DCOUNT[1]	DO Loop Count Register
DOSTARTH[1,2], DOSTARTL[1,2]	DO Loop Start Address Register (High and Low)
DOENDH[1], DOENDL[1]	DO Loop End Address Register (High and Low)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

Note 1: This register is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

2: The DOSTARTH and DOSTARTL registers are read-only.

TABLE 4-31: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—	INT1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>							0000
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>							0000
RPINR7	06AE	—	IC2R<6:0>						—		IC1R<6:0>							0000
RPINR8	06B0	—	IC4R<6:0>						—		IC3R<6:0>							0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>							0000
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>							0000
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>							0000
RPINR22	06CC	—	SCK2INR<6:0>						—		SDI2R<6:0>							0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>							0000
RPINR26	06D4	—	—	—	—	—	—	—	—	—	C1RXR<6:0>							0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-32: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—	INT1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>							0000
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>							0000
RPINR7	06AE	—	IC2R<6:0>						—		IC1R<6:0>							0000
RPINR8	06B0	—	IC4R<6:0>						—		IC3R<6:0>							0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>							0000
RPINR12	06B8	—	FLT2R<6:0>						—		FLT1R<6:0>							0000
RPINR14	06BC	—	QEB1R<6:0>						—		QEA1R<6:0>							0000
RPINR15	06BE	—	HOME1R<6:0>						—		INDX1R<6:0>							0000
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>							0000
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>							0000
RPINR22	06CC	—	SCK2INR<6:0>						—		SDI2R<6:0>							0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>							0000
RPINR26	06D4	—	—	—	—	—	—	—	—	—	C1RXR<6:0>							0000
RPINR37	06EA	—	SYNCI1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR38	06EC	—	DTCMP1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR39	06EE	—	DTCMP3R<6:0>							—	DTCMP2R<6:0>							0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.5.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions, which apply to dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and the DSP accumulator class of instructions, which apply to the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

> **Note:** For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

> **Note:** Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.5.4 MAC INSTRUCTIONS (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X DEVICES ONLY)

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY.N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The Two-Source Operand Prefetch registers must be members of the set: {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

> **Note:** Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the MAC class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.5.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as a NOP, do not have any operands.

4.8 Interfacing Program and Data Memory Spaces

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture uses a 24-bit-wide Program Space (PS) and a 16-bit-wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the architecture of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices provides two methods by which Program Space can be accessed during operation:

• Using table instructions to access individual bytes or words anywhere in the Program Space
• Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

TABLE 4-65: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		<23>	**<22:16>**	**<15>**	**<14:1>**	**<0>**
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xx xxxx xxxx xxxx xxxx xxx0				
`TBLRD/TBLWT` (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx xxxx xxxx xxxx xxxx xxxx				
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		1xxx xxxx xxxx xxxx xxxx xxxx				

FIGURE 4-22: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION

Note 1: The Least Significant bit (LSb) of Program Space addresses is always fixed as '0' to maintain word alignment of data in the Program and Data Spaces.

2: Table operations are not required to be word-aligned. Table Read operations are permitted in the configuration memory space.
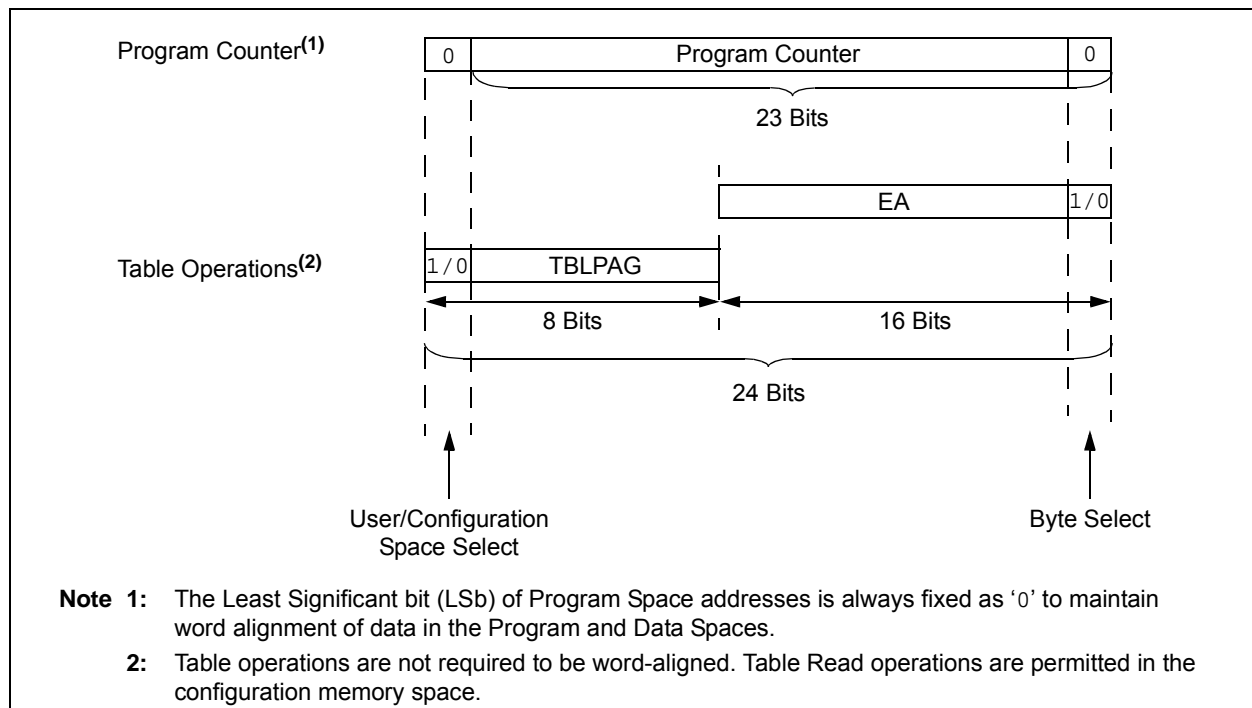
REGISTER 8-7: DMAxPAD: DMA CHANNEL x PERIPHERAL ADDRESS REGISTER[1]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PAD<15:8>				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PAD<7:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **PAD<15:0>:** Peripheral Address Register bits

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-8: DMAxCNT: DMA CHANNEL x TRANSFER COUNT REGISTER[1]

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			CNT<13:8>[2]			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			CNT<7:0>[2]				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14   **Unimplemented:** Read as '0'

bit 13-0   **CNT<13:0>:** DMA Transfer Count Register bits[2]

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

    2: The number of DMA transfers = CNT<13:0> + 1.

9.0 OSCILLATOR CONFIGURATION

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Oscillator"** (DS70580) in the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).
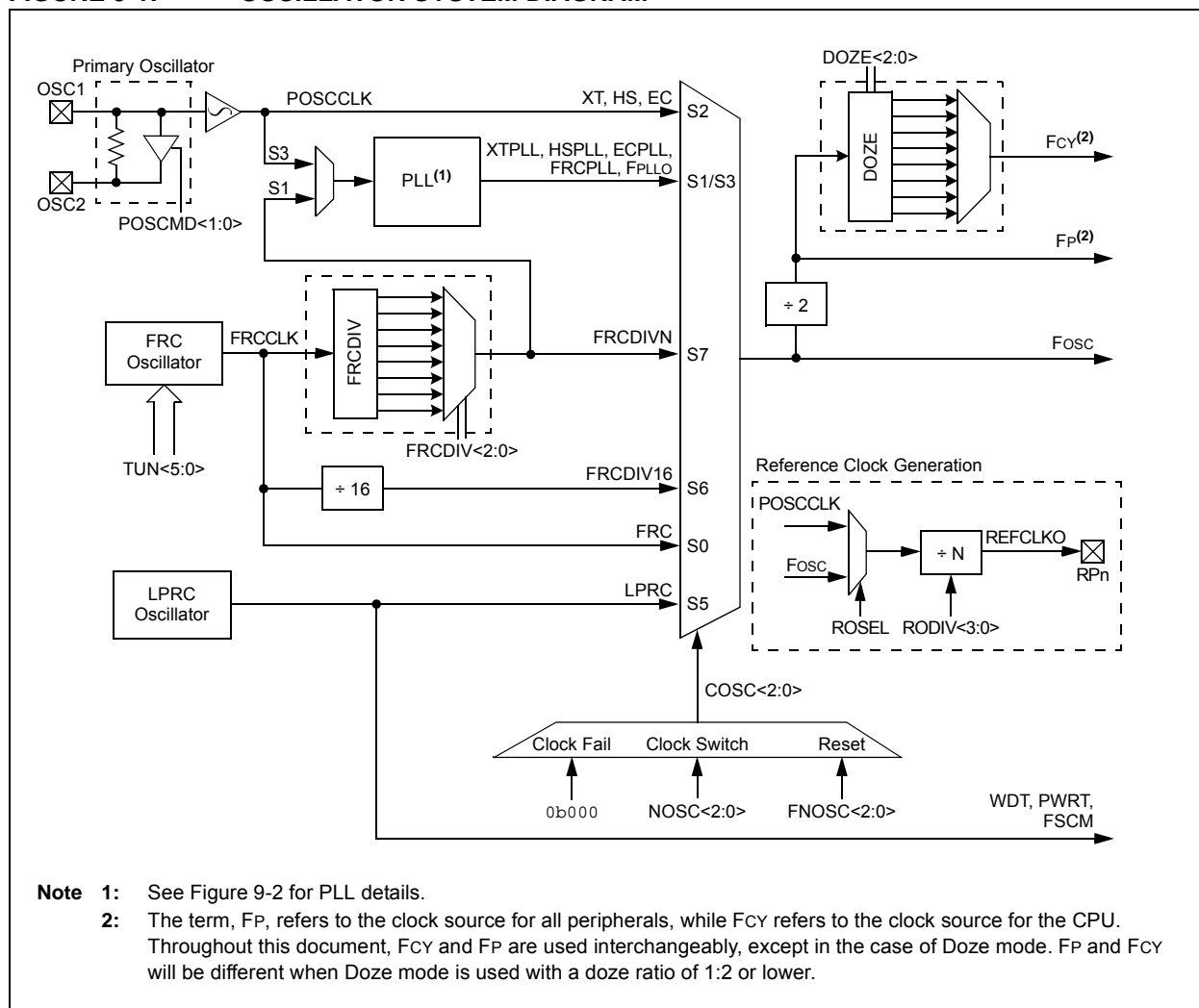
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X oscillator system provides:

- On-chip Phase-Locked Loop (PLL) to boost internal operating frequency on select internal and external oscillator sources
- On-the-fly clock switching between various clock sources
- Doze mode for system power savings
- Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Configuration bits for clock source selection

A simplified diagram of the oscillator system is shown in Figure 9-1.

FIGURE 9-1: OSCILLATOR SYSTEM DIAGRAM

Note 1: See Figure 9-2 for PLL details.
2: The term, FP, refers to the clock source for all peripherals, while FCY refers to the clock source for the CPU. Throughout this document, FCY and FP are used interchangeably, except in the case of Doze mode. FP and FCY will be different when Doze mode is used with a doze ratio of 1:2 or lower.

9.3 Oscillator Control Registers

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER[1]

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
—	COSC2	COSC1	COSC0	—	NOSC2[2]	NOSC1[2]	NOSC0[2]
bit 15							bit 8

R/W-0	R/W-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
CLKLOCK	IOLOCK	LOCK	—	CF[3]	—	—	OSWEN
bit 7							bit 0

Legend:		y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **Unimplemented:** Read as '0'

bit 14-12   **COSC<2:0>:** Current Oscillator Selection bits (read-only)

111 = Fast RC Oscillator (FRC) with Divide-by-n
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Reserved
011 = Primary Oscillator (XT, HS, EC) with PLL
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 11   **Unimplemented:** Read as '0'

bit 10-8   **NOSC<2:0>:** New Oscillator Selection bits[2]

111 = Fast RC Oscillator (FRC) with Divide-by-n
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Reserved
011 = Primary Oscillator (XT, HS, EC) with PLL
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 7   **CLKLOCK:** Clock Lock Enable bit

1 = If (FCKSM0 = 1), then clock and PLL configurations are locked; if (FCKSM0 = 0), then clock and PLL configurations may be modified
0 = Clock and PLL selections are not locked, configurations may be modified

bit 6   **IOLOCK:** I/O Lock Enable bit

1 = I/O lock is active
0 = I/O lock is not active

bit 5   **LOCK:** PLL Lock Status bit (read-only)

1 = Indicates that PLL is in lock or PLL start-up timer is satisfied
0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

Note 1: Writes to this register require an unlock sequence. Refer to **"Oscillator"** (DS70580) in the *"dsPIC33/ PIC24 Family Reference Manual"* (available from the Microchip web site) for details.

     2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

     3: This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.

REGISTER 9-5: **REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER**

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON	—	ROSSLP	ROSEL	RODIV3[1]	RODIV2[1]	RODIV1[1]	RODIV0[1]
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROON:** Reference Oscillator Output Enable bit

1 = Reference oscillator output is enabled on the REFCLK pin[2]
0 = Reference oscillator output is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSSLP:** Reference Oscillator Run in Sleep bit

1 = Reference oscillator output continues to run in Sleep
0 = Reference oscillator output is disabled in Sleep

bit 12 **ROSEL:** Reference Oscillator Source Select bit

1 = Oscillator crystal is used as the reference clock
0 = System clock is used as the reference clock

bit 11-8 **RODIV<3:0>:** Reference Oscillator Divider bits[1]

1111 = Reference clock divided by 32,768
1110 = Reference clock divided by 16,384
1101 = Reference clock divided by 8,192
1100 = Reference clock divided by 4,096
1011 = Reference clock divided by 2,048
1010 = Reference clock divided by 1,024
1001 = Reference clock divided by 512
1000 = Reference clock divided by 256
0111 = Reference clock divided by 128
0110 = Reference clock divided by 64
0101 = Reference clock divided by 32
0100 = Reference clock divided by 16
0011 = Reference clock divided by 8
0010 = Reference clock divided by 4
0001 = Reference clock divided by 2
0000 = Reference clock

bit 7-0 **Unimplemented:** Read as '0'

Note 1: The reference oscillator output must be disabled (ROON = 0) before writing to these bits.

2: This pin is remappable. See **Section 11.4 "Peripheral Pin Select (PPS)"** for more information.

REGISTER 11-15: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				SYNCI1R<6:0>			

bit 15   bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—

bit 7   bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **SYNCI1R<6:0>:** Assign PWM Synchronization Input 1 to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
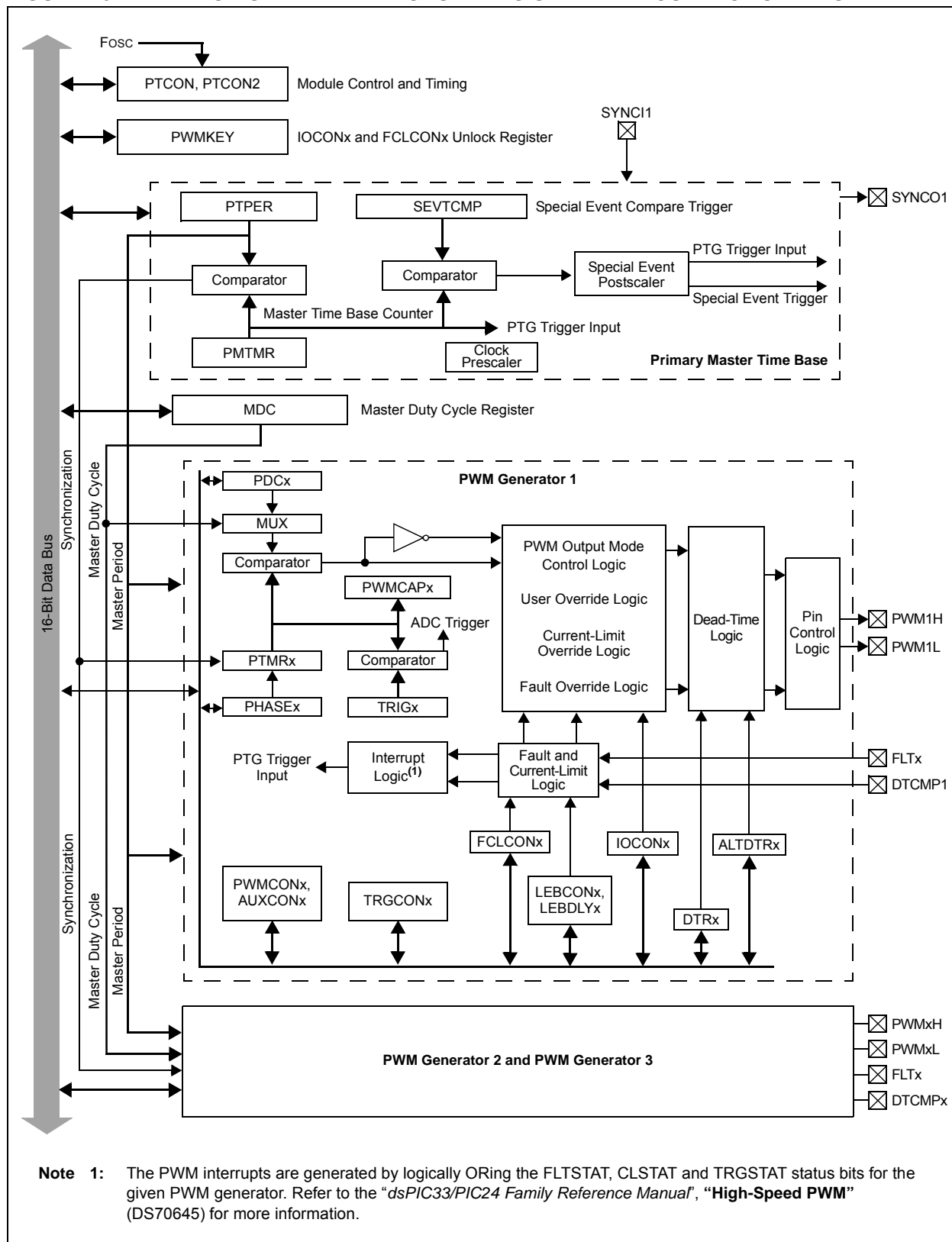
1111001 = Input tied to RPI121
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

FIGURE 16-2: **HIGH-SPEED PWMx MODULE REGISTER INTERCONNECTION DIAGRAM**

Note 1: The PWM interrupts are generated by logically ORing the FLTSTAT, CLSTAT and TRGSTAT status bits for the given PWM generator. Refer to the "*dsPIC33/PIC24 Family Reference Manual*", **"High-Speed PWM"** (DS70645) for more information.

REGISTER 17-2:   QEI1IOC: QEI1 I/O CONTROL REGISTER (CONTINUED)

bit 2   **INDEX:** Status of INDXx Input Pin After Polarity Control

               1 = Pin is at logic '1'
               0 = Pin is at logic '0'

bit 1   **QEB:** Status of QEBx Input Pin After Polarity Control And SWPAB Pin Swapping

               1 = Pin is at logic '1'
               0 = Pin is at logic '0'

bit 0   **QEA:** Status of QEAx Input Pin After Polarity Control And SWPAB Pin Swapping

               1 = Pin is at logic '1'
               0 = Pin is at logic '0'

REGISTER 24-12: PTGQPTR: PTG STEP QUEUE POINTER REGISTER[1]

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	PTGQPTR<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5   **Unimplemented:** Read as '0'

bit 4-0   **PTGQPTR<4:0>:** PTG Step Queue Pointer Register bits

This register points to the currently active Step command in the Step queue.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-13: PTGQUEx: PTG STEP QUEUE REGISTER x (x = 0-7)[1,3]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP(2x + 1)<7:0>[2]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP(2x)<7:0>[2]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8   **STEP(2x + 1)<7:0>:** PTG Step Queue Pointer Register bits[2]

A queue location for storage of the STEP(2x + 1) command byte.

bit 7-0   **STEP(2x)<7:0>:** PTG Step Queue Pointer Register bits[2]

A queue location for storage of the STEP(2x) command byte.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

    2: Refer to Table 24-1 for the Step command encoding.

    3: The Step registers maintain their values on any type of Reset.

REGISTER 26-3:   CRCXORH: CRC XOR POLYNOMIAL HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
X<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
X<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **X<31:16>:** XOR of Polynomial Term X^n Enable bits

REGISTER 26-4:   CRCXORL: CRC XOR POLYNOMIAL LOW REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
X<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
X<7:1>							—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-1   **X<15:1>:** XOR of Polynomial Term X^n Enable bits
bit 0   **Unimplemented:** Read as '0'

TABLE 30-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Parameter No.	Typ.	Max.	Units	Conditions		
Operating Current (IDD)[1]						
DC20d	9	15	mA	-40°C	3.3V	10 MIPS
DC20a	9	15	mA	+25°C		
DC20b	9	15	mA	+85°C		
DC20c	9	15	mA	+125°C		
DC22d	16	25	mA	-40°C	3.3V	20 MIPS
DC22a	16	25	mA	+25°C		
DC22b	16	25	mA	+85°C		
DC22c	16	25	mA	+125°C		
DC24d	27	40	mA	-40°C	3.3V	40 MIPS
DC24a	27	40	mA	+25°C		
DC24b	27	40	mA	+85°C		
DC24c	27	40	mA	+125°C		
DC25d	36	55	mA	-40°C	3.3V	60 MIPS
DC25a	36	55	mA	+25°C		
DC25b	36	55	mA	+85°C		
DC25c	36	55	mA	+125°C		
DC26d	41	60	mA	-40°C	3.3V	70 MIPS
DC26a	41	60	mA	+25°C		
DC26b	41	60	mA	+85°C		

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:
- Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- CPU is executing while(1){NOP();} statement
- JTAG is disabled

TABLE 30-8:   DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended	
Parameter No.	Typ.	Max.	Units	Conditions	
Power-Down Current (IPD)[1] – dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X and PIC24EP32GP/MC20X					
DC60d	30	100	μA	-40°C	
DC60a	35	100	μA	+25°C	3.3V
DC60b	150	200	μA	+85°C	
DC60c	250	500	μA	+125°C	
Power-Down Current (IPD)[1] – dsPIC33EP64GP50X, dsPIC33EP64MC20X/50X and PIC24EP64GP/MC20X					
DC60d	25	100	μA	-40°C	
DC60a	30	100	μA	+25°C	3.3V
DC60b	150	350	μA	+85°C	
DC60c	350	800	μA	+125°C	
Power-Down Current (IPD)[1] – dsPIC33EP128GP50X, dsPIC33EP128MC20X/50X and PIC24EP128GP/MC20X					
DC60d	30	100	μA	-40°C	
DC60a	35	100	μA	+25°C	3.3V
DC60b	150	350	μA	+85°C	
DC60c	550	1000	μA	+125°C	
Power-Down Current (IPD)[1] – dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X and PIC24EP256GP/MC20X					
DC60d	35	100	μA	-40°C	
DC60a	40	100	μA	+25°C	3.3V
DC60b	250	450	μA	+85°C	
DC60c	1000	1200	μA	+125°C	
Power-Down Current (IPD)[1] – dsPIC33EP512GP50X, dsPIC33EP512MC20X/50X and PIC24EP512GP/MC20X					
DC60d	40	100	μA	-40°C	
DC60a	45	100	μA	+25°C	3.3V
DC60b	350	800	μA	+85°C	
DC60c	1100	1500	μA	+125°C	

Note 1:   IPD (Sleep) current is measured as follows:
- CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all set)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to standby while the device is in Sleep mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

FIGURE 30-11: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS
(dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)
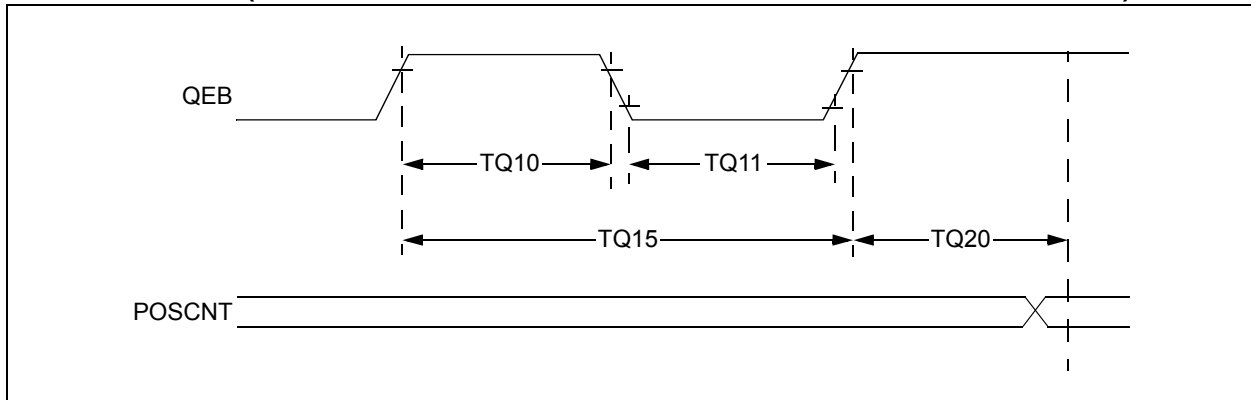
TABLE 30-30: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS
(dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic[1]		Min.	Typ.	Max.	Units	Conditions
TQ10	TtQH	TQCK High Time	Synchronous, with prescaler	Greater of 12.5 + 25 or (0.5 TCY/N) + 25	—	—	ns	Must also meet Parameter TQ15
TQ11	TtQL	TQCK Low Time	Synchronous, with prescaler	Greater of 12.5 + 25 or (0.5 TCY/N) + 25	—	—	ns	Must also meet Parameter TQ15
TQ15	TtQP	TQCP Input Period	Synchronous, with prescaler	Greater of 25 + 50 or (1 TCY/N) + 50	—	—	ns	
TQ20	TCKEXTMRL	Delay from External TQCK Clock Edge to Timer Increment		—	1	TCY	—	

Note 1: These parameters are characterized but not tested in manufacturing.

Revision E (April 2012)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

TABLE A-4: MAJOR SECTION UPDATES

Section Name	Update Description
"16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High-Speed PWM, Op amps, and Advanced Analog"	The following 512-Kbyte devices were added to the General Purpose Families table (see Table 1): • PIC24EP512GP202 • PIC24EP512GP204 • PIC24EP512GP206 • dsPIC33EP512GP502 • dsPIC33EP512GP504 • dsPIC33EP512GP506 The following 512-Kbyte devices were added to the Motor Control Families table (see Table 2): • PIC24EP512MC202 • PIC24EP512MC204 • PIC24EP512MC206 • dsPIC33EP512MC202 • dsPIC33EP512MC204 • dsPIC33EP512MC206 • dsPIC33EP512MC502 • dsPIC33EP512MC504 • dsPIC33EP512MC506 Certain Pin Diagrams were updated to include the new 512-Kbyte devices.
Section 4.0 "Memory Organization"	Added a Program Memory Map for the new 512-Kbyte devices (see Figure 4-4). Added a Data Memory Map for the new dsPIC 512-Kbyte devices (see Figure 4-11). Added a Data Memory Map for the new PIC24 512-Kbyte devices (see Figure 4-16).
Section 7.0 "Interrupt Controller"	Updated the VECNUM bits in the INTTREG register (see Register 7-7).
Section 11.0 "I/O Ports"	Added tip 6 to **Section 11.5 "I/O Helpful Tips"**.
Section 27.0 "Special Features"	The following modifications were made to the Configuration Byte Register Map (see Table 27-1): • Added the column Device Memory Size (Kbytes) • Removed Notes 1 through 4 • Added addresses for the new 512-Kbyte devices
Section 30.0 "Electrical Characteristics"	Updated the Minimum value for Parameter DC10 (see Table 30-4). Added Power-Down Current (Ipd) parameters for the new 512-Kbyte devices (see Table 30-8). Updated the Minimum value for Parameter CM34 (see Table 30-53). Updated the Minimum and Maximum values and the Conditions for paramteer SY12 (see Table 30-22).

TABLE A-5: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description

Section 30.0 "Electrical Characteristics"	• Throughout: qualifies all footnotes relating to the operation of analog modules below V_{DDMIN} (replaces "will have" with "may have")
	 • Throughout: changes all references of SPI timing parameter symbol "TscP" to "FscP"
	 • Table 30-1: changes V_{DD} range to 3.0V to 3.6V
	 • Table 30-4: removes Parameter DC12 (RAM Retention Voltage)
	 • Table 30-7: updates Maximum values at 10 and 20 MIPS
	 • Table 30-8: adds Maximum I_{PD} values, and removes all ΔI_{WDT} entries
	 • Adds new Table 30-9 (Watchdog Timer Delta Current) with consolidated values removed from Table 30-8. All subsequent tables are renumbered accordingly.
	 • Table 30-10: adds footnote for all parameters for 1:2 Doze ratio
	 • Table 30-11:
	   - changes Minimum and Maximum values for D120 and D130
	   - adds Minimum and Maximum values for D131
	   - adds Minimum and Maximum values for D150 through D156, and removes Typical values
	 • Table 30-12:
	   - reformats table for readability
	   - changes I_{OL} conditions for DO10
	 • Table 30-14: adds footnote to D135
	 • Table 30-17: changes Minimum and Maximum values for OS30
	 • Table 30-19:
	   - splits temperature range and adds new values for F20a
	   - reduces temperature range for F20b to extended temperatures only
	 • Table 30-20:
	   - splits temperature range and adds new values for F21a
	   - reduces temperature range for F20b to extended temperatures only
	 • Table 30-53:
	   - adds Maximum value to CM30
	   - adds footnote ("Parameter characterized...") to multiple parameters
	 • Table 30-55: adds Minimum and Maximum values for all CTMUI specifications, and removes Typical values
	 • Table 30-57: adds new footnote to AD09
	 • Table 30-58:
	   - removes all specifications for accuracy with external voltage references
	   - removes Typical values for AD23a and AD24a
	   - replaces Minimum and Maximum values for AD21a, AD22a, AD23a and AD24a with new values, split by Industrial and Extended temperatures
	   - removes Maximum value of AD30
	   - removes Minimum values from AD31a and AD32a
	   - adds or changes Typical values for AD30, AD31a, AD32a and AD33a
	 • Table 30-59:
	   - removes all specifications for accuracy with external voltage references
	   - removes Maximum value of AD30
	   - removes Typical values for AD23b and AD24b
	   - replaces Minimum and Maximum values for AD21b, AD22b, AD23b and AD24b with new values, split by Industrial and Extended temperatures
	   - removes Minimum and Maximum values from AD31b, AD32b, AD33b and AD34b
	   - adds or changes Typical values for AD30, AD31a, AD32a and AD33a
	 • Table 30-61: Adds footnote to AD51

Section 32.0 "DC and AC Device Characteristics Graphs"	• Updates Figure 32-6 (Typical I_{DD} @ 3.3V) with individual current vs. processor speed curves for the different program memory sizes
Section 33.0 "Packaging Information"	• Replaces drawing C04-149C (64-pin QFN, 7.15 x 7.15 exposed pad) with C04-154A (64-pin QFN, 5.4 x 5.4 exposed pad)