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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep128gp202t-e-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

File Name Addr. Bit 15 Bit 14 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 00 All Reset OC1CON1 0900 — — OCSIDL CCTSEL<2.0> — ENFLT8 ENFLT8 — OCFIT8 OCFIT8<		+- I U.	001	FUIC			CUGII	OUTFU			KE013		F						
OC1CON1 0900 — — ENFLTB ENFLTB ENFLTB OCFLTB OCFLTB OCFLTA TRIGMODE OCM<2:0> 0000 OC1CON2 9902 FLTMD FLTOUT FLTRIEN OCINV — — — OC32 OCTRIG TRIGSTAT OCFLTB OCFLTA TRIGMODE OCM<2:0> 0000 OC100N2 9902 FLTMD FLTRIEN OCINV — — — OC32 OCTRIG TRIGSTAT OCTRIS SYNCSEL 0000 OC100N2 9906 — — Output Compare 1 Beotondary Register XXXX OC2001 9906 — — OLTME 1 Register XXXX XXXX OC2001 9904 — — OC32 OCTRIG TRIGSTAT OCTRIS SYNCSEL 9000 OC2001 9906 — OCSIDL OCTRE — ENFLTB ENFLTB ENFLTB OCTRIS SYNCSEL 9000 CZ200 PLTMU PLTMU<	File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1CON2 0902 FLTMD FLTNIEN OCINV — — OC22 OCTRIG TRIGSTAT OCTRIS SYNCSEL4:0> 0000 OC1RN 0906	OC1CON1	0900	_	—	OCSIDL	C	CTSEL<2:	0>	—	ENFLTB	ENFLTA	_	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>	•	0000
0C1RS 0904	OC1CON2	0902	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS		SYN	NCSEL<4:0)>		000C
OC1R 096	OC1RS	0904							Outp	out Compare	e 1 Seconda	ary Register							xxxx
0C1TMR 0908	OC1R	0906								Output Co	mpare 1 Re	egister							xxxx
OC2CON1 090A — OCSIDL C_TSEL<2:> — ENFLTB ENFLTB M OCFLTB OCFLTA TRIGMODE OCM 000000000000000000000000000000000000	OC1TMR	0908								Timer V	alue 1 Regi	ster							xxxx
OC2CON2 0900 FLTMU FLTMU FLTNIEN OCINV - - OC32 OCTRIG TRIGSTAT OCTRIS SYNCSEL4:0> OOD OC2R 0906 - - OC4 Corras SYNCSEL4:0> OOD OOD OC2R OOD Corras SYNCSEL4:0> OOD OO	OC2CON1	090A		—	OCSIDL	0	CTSEL<2:	0>	—	ENFLTB	ENFLTA	_	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>		0000
OC2RS 0906 Image: Second Windows Condows	OC2CON2	090C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS		SYN	NCSEL<4:0)>		000C
OC2R 0910 UNIC UNIC UNIC UNIC UNIC UNIC UNIC UNIC	OC2RS	090E							Outp	out Compare	e 2 Seconda	ary Register						xxxx	
OC2TMR 0912 Image: Second	OC2R	0910								Output Co	mpare 2 Re	egister							xxxx
OC3CON1 0914 — — OCSIDL OCTSEL<2:> — ENFLTB ENFLTA — OCFLTB OCFLTA TRIGMODE OCM<2:>> 000000000000000000000000000000000000	OC2TMR	0912								Timer V	alue 2 Regi	ster							xxxx
OC3CON20916FLTMDFLTOUTFLTRIENOCINV———OC32OCTRIGTRIGSTATOCTRISSYNCSEL4:0>0000OC3RS09180918	OC3CON1	0914		—	OCSIDL	0	CTSEL<2:	0>	—	ENFLTB	ENFLTA	_	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>		0000
OC3Rs 0918 Output Compare 3 Secondary Register xxxx OC3R 091A	OC3CON2	0916	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS		SYN	NCSEL<4:0)>		000C
OC3R 091A	OC3RS	0918							Outp	out Compare	e 3 Seconda	ary Register							xxxx
OC3TMR 091C	OC3R	091A								Output Co	mpare 3 Re	egister							xxxx
OC4CON1 091E — OCSIDL OCTSEL<2:··· — ENFLTB ENFLTB OCFLTB OCFLTB OCFLTA TRIGMODE OCM<2:0> 000000000000000000000000000000000000	OC3TMR	091C								Timer V	alue 3 Regi	ster							xxxx
OC4CON2 0920 FLTMD FLTRIEN OCINV — — OC32 OCTRIG TRIGSTAT OCTRIS SYNCSEL<4:0> 000000000000000000000000000000000000	OC4CON1	091E	—	—	OCSIDL	0	CTSEL<2:	0>	_	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE		OCM<2:0>		0000
OC4Rs0922Output Compare 4 Secondary RegisterxxxxOC4R0924Output Compare 4 RegisterxxxxOC4TMR0926Timer Value 4 Registerxxxx	OC4CON2	0920	FLTMD FLTOUT FLTTRIEN OCINV OC32 OCTRIG TRIGSTAT OCTRIS SYNCSEL<4:0> 000									000C							
OC4R 0924 Output Compare 4 Register xxxx OC4TMR 0926 Timer Value 4 Register xxxx	OC4RS	0922	Output Compare 4 Secondary Register							xxxx									
OC4TMR 0926 Timer Value 4 Register xxxx	OC4R	0924								Output Co	mpare 4 Re	egister							xxxx
	OC4TMR	0926		Timer Value 4 Register xxxx															

TABLE 4-10: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 4 REGISTER MAP

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-19: SPI1 AND SPI2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	:	SPIBEC<2:0	>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI1CON1	0242	_	_	_	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	—	_	_	_	FRMDLY	SPIBEN	0000
SPI1BUF	0248							SPI1 Tra	ansmit and F	Receive Buf	fer Registe	r						0000
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	:	SPIBEC<2:0)>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI2CON1	0262	_	—		DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	—	_	_	_	FRMDLY	SPIBEN	0000
SPI2BUF	0268	68 SPI2 Transmit and Receive Buffer Register 0000																

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-56: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00			—			—		TRISA8				TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	011F
PORTA	0E02		-	—	-	-	—	-	RA8	_	_	-	RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04	_	_	_	_	_	_	_	LATA8	_	_	_	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	_	_	_	_	_	_	_	ODCA8	_	_	_	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08	_	_	_	_	_	_	_	CNIEA8	_	_	_	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	_	_	_	_	_	_	_	CNPUA8	_	_	_	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	_	_	_	_	_	_	_	CNPDA8	_	_	_	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E			—			—		_	_			ANSA4		-	ANSA1	ANSA0	0013

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-57: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	_	_	_	_	_	_	_	ANSB8	_	_	_	_	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-58: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	—	_	—	_	—	—	—	TRISC8	_	—	—	—	—	—	TRISC1	TRISC0	0103
PORTC	0E22	—	_	—	_	_	_	_	RC8		—	_	_	_	_	RC1	RC0	xxxx
LATC	0E24	—	_	—	_	—	—	—	LATC8		_	—	—	—	_	LATC1	LATC0	xxxx
ODCC	0E26	—	_	—	_	—	—	—	ODCC8		_	—	—	—	_	ODCC1	ODCC0	0000
CNENC	0E28	—	_	—	_	—	—	—	CNIEC8		_	—	—	—	_	CNIEC1	CNIEC0	0000
CNPUC	0E2A	—	_	—	_	—	—	—	CNPUC8		_	—	—	—	_	CNPUC1	CNPUC0	0000
CNPDC	0E2C	—	_	—	_	—	—	—	CNPDC8		_	—	—	—	_	CNPDC1	CNPDC0	0000
ANSELC	0E2E	_	_	_	_	_	_	_	_	_	_	_	_	_		ANSC1	ANSC0	0003

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	ILR3	ILR2	ILR1	ILR0
bit 15	·					•	bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VECNUM7	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-12	Unimplemen	ted: Read as '	0'				
bit 11-8	ILR<3:0>: Ne	w CPU Interru	pt Priority Lev	el bits			
	1111 = CPU	Interrupt Priori	y Level is 15				
	•						
	•						
	0001 = CPU 0000 = CPU	Interrupt Priorif Interrupt Priorif	y Level is 1 y Level is 0				
bit 7-0	VECNUM<7:0	D>: Vector Nun	- nber of Pendin	g Interrupt bits			
	11111111 = 2	255, Reserved	; do not use	0			
	•						
	•						
	•						
	00001001 =	9, IC1 – Input (Capture 1				
	00001000 =	8, INT0 – Exter	rnal Interrupt ()			
	00000111 = 00000110 = 00000110 = 00000110 = 00000110 = 00000100000000	7, Reserved; d	o not use				
	00000101 = 00000101 = 000000101 = 00000000	5. DMAC error	trap				
	00000100 =	4, Math error tr	ap				
	00000011 =	3, Stack error t	rap				
	00000010 = 2	2, Generic har	d trap				
	00000001 =	1, Address erro	or trap				
	0000000000	o, Oscillator la	nuap				

REGISTER 7-7: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STB<	23:16>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown

REGISTER 8-5: DMAXSTBH: DMA CHANNEL X START ADDRESS REGISTER B (HIGH)

bit 15-8 Unimplemented: Read as '0'

bit 7-0 STB<23:16>: Secondary Start Address bits (source or destination)

REGISTER 8-6: DMAXSTBL: DMA CHANNEL X START ADDRESS REGISTER B (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STE	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			ST	3<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimpler	mented bit, rea	id as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	x = Bit is unkr	nown	

bit 15-0 **STB<15:0>:** Secondary Start Address bits (source or destination)

11.5 I/O Helpful Tips

- In some cases, certain pins, as defined in Table 30-11, under "Injection Current", have internal protection diodes to VDD and Vss. The term, "Injection Current", is also referred to as "Clamp Current". On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the Vss and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device, that is clamped internally by the VDD and Vss power rails, may affect the ADC accuracy by four to six counts.
- 2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '0', regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a '0'.
- **Note:** Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.
- 3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
- 4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(VDD - 0.8), not VDD. This value is still above the minimum VIH of CMOS and TTL devices.

5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specification. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH, and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of this data sheet. For example:

VOH = 2.4V @ IOH = -8 mA and VDD = 3.3VThe maximum output current sourced by any 8 mA I/O pin = 12 mA.

LED source current < 12 mA is technically permitted. Refer to the VOH/IOH graphs in Section 30.0 "Electrical Characteristics" for additional information.

- 6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:
 - a) Only one "output" function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).
 - b) It is possible to assign a "remappable output" function to multiple pins and externally short or tie them together for increased current drive.
 - c) If any "dedicated output" function is enabled on a pin, it will take precedence over any remappable "output" function.
 - d) If any "dedicated digital" (input or output) function is enabled on a pin, any number of "input" remappable functions can be mapped to the same pin.
 - e) If any "dedicated analog" function(s) are enabled on a given pin, "digital input(s)" of any kind will all be disabled, although a single "digital output", at the user's cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input provided there is no external analog input, such as for a built-in self-test.
 - f) Any number of "input" remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable "output".

REGISTER 11-15: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

	5444.0	D 44/ 0	D 444 0		D 44/ 0	D 444 0			
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—				SYNCI1R<6:0)>				
bit 15							bit 8		
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—	—	—		—	—	—	—		
bit 7				-	•		bit 0		
Legend:									
R = Readabl	le bit	W = Writable b	oit	U = Unimpler	mented bit, read	l as '0'			
-n = Value at	-n = Value at POR			'0' = Bit is cle	eared	x = Bit is unknown			
bit 15	Unimplemer	nted: Read as '0)'						
bit 14-8	SYNCI1R<6: (see Table 11	• 0>: Assign PWI I-2 for input pin :	VI Synchroniz selection nur	zation Input 1 to nbers)	o the Correspon	ding RPn Pin b	its		
	1111001 = 	nput tied to RPI	121						
	•								
	•								
	0000001 = I	nout tied to CME	21						
	0000000 = 1	nput tied to Vss							
bit 7-0	Unimplemer	nted: Read as '0)'						

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 6	STREN: SCLx Clock Stretch Enable bit (when operating as I ² C slave) Used in conjunction with the SCLREL bit. 1 = Enables software or receives clock stretching 0 = Disables software or receives clock stretching
bit 5	ACKDT: Acknowledge Data bit (when operating as I ² C master, applicable during master receive)
	Value that is transmitted when the software initiates an Acknowledge sequence. 1 = Sends NACK during Acknowledge 0 = Sends ACK during Acknowledge
bit 4	ACKEN: Acknowledge Sequence Enable bit (when operating as I ² C master, applicable during master receive)
	 1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit. Hardware is clear at the end of the master Acknowledge sequence. 0 = Acknowledge sequence is not in progress
bit 3	RCEN: Receive Enable bit (when operating as I ² C master)
	 1 = Enables Receive mode for I²C. Hardware is clear at the end of the eighth bit of the master receive data byte. a Receive acquirement in program.
hit 2	0 = Receive sequence is not in progress
511 2	 1 = Initiates Stop condition on SDAx and SCLx pins. Hardware is clear at the end of the master Stop sequence. a Stop condition is not in processor.
h :+ 4	0 = Stop condition is not in progress
DIT	RSEN: Repeated Start Condition Enable bit (when operating as I-C master)
	 Initiates Repeated Start condition on SDAx and SCLX pins. Hardware is clear at the end of the master Repeated Start sequence. 0 = Repeated Start condition is not in progress
bit 0	SEN: Start Condition Enable bit (when operating as l^2C master)
	 1 = Initiates Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Start sequence. 0 = Start condition is not in progress

Note 1: When performing master operations, ensure that the IPMIEN bit is set to '0'.

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	_	_	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0
bit 15							bit 8
U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
	ICODE6	ICODE5	ICODE4	ICODE3	ICODE2	ICODE1	ICODE0
bit 7			1	1	I	1	bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own
bit 15-13	Unimplemen	ted: Read as '	0'				
bit 12-8	FILHIT<4:0>:	Filter Hit Num	ber bits				
	10000-1111	1 = Reserved					
	01111 = Filte	r 15					
	•						
	•						
	•						
	00001 = Filte 00000 = Filte	r 1 r 0					
bit 7	Unimplemen	ted: Read as '	0'				
bit 6-0	ICODE<6:0>:	: Interrupt Flag	Code bits				
	1000101-11	11111 = Rese	rved				
	1000100 = F	IFO almost full	interrupt				
	1000011 = R 1000010 = W	ake-up interru	pt				
	1000001 = E	rror interrupt					
	1000000 = N	o interrupt					
	•						
	•						
	•						
	0010000-01	11111 = Kese B15 buffer inte	rved				
	•		nupt				
	•						
	•						
	0001001 = R	B9 buffer inter	rupt				
	0001000 = R	B8 buffer inter	rupt				
	0000111 = T	RB7 buffer inte	rrupt				
	0000110 = 1	RB5 buffer inte	errupt				
	0000100 = T	RB4 buffer inte	errupt				
	0000011 = T	RB3 buffer inte	rrupt				
	0000010 = T	RB2 buffer inte	rrupt				
	0000001 = T	RB1 buffer inte	errupt				
			πupι				

REGISTER 21-3: CxVEC: ECANx INTERRUPT CODE REGISTER

REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER (CONTINUED)

- bit 1 **RBIF:** RX Buffer Interrupt Flag bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 0 **TBIF:** TX Buffer Interrupt Flag bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred

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REGISTER 21-22: CxRXFUL1: ECANx RECEIVE BUFFER FULL REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8
bit 15							bit 8

| R/C-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| RXFUL7 | RXFUL6 | RXFUL5 | RXFUL4 | RXFUL3 | RXFUL2 | RXFUL1 | RXFUL0 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 **RXFUL<15:0>:** Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)

REGISTER 21-23: CxRXFUL2: ECANx RECEIVE BUFFER FULL REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXFUL31 | RXFUL30 | RXFUL29 | RXFUL28 | RXFUL27 | RXFUL26 | RXFUL25 | RXFUL24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXFUL23 | RXFUL22 | RXFUL21 | RXFUL20 | RXFUL19 | RXFUL18 | RXFUL17 | RXFUL16 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 **RXFUL<31:16>:** Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)

23.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

- **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. То complement the information in this data sheet. refer to "Analog-to-Digital Converter (ADC)" (DS70621) in the "dsPIC33/PIC24 Family Reference Manual', which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have one ADC module. The ADC module supports up to 16 analog input channels.

On ADC1, the AD12B bit (AD1CON1<10>) allows the ADC module to be configured by the user as either a 10-bit, 4 Sample-and-Hold (S&H) ADC (default configuration) or a 12-bit, 1 S&H ADC.

Note: The ADC module needs to be disabled before modifying the AD12B bit.

23.1 Key Features

23.1.1 10-BIT ADC CONFIGURATION

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) conversion
- · Conversion speeds of up to 1.1 Msps
- · Up to 16 analog input pins
- Connections to three internal op amps
- Connections to the Charge Time Measurement Unit (CTMU) and temperature measurement diode
- Channel selection and triggering can be controlled by the Peripheral Trigger Generator (PTG)
- External voltage reference input pins
- · Simultaneous sampling of:
 - Up to four analog input pins
 - Three op amp outputs
 - Combinations of analog inputs and op amp outputs
- Automatic Channel Scan mode
- Selectable conversion Trigger source
- · Selectable Buffer Fill modes
- Four result alignment options (signed/unsigned, fractional/integer)
- Operation during CPU Sleep and Idle modes

23.1.2 12-BIT ADC CONFIGURATION

The 12-bit ADC configuration supports all the features listed above, with the exception of the following:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only one S&H amplifier in the 12-bit configuration; therefore, simultaneous sampling of multiple channels is not supported.

Depending on the particular device pinout, the ADC can have up to 16 analog input pins, designated AN0 through AN15. These analog inputs are shared with op amp inputs and outputs, comparator inputs, and external voltage references. When op amp/comparator functionality is enabled, or an external voltage reference is used, the analog input that shares that pin is no longer available. The actual number of analog input pins, op amps and external voltage reference input configuration depends on the specific device.

A block diagram of the ADC module is shown in Figure 23-1. Figure 23-2 provides a diagram of the ADC conversion clock period.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
CH0NB		_	CH0SB4 ⁽¹⁾	CH0SB3 ⁽¹⁾	CH0SB2 ⁽¹⁾	CH0SB1 ⁽¹⁾	CH0SB0 ⁽¹⁾		
bit 15		·	•	•			bit 8		
R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
CH0NA			CH0SA4 ⁽¹⁾	CH0SA3 ⁽¹⁾	CH0SA2 ⁽¹⁾	CH0SA1 ⁽¹⁾	CH0SA0 ⁽¹⁾		
bit 7		•		•	•	•	bit 0		
Legend:									
R = Read	able bit	W = Writable b	oit	U = Unimpler	nented bit, read	as '0'			
-n = Value	e at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	iown		
bit 15	CH0NB: Cha	nnel 0 Negative	Input Select fo	r Sample MUX	B bit				
	1 = Channel (0 negative input	is AN1 ⁽¹⁾						
	0 = Channel (0 negative input	i s Vrefl						
bit 14-13	Unimplemented: Read as '0'								
bit 12-8	-8 CH0SB<4:0>: Channel 0 Positive Input Select for Sample MUXB bits ⁽¹⁾								
	11111 = Open; use this selection with CTMU capacitive and time measurement								
	11110 = Cha	nnel 0 positive inp	out is connected	to the CTMU te	emperature mea	surement diode	(CTMU TEMP)		
	11101 = Reserved								
	11011 = Res	erved							
	11010 = Cha	innel 0 positive ir	nput is the outp	out of OA3/AN6	₆ (2,3)				
	11001 = Cha	innel 0 positive ir	nput is the outp	out of OA2/AN)(2) (2)				
	11000 = Cha	innel 0 positive ir	nput is the outp	out of OA1/AN3	3(2)				
	•	erveu							
	•								
	•								
	10000 = Res	erved	anutia ANIZ (3)						
	01111 = Cha	innel 0 positive ir innel 0 positive ir	$\frac{1901 \text{ is AN 15}}{1001 \text{ is AN 14}}$						
	01101 = Cha	innel 0 positive ir	nput is AN13 ⁽³⁾						
	•								
	•								
	• $00010 = Cha$	innel () nositive ir	Dout is ANI2(3)						
	00001 = Cha	innel 0 positive ir	nput is AN1 ⁽³⁾						
	00000 = Cha	innel 0 positive ir	nput is AN0 ⁽³⁾						
bit 7	CH0NA: Cha	nnel 0 Negative	Input Select fo	r Sample MUX	A bit				
	1 = Channel (0 negative input	is AN1 ⁽¹⁾						
	0 = Channel (0 negative input	i s Vrefl						
bit 6-5	Unimplemen	ted: Read as '0'	,						
Note 1:	AN0 through AN to determine ho	17 are repurpose w enabling a par	ed when compa ticular op amp	rator and op a or comparator	mp functionality affects selection	v is enabled. Se on choices for C	e Figure 23-1 hannels 1, 2		
2:	The OAx input is	s used if the corr	responding on a	amp is selecte	d (OPMODE (C	MxCON<10>) =	= 1):		

REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER

3: See the "**Pin Diagrams**" section for the available analog channels for each device.

otherwise, the ANx input is used.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0
bit 7	·						bit 0
Legend:							
R = Readable bit W = Writable bit		oit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknown				

REGISTER 23-8: AD1CSSL: ADC1 INPUT SCAN SELECT REGISTER LOW^(1,2)

bit 15-0 CSS<15:0>: ADC1 Input Scan Selection bits

1 = Selects ANx for input scan

0 = Skips ANx for input scan

Note 1: On devices with less than 16 analog inputs, all AD1CSSL bits can be selected by the user. However, inputs selected for scan, without a corresponding input on the device, convert VREFL.

2: CSSx = ANx, where x = 0-15.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 24-12: PTGQPTR: PTG STEP QUEUE POINTER REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—	—		—	_	—		—		
bit 15							bit 8		
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—	—	—	PTGQPTR<4:0>						
bit 7							bit 0		

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-5 Unimplemented: Read as '0'

bit 4-0 **PTGQPTR<4:0>:** PTG Step Queue Pointer Register bits This register points to the currently active Step command in the Step queue.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-13: PTGQUEX: PTG STEP QUEUE REGISTER x (x = 0-7)^(1,3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
STEP(2x + 1)<7:0> ⁽²⁾									
bit 15							bit 8		
R/\\/_0	R/\/_0	R/\/_0	R/\/_0	R/W_0	R/\/_0	R/\/_0	R/\/_0		

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
STEP(2x)<7:0> ⁽²⁾								
bit 7 bit 0								

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8	STEP(2x + 1)<7:0>: PTG Step Queue Pointer Register bits ⁽²⁾
	A queue location for storage of the STEP(2x + 1) command byte
bit 7-0	STEP(2x)<7:0>: PTG Step Queue Pointer Register bits ⁽²⁾
	A queue location for storage of the STEP(2x) command byte.

- **Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).
 - 2: Refer to Table 24-1 for the Step command encoding.

3: The Step registers maintain their values on any type of Reset.

TABLE 30-48:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions	
SP70	FscP	Maximum SCK1 Input Frequency		_	11	MHz	(Note 3)	
SP72	TscF	SCK1 Input Fall Time	_		—	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO1 Data Output Fall Time			_	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO1 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	_	_	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns		
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	Ι	—	ns		
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)	
SP52	TscH2ssH, TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 Tcy + 40	—	_	ns	(Note 4)	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

AC CHARACTERISTICS				$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param. No.	Symbol	Characteristic ⁽³⁾		Min.	Max.	Units	Conditions	
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7		μS		
			400 kHz mode	1.3	_	μS		
			1 MHz mode ⁽¹⁾	0.5	—	μS		
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	-	μS	Device must operate at a minimum of 1.5 MHz	
			400 kHz mode	0.6	—	μS	Device must operate at a minimum of 10 MHz	
			1 MHz mode ⁽¹⁾	0.5		μS		
IS20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be from	
		Fall Time	400 kHz mode	20 + 0.1 CB	300	ns	10 to 400 pF	
			1 MHz mode ⁽¹⁾	—	100	ns		
IS21	TR:SCL	SDAx and SCLx	100 kHz mode	—	1000	ns	CB is specified to be from	
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
			1 MHz mode ⁽¹⁾	—	300	ns		
IS25	TSU:DAT	Data Input	100 kHz mode	250		ns		
	Setup Time	400 kHz mode	100		ns			
			1 MHz mode ⁽¹⁾	100		ns		
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0		μS		
			400 kHz mode	0	0.9	μS		
			1 MHz mode ⁽¹⁾	0	0.3	μS		
IS30	TSU:STA	Start Condition	100 kHz mode	4.7		μS	Only relevant for Repeated	
		Setup Time	400 kHz mode	0.6		μS	Start condition	
			1 MHz mode ⁽¹⁾	0.25	—	μS		
IS31	THD:STA	Start Condition	100 kHz mode	4.0	—	μS	After this period, the first	
		Hold Time	400 kHz mode	0.6	—	μS	clock pulse is generated	
			1 MHz mode ⁽¹⁾	0.25	—	μS		
IS33	Tsu:sto	Stop Condition	100 kHz mode	4.7	—	μS		
		Setup Time	400 kHz mode	0.6	—	μS		
			1 MHz mode ⁽¹⁾	0.6	—	μS		
IS34	THD:STO	Stop Condition	100 kHz mode	4	—	μS		
		Hold Time	400 kHz mode	0.6	—	μS		
			1 MHz mode ⁽¹⁾	0.25		μS		
IS40	TAA:SCL	Output Valid	100 kHz mode	0	3500	ns		
		From Clock	400 kHz mode	0	1000	ns		
			1 MHz mode ⁽¹⁾	0	350	ns		
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μS	Time the bus must be free	
			400 kHz mode	1.3	—	μS	perore a new transmission	
			1 MHz mode ⁽¹⁾	0.5	—	μS	Call Stall	
IS50	Св	Bus Capacitive Lo	bading	—	400	pF		
IS51	TPGD	Pulse Gobbler De	65	390	ns	(Note 2)		

TABLE 30-50: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

2: Typical value for this parameter is 130 ns.

3: These parameters are characterized, but not tested in manufacturing.

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$							
Param No.	Symbol	Characteristic	Min Typ Max			Units	Conditions			
	ADC Accuracy (12-Bit Mode) ⁽¹⁾									
HAD20a	Nr	Resolution ⁽³⁾	1:	12 Data Bits						
HAD21a	INL	Integral Nonlinearity	-5.5 — 5.5		LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V				
HAD22a	DNL	Differential Nonlinearity	-1 — 1		LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V				
HAD23a	Gerr	Gain Error	-10	_	10	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V			
HAD24a	EOFF	Offset Error	-5 — 5		LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V				
	Dynamic Performance (12-Bit Mode) ⁽²⁾									
HAD33a	FNYQ	Input Signal Bandwidth	_	_	200	kHz				

TABLE 31-12: ADC MODULE SPECIFICATIONS (12-BIT MODE)

Note 1: These parameters are characterized, but are tested at 20 ksps only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

TABLE 31-13: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHAF	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$						
Param No.	Symbol	Characteristic	Min Typ Max			Units	Conditions
		ADC A	ccuracy	(10-Bit I	Mode) ⁽¹⁾		
HAD20b	Nr	Resolution ⁽³⁾	10 Data Bits			bits	
HAD21b	INL	Integral Nonlinearity	-1.5 — 1.5		LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V	
HAD22b	DNL	Differential Nonlinearity	-0.25	-0.25 — 0.25		LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V
HAD23b	Gerr	Gain Error	-2.5	_	2.5	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V
HAD24b	EOFF	Offset Error	-1.25 — 1.25			LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V
		Dynamic P	Performa	nce (10-	Bit Mode	e) ⁽²⁾	
HAD33b FNYQ Input Signal Bandwidth — — 400 kHz							

Note 1: These parameters are characterized, but are tested at 20 ksps only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

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Microchip Tradema Architecture — Flash Memory Fam Program Memory S Product Group — Pin Count — Tape and Reel Flag Temperature Range Package Pattern	rk ily ize (Kb (if app	dsPI	C 33 EP 64 MC5 04 T 1/PT - XXX	Examples: dsPIC33EP64MC504-I/PT: dsPIC33, Enhanced Performance, 64-Kbyte Program Memory, Motor Control, 44-Pin, Industrial Temperature, TQFP package.
Architecture:	33 24	= =	16-bit Digital Signal Controller 16-bit Microcontroller	
Flash Memory Family:	EP	=	Enhanced Performance	
Product Group:	GP MC	= =	General Purpose family Motor Control family	
Pin Count:	02 03 04 06	= = =	28-pin 36-pin 44-pin 64-pin	
Temperature Range:	l E	= =	-40°C to+85°C (Industrial) -40°C to+125°C (Extended)	
Package:	ML MR MV PT SO SP SS TL TL		Plastic Quad, No Lead Package - (44-pin) 8x8 mm body (QFN) Plastic Quad, No Lead Package - (28-pin) 6x6 mm body (QFN-S) Plastic Quad, No Lead Package - (64-pin) 9x9 mm body (QFN) Thin Quad, No Lead Package - (64-pin) 9x9 mm body (UQFN) Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP) Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP) Plastic Small Outline, Wide - (28-pin) 7.50 mm body (SOIC) Skinny Plastic Dual In-Line - (28-pin) 300 mil body (SPDIP) Plastic Shrink Small Outline - (28-pin) 5.30 mm body (SOP) Very Thin Leadless Array - (36-pin) 5x5 mm body (VTLA) Very Thin Leadless Array - (44-pin) 6x6 mm body (VTLA)	